Challenges in Patterning High K Dielectrics

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Outline

- Hi-k etching methods and issues
- Gate structure and device parasitics
  - Fringing fields
  - External resistance
  - TSuprem4 and Medici Simulations

Hi-k Etch Overview

Hi-k Candidates:

ZrO_2
HfO_2
Al_2O_3
TiO_2
Ta_2O_5

Plasma Etch Gas:

- Chlorine based (Cl_2, CCl_4, BCl_3)
- Fluorine based
- Hydrogen containing
- Argon

Wet Etch Chemicals:

- HF
- Nitric, Phosphoric Acid

CMP Chemicals:

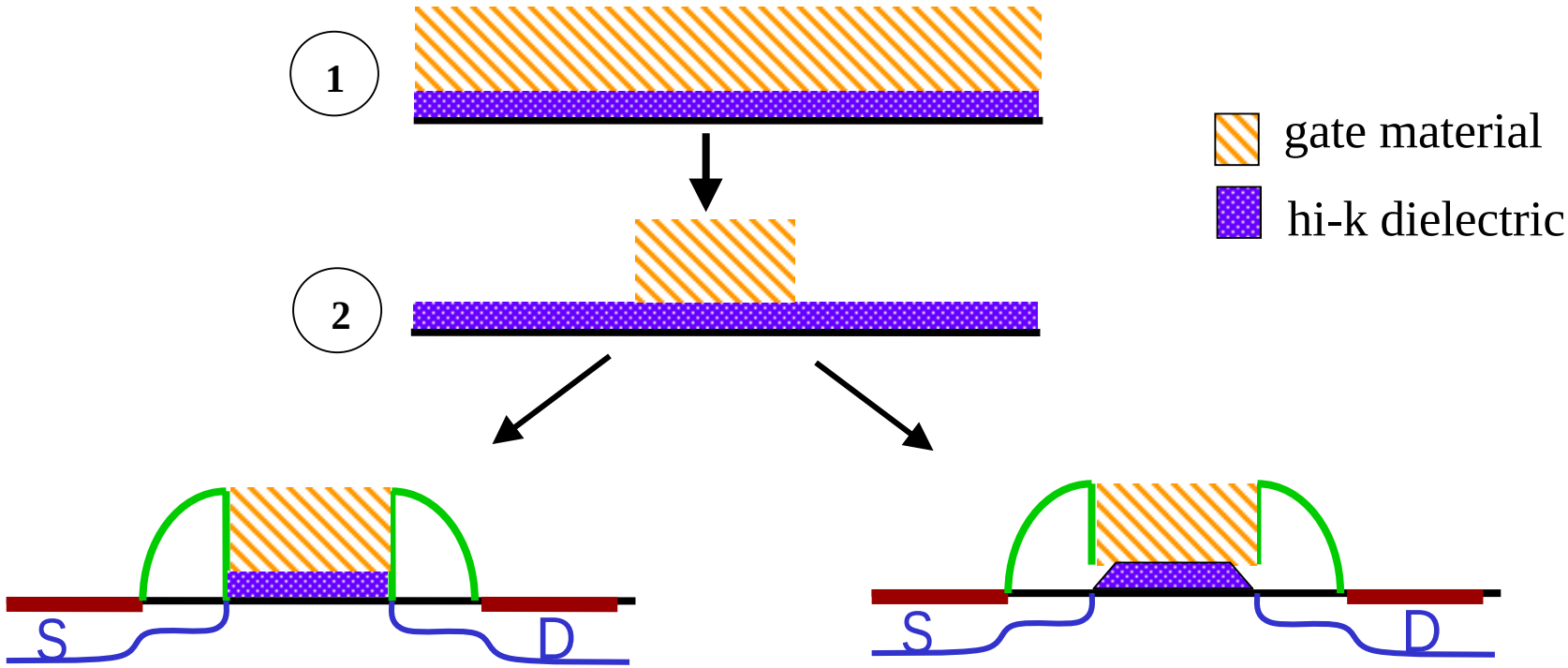
- Slurry

ESH concern

By-products:

- Toxic by-products ($ZrCl_2$,$HfCl_2$)
- Heavy metal waste
- CMP slurry

Direct Etch Processes



Anisotropic Etched Structure
- Plasma etching and/or sputtering
- Straight gate profile

Wet Etched Structure
- Wet chemicals
- Isotropic gate profile

Dry Etch Process Issue

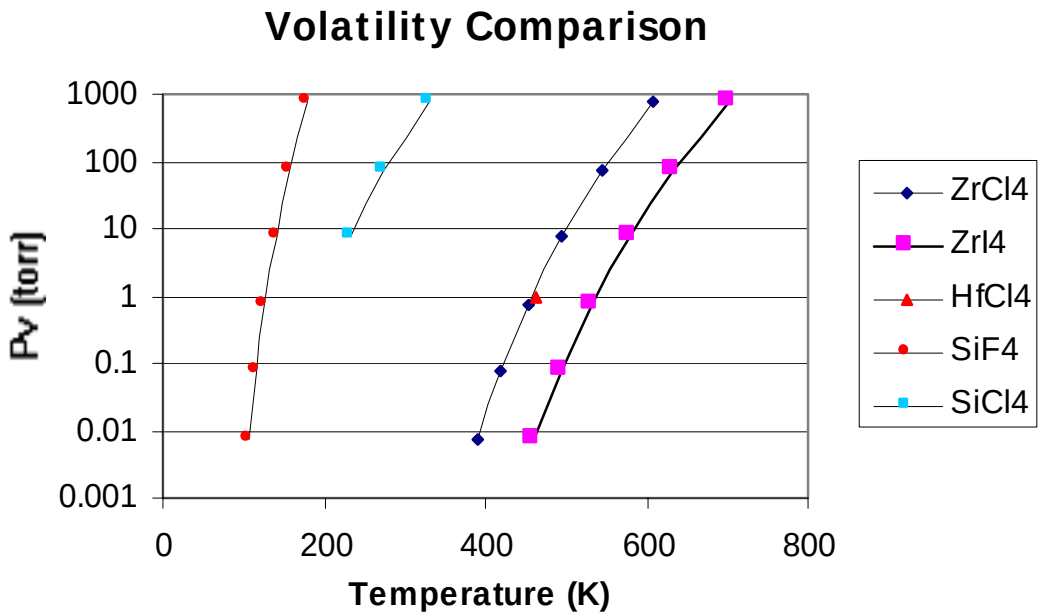
Sputtering

Material	Melting Point	Sputter Yield*
Si	1420°C	0.6
SiO_2	1610°C	0.13
TiO_2	1840°C	
Ta_2O_5	1800°C	
Al_2O_3	2035°C	0.04
ZrO_2	2550°C	

*Ar+, 1KeV

- Poor silicon selectivity
- Damage to silicon

Plasma (Chemical Enhanced)



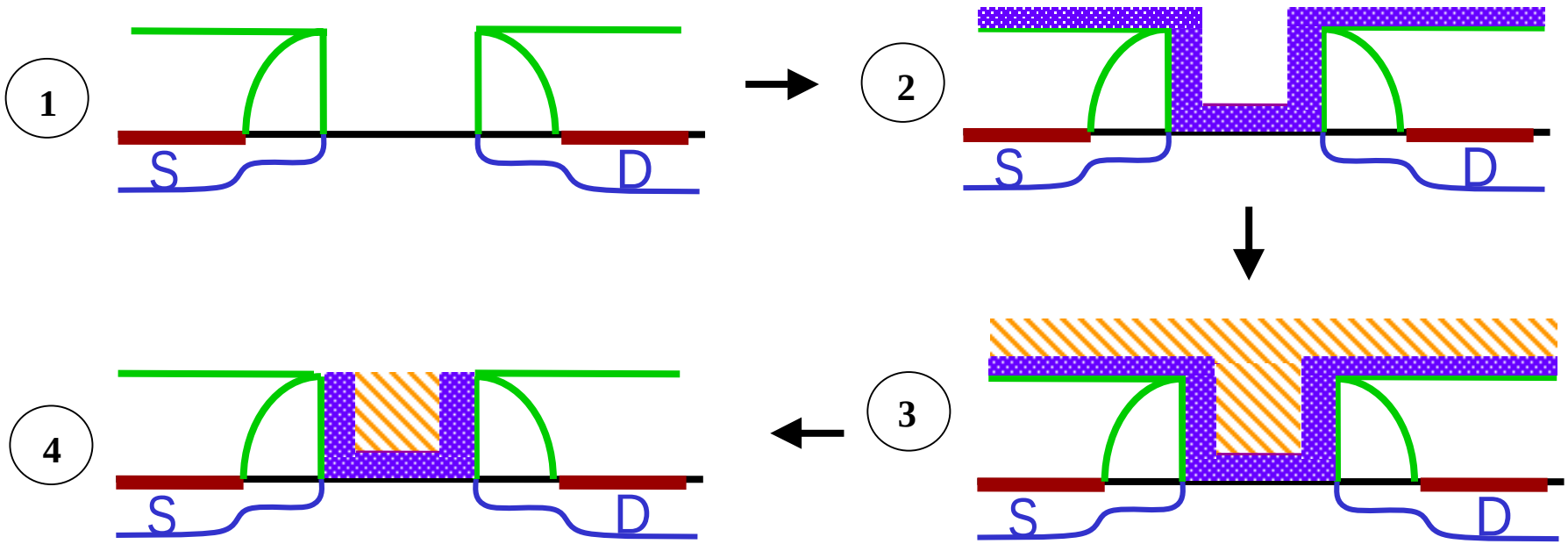
- Require heat to form volatile products
- Poor selectivity to silicon with Cl
- May require large physical component and polymer deposition for selectivity
- UV damage? -observed color change
- Toxic by-products

Wet Etch Process Issue

- Mostly HF based
- Very low etch rates for ZrO_2 and Ta_2O_5
- Etch rates of near interface silicates?
- Refill?
- Heavy metal by-product
- Undercut ––> Etch control critical

K (Hi-k)	Hi-k thickness	EOT	Gate length (nm)	% of gate length etched
8	3.1	1.5	100	3.1
8	2.1	1.0	65	3.2
8	1.6	0.8	45	3.6
8	1.0	0.5	22	4.7
25	9.6	1.5	100	9.6
25	6.4	1.0	65	9.9
25	5.1	0.8	45	11.4
25	3.2	0.5	22	14.6
100	38.5	1.5	100	38.5
100	25.6	1.0	65	39.4
100	20.5	0.8	45	45.6
100	12.8	0.5	22	58.3

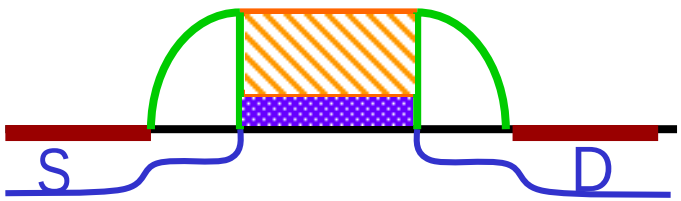
Replacement Gate Process



Two hi-k removal schemes

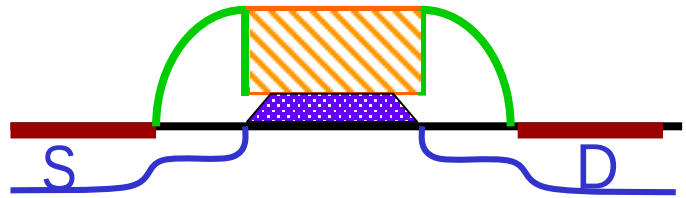
- CMP
- Etch stop on thick oxide

Hi-k Etch Structures



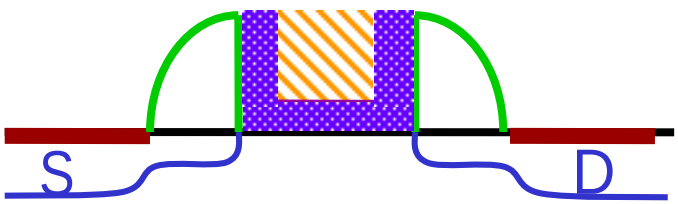
Direct Etched Structure

- Damage from plasma or sputtering
- Damage from source/drain implants
- Selectivity to silicon concern
- High post etch thermal budget



Wet Etched Structure

- Damage from source/drain implants
- Good selectivity to silicon
- High post etch thermal budget



Replacement Gate Structure

- Damage from plasma during removal
- Good selectivity
- Good thermal budget
- Process complexity

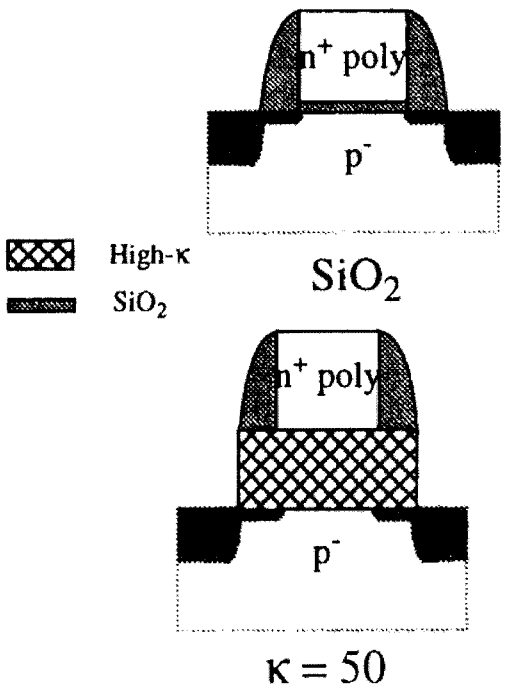
Which gate structure gives optimal device performance?

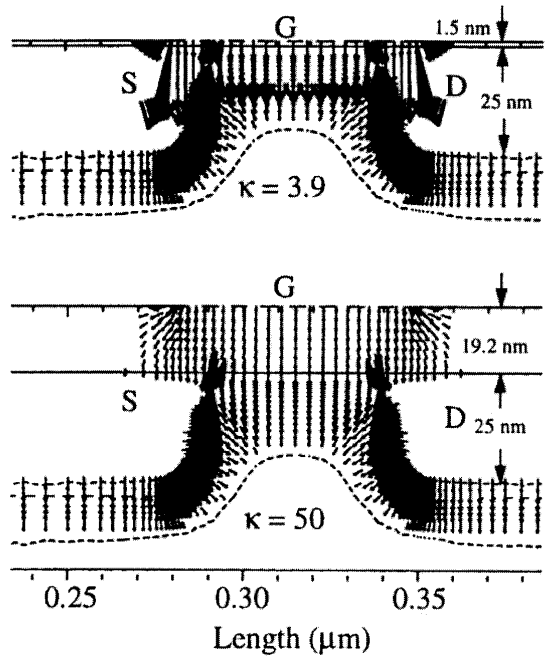
Device performance and reliability issues

- Post etch limited thermal budget for interface, dielectric, and gate material integrity
- Damage from plasma etching, sputtering and/or source/drain implants
- Resistance increase from overetch into silicon as result of poor selectivity
- Parasitic capacitance and resistance from gate structure geometry

Fringing Field Problem

Reference: Cheng, Baohong. etc al., IEEE TED July 1999





- Examined hi-k, multi-layered structure
- Field spreads as gate thickness increases
  - Effect scales as T_k/L_{gate}
- Loss of gate control

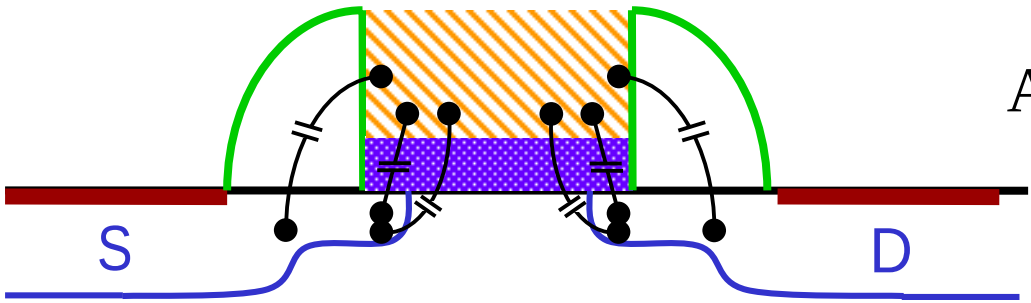
Transistor Parasitics Simulations

- Structures studied in our work: Replacement gate, Direct gate

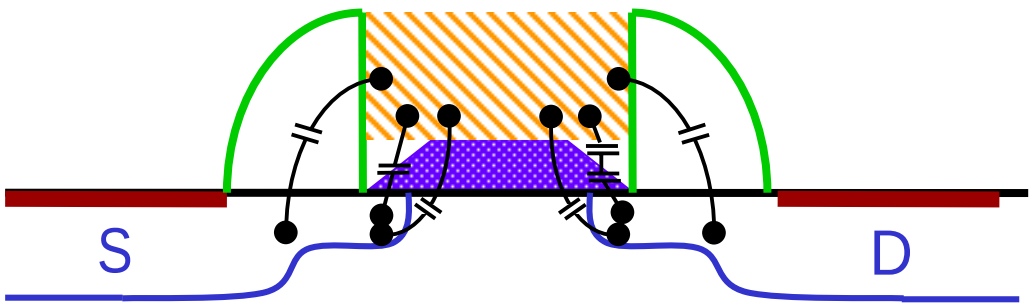
- TSuprem4:
  - Created transistor structure for the three gate structure geometries
  - Varied gate overlap with S/D, gate dielectric permitivity

- Medici:
  - Import structure from TSuprem4
  - Extrapolated the parasitic capacitance
  - Extrapolated the resistivity

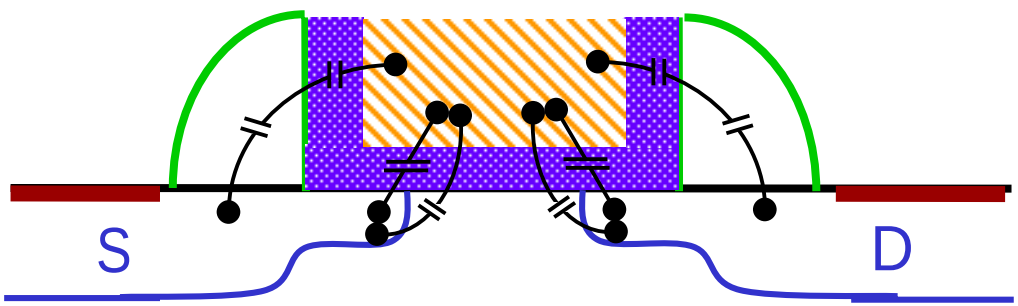
Parasitic Capacitance



Anisotropic Etched Structure

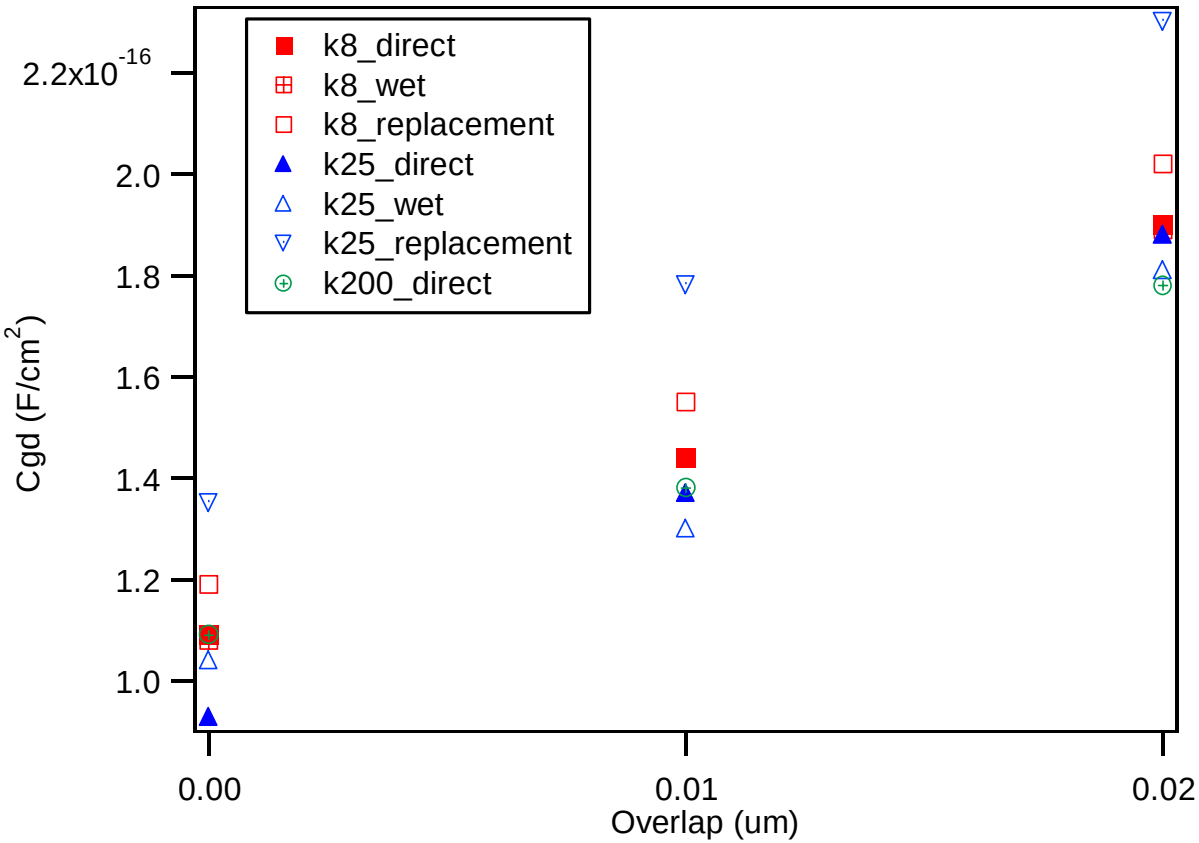


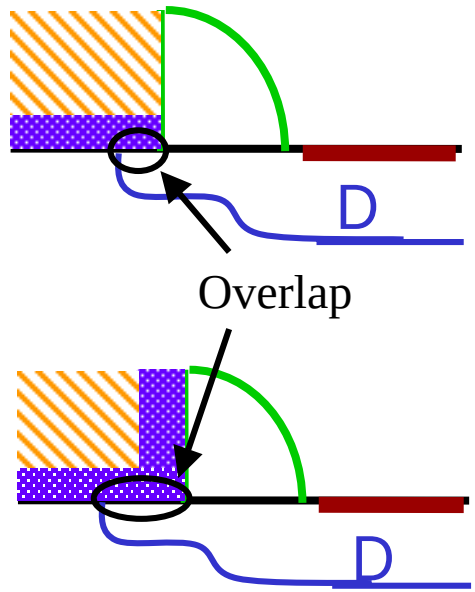
Wet Etched Structure



Replacement Gate Structure
(More gate/drain overlap)

Parasitic Capacitance



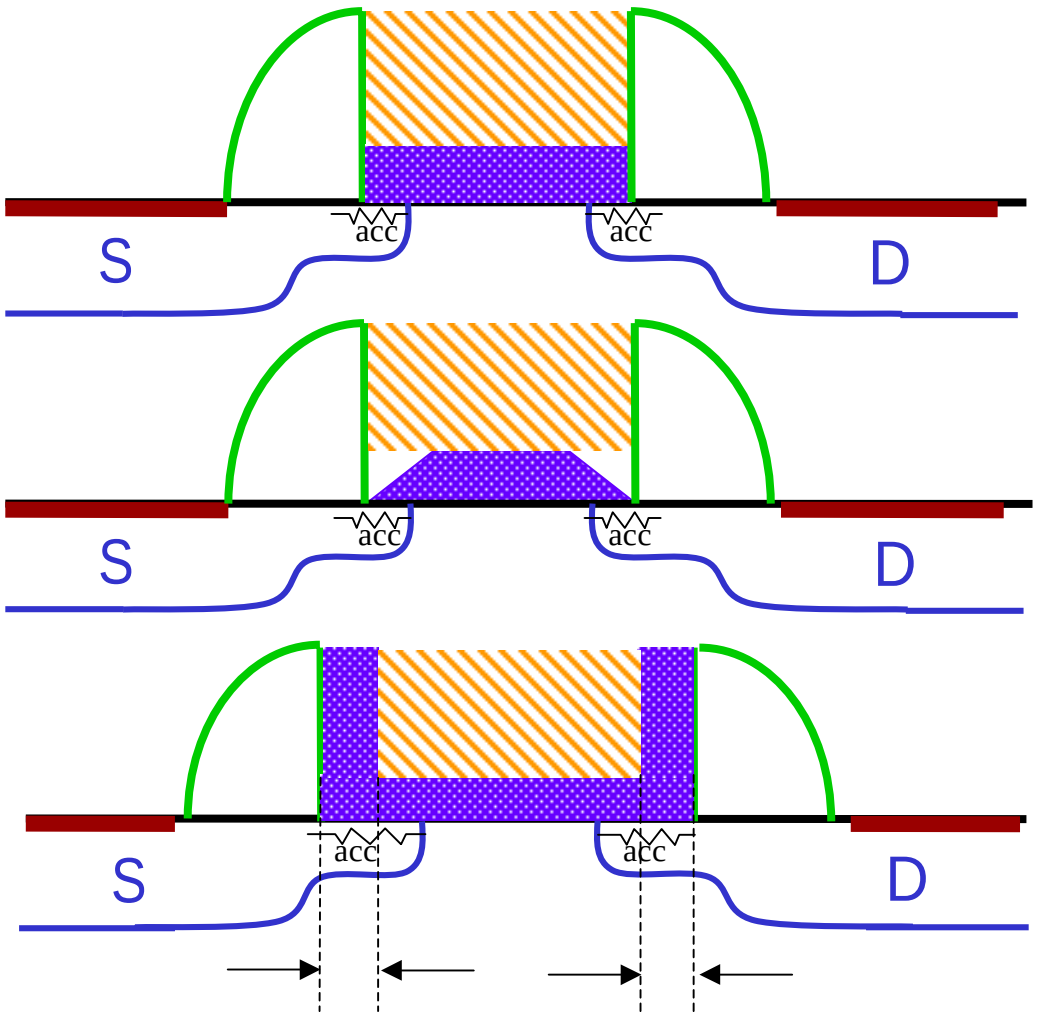


- Replacement gate shows higher parasitic capacitance
- Decrease overlap —> decrease parasitic capacitance

Effect of Parasitic Capacitance

- Increased parasitic capacitance slows switching speed
- 40% change in parasitic capacitance seen
- Simulations show 6% decrease in switching speed for an inverter circuit

External Resistance



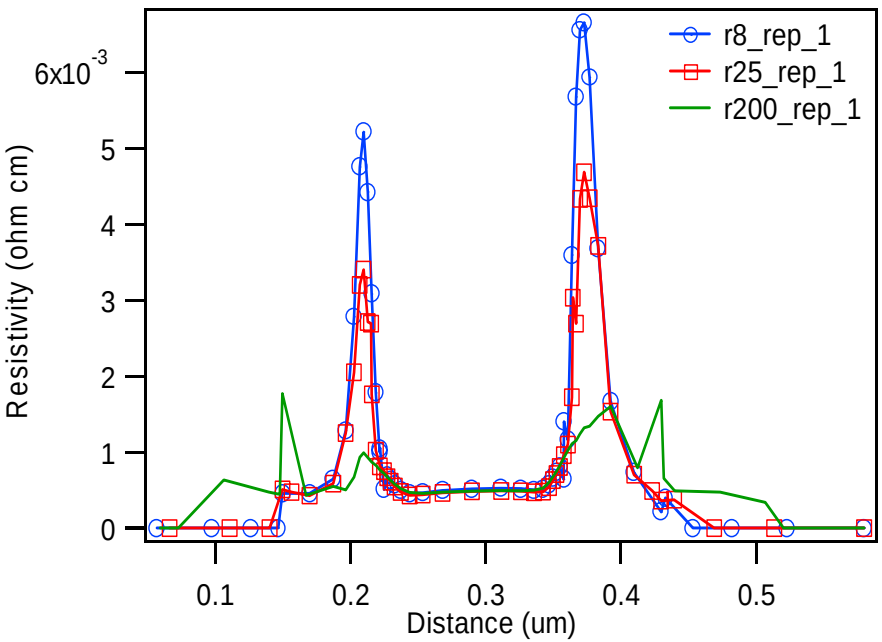
Anisotropic Etched Structure

Wet Etched Structure

Replacement Gate Structure

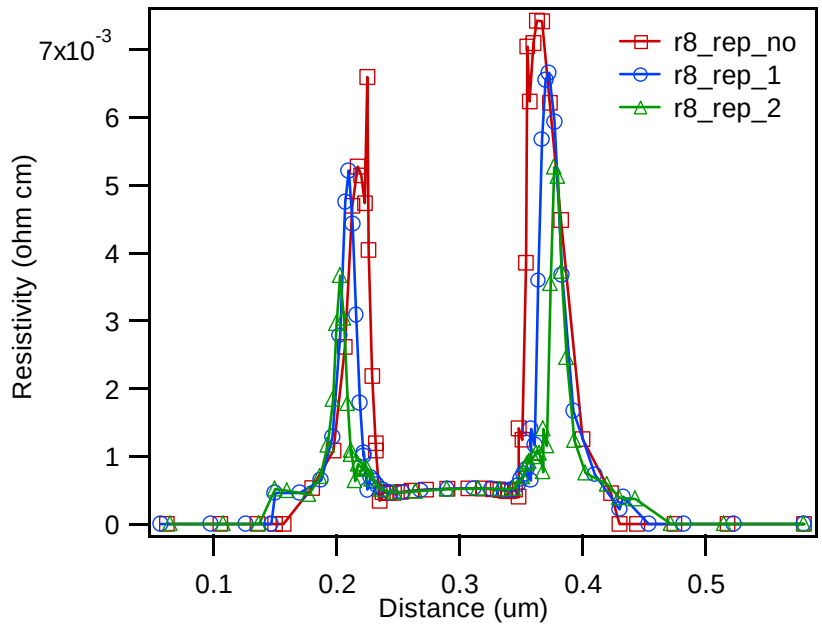
External Resistance

Resistivity for Various K



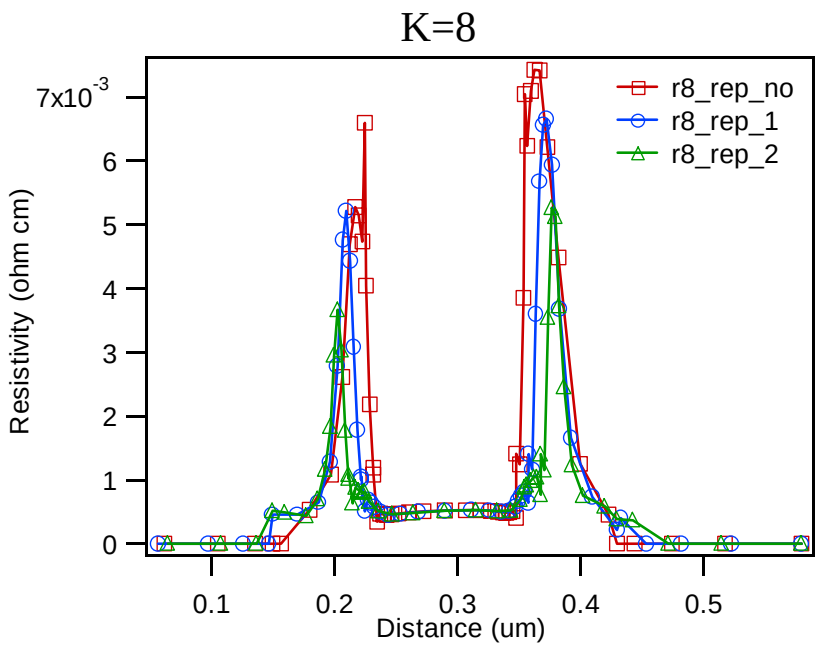
• Higher k –> decrease in resistance for replacement structure

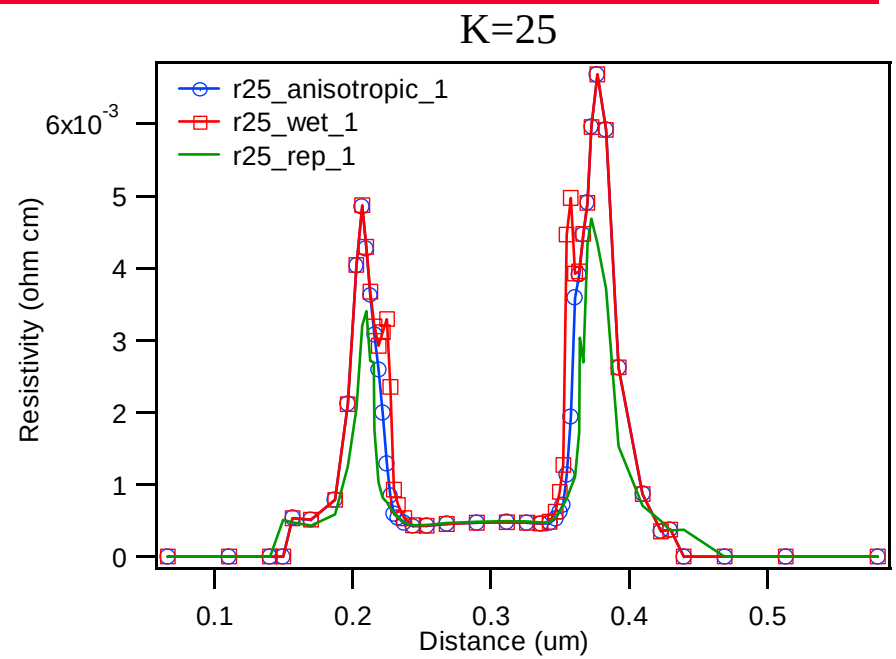
Resistivity for Various Overlaps

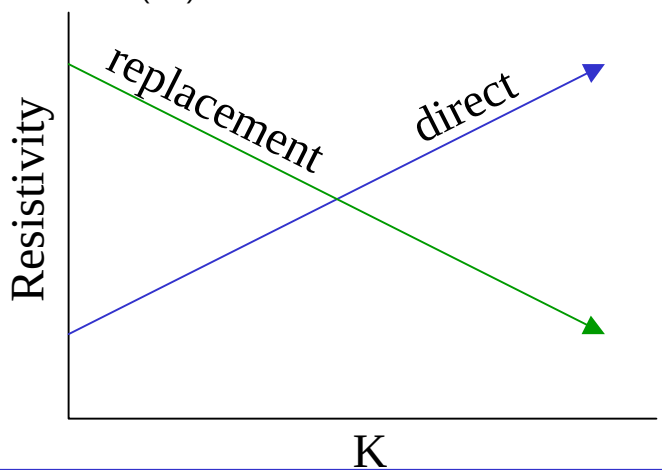


• Decrease in overlap –> increase in resistivity

External Resistance







- Competing effect on resistivity for overlap and $t_{Hi\text{-}k}$

Conclusion

Hi-k Etching

- Replacement gate approach
  - few etch problems
  - process complexity increase
  - increased parasitic capacitance
- Wet etch
  - limited by undercut
- Anisotropic etch
  - many etch challenges
  - best device

Device

- Parasitic capacitance worst for replacement gate
- Competing effects for resistivity