TOTAL SOLUTIONS™

CVD low k Solutions for sub-0.18um Technology

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OUTLINE

Introduction:

- Materials World.
- Low k Roadmap.

Inorganic Low K Materials

- FSG
- Black Diamond

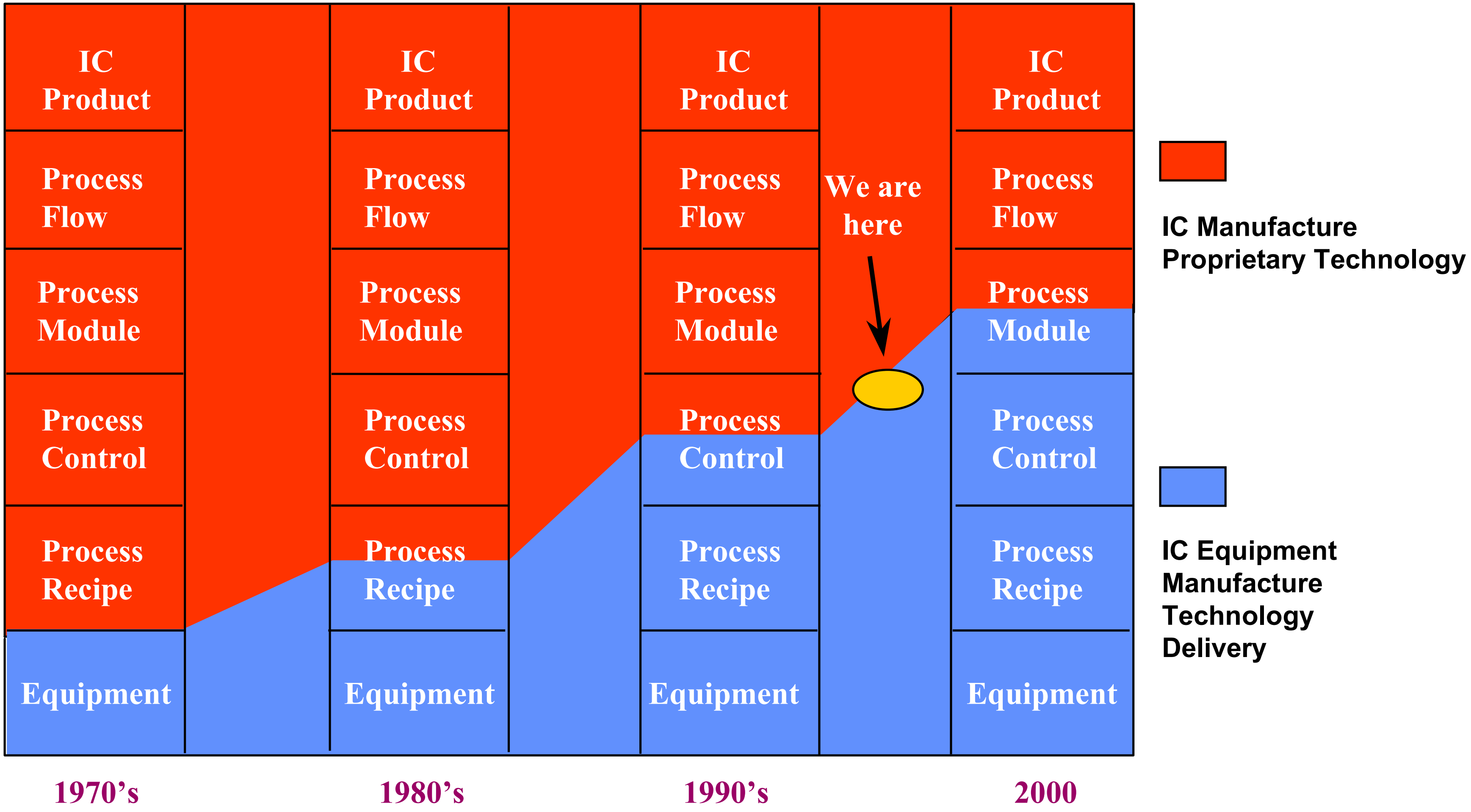
Barrier/Etch Stop Materials

- Copper Surface Treatment.
- BLOk.

CVD Remote Clean Technology

Summary

IC Manufacture/Equipment Industry Interaction



IC Product
Process Flow
Process Module
Process Control
Process Recipe
Equipment

We are here

🟥 IC Manufacture Proprietary Technology

🟦 IC Equipment Manufacture Technology Delivery

1970's
1980's
1990's
2000

Each Transition is Characterized by Change Cycle

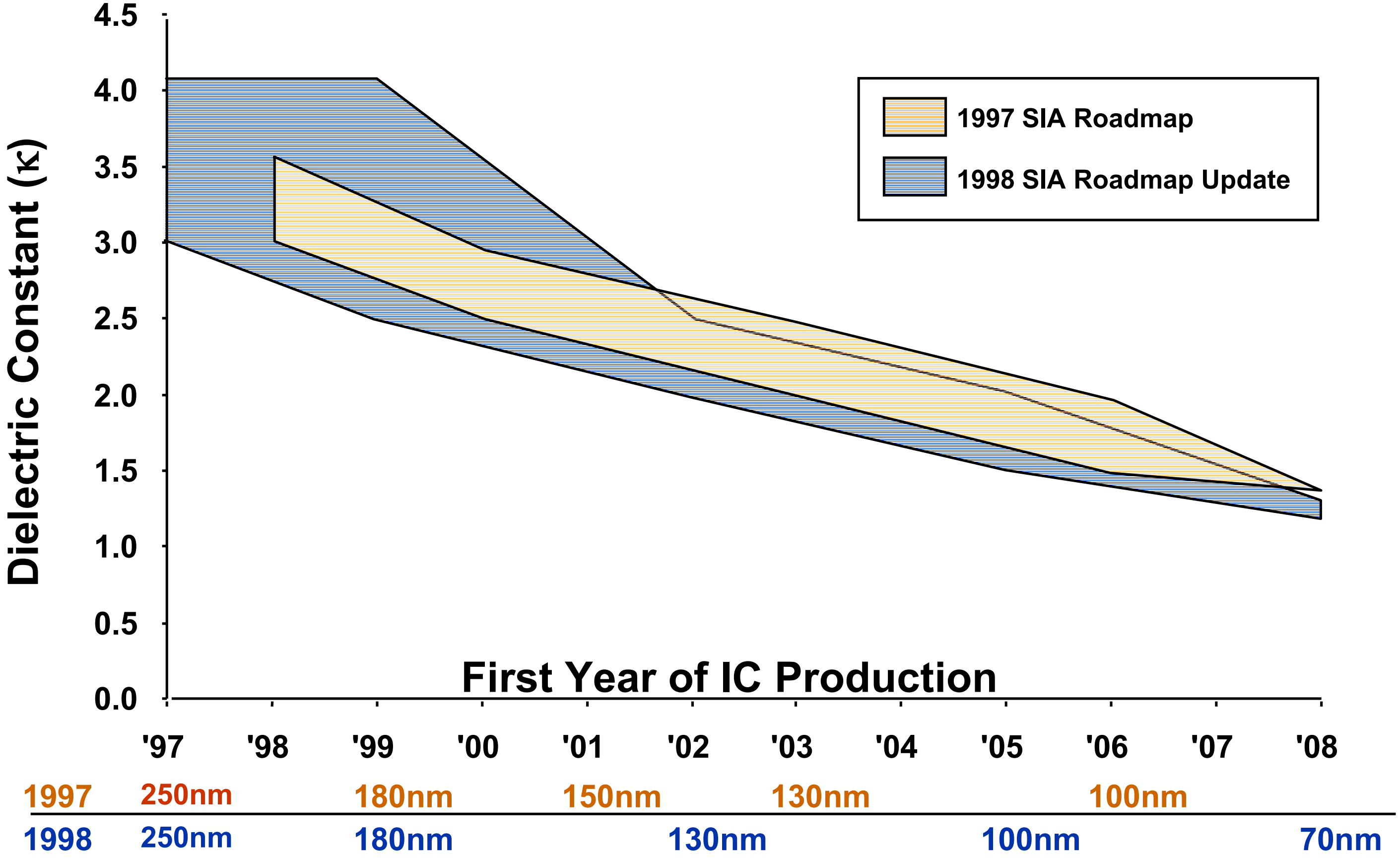
Source: Texas Instruments/Applied Materials

Driving Moore's Law

- Historically
  - 90% Dimensional Improvements, 10% Material Changes
  - Dimensional: Lithography and Etch
  - Materials: PSG-BPSG, PVD - CVD W, WSi_x-TiSi-CoSi
- Now
  - 50% Dimensional Improvements, 50% Material Changes
  - Dimensional: Lithography, Etch, Integration (T-Gate, Damascene)
  - Materials: TaO, BST, Low K Dielectric, Copper
- Future Beyond 0.1um - Trend Will Continue
  - 30% Dimensional Improvements, 70% Material Changes

More Emphasis on Performance due to Materials, in addition to the traditional Focus on Lithography

LOW κ SIA ROADMAP



- Dielectric constant range in Y2000 is 2.5-3.6, but expected to drop to <2.5 by 2002
- Expect another revision

HISTORY OF INDUSTRY LOW κ DEVELOPMENT

- The need for Cu/Low κ first introduced in 1994 NTRS
- First screening period (1995-1997) focused on k and thermal stability, since most initial candidates were organic SOD. Evaluation only involved 1 or 2 level metal damascene builds.
- Industry began to shift focus in 1998 to multi-level damascene integration compatibility. Thermal-mechanical properties become key criteria, which exposed deficiencies in many organic materials.
- Serious CVD options entered market in 1999 and continue to rapidly gained DTOR status. The majority of customers now looking at CVD carbon doped oxide as first viable k<3.0 product.

RECENT INTERCONNECT CONFERENCE SUMMARY

Advanced Semiconductor Manufacturing Conference, Sept 99 in Boston, MA

- Documentation by Dataquest specifically revising their prediction 2 years ago of first generation $\kappa<3.0$ materials being SOD to CVD C-Doped Oxide materials.

Advanced Metallization Conference, Sept 99 in Orlando, FL

- First generation low κ material will be FSG.
- Conference papers shows promising result of CVD Low κ, Carbon Doped Oxide.
- Key consensus from Panel Discussion:
    - CVD Low κ provides better reliability than SOD.
    - Toughness, mechanical strength and adhesion of Low κ are keys to success

<0.15μm Interconnect Materials Workshop, Nov 99 in Monterey, CA

- Oxide type of Low k materials is the most promising.
- Thermal-mechanical properties are the most crucial criteria for selection.

LOW κ MATERIALS FOR ADVANCED INTERCONNECTS

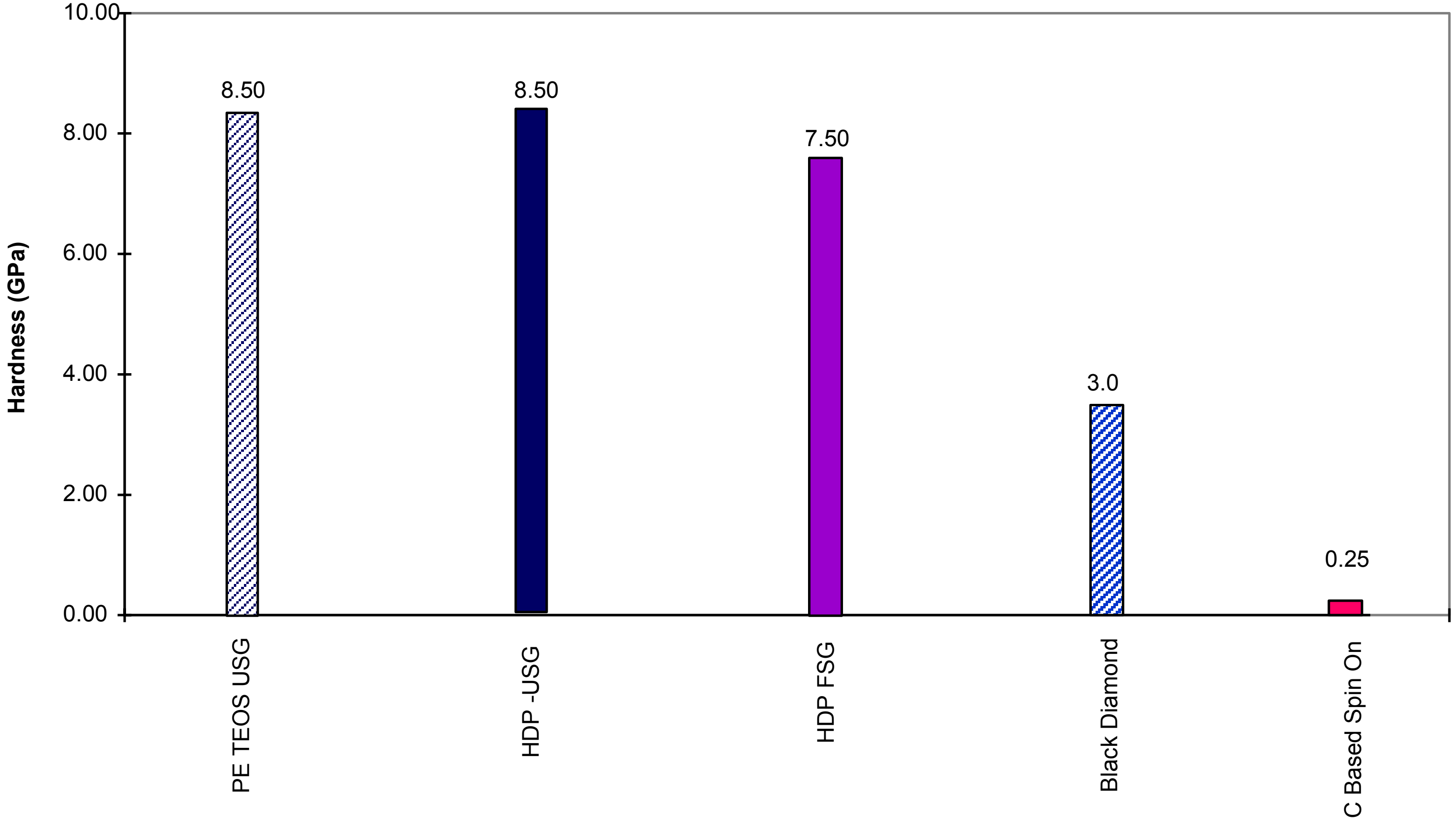
		Deposition Method	
		CVD	**Spin-on**
Material Type	**Inorganic**	• FSG • Black Diamond	• Fox (HSQ) • MSQ • LOSP (T-23) • Nanoglass
	Organic	• a:FC • Parylene AF4 • Copolymer	• Silk • BCB • Flare • PAE2 • AS 418

Inorganic CVD Low k:

- ***Proven CVD deposition technology***
- ***Oxide-like properties for ease of integration***

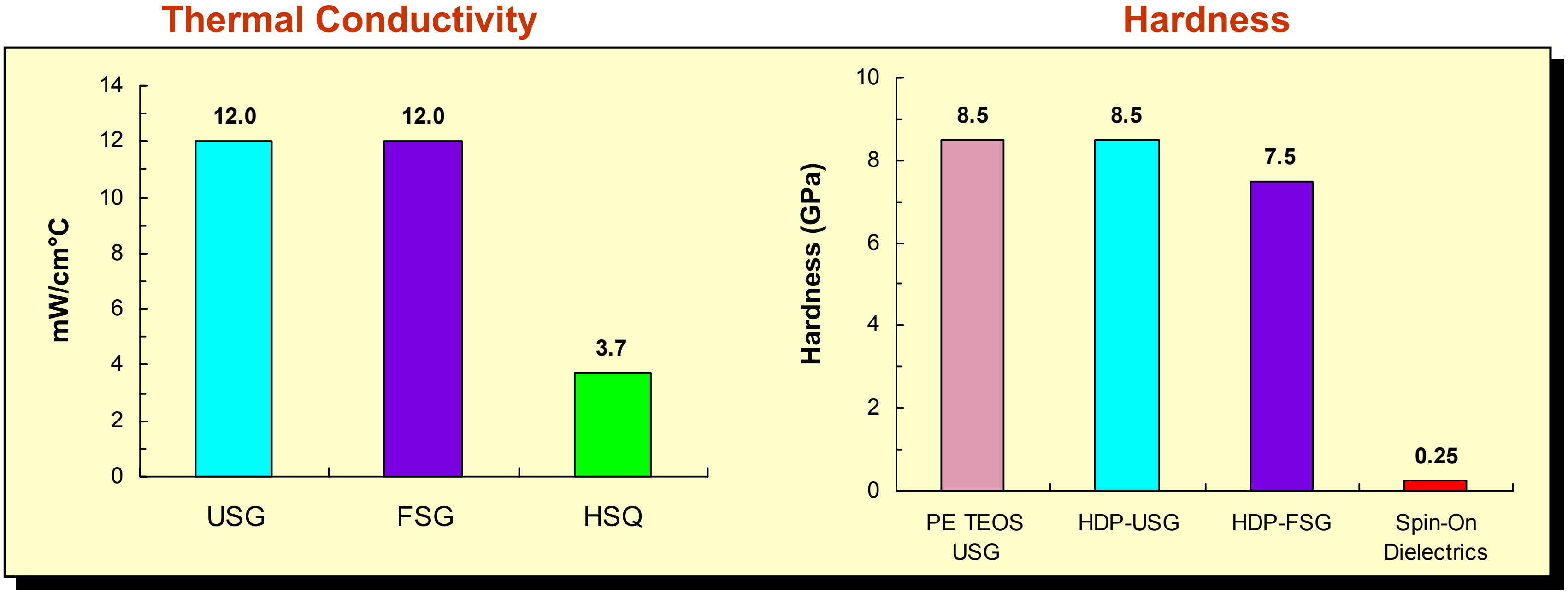
Hardness Measurement of Different Low κ Materials

(Nano Indentation Method)



ULTIMA HDP-CVD™ FSG

Bulk Film Comparison vs. HSQ



- High thermal conductivity critical for heat dissipation
  - FSG provides equivalent thermal properties to conventional oxides
  - >3x thermal conductivity of Low κ spin-on dielectrics

- High hardness critical for electromigration resistance, mechanical stability during CMP
  - FSG provides equivalent hardness to conventional oxides
  - >20x hardness of Low κ SODs

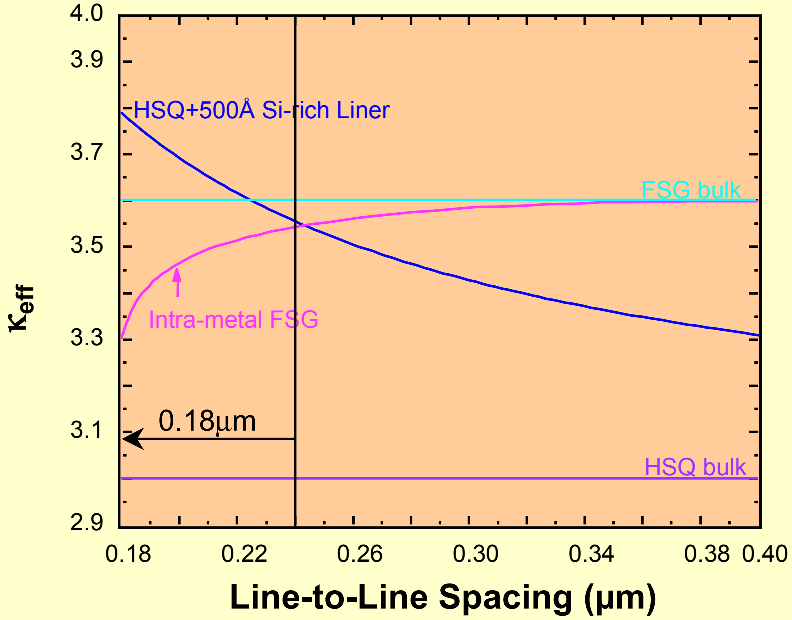
Oxide-Like Bulk Film Properties Contribute to Integration Ease, Device Reliability

ULTIMA HDP-CVD™

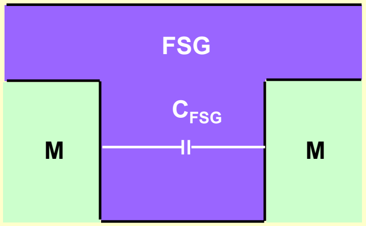
FSG and HSQ Dielectric Constant Comparison

FSG $\kappa_{eff} \leq$ HSQ κ_{eff} For Narrow Gaps

κ_{eff} as Function of Line-to-Line Spacing

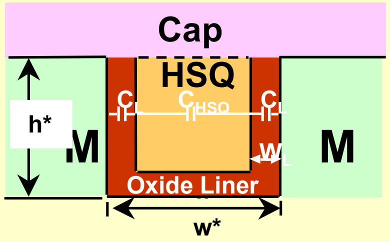


Full Flow FSG



- FSG κ decreases with smaller spacing due to higher F concentration between gaps

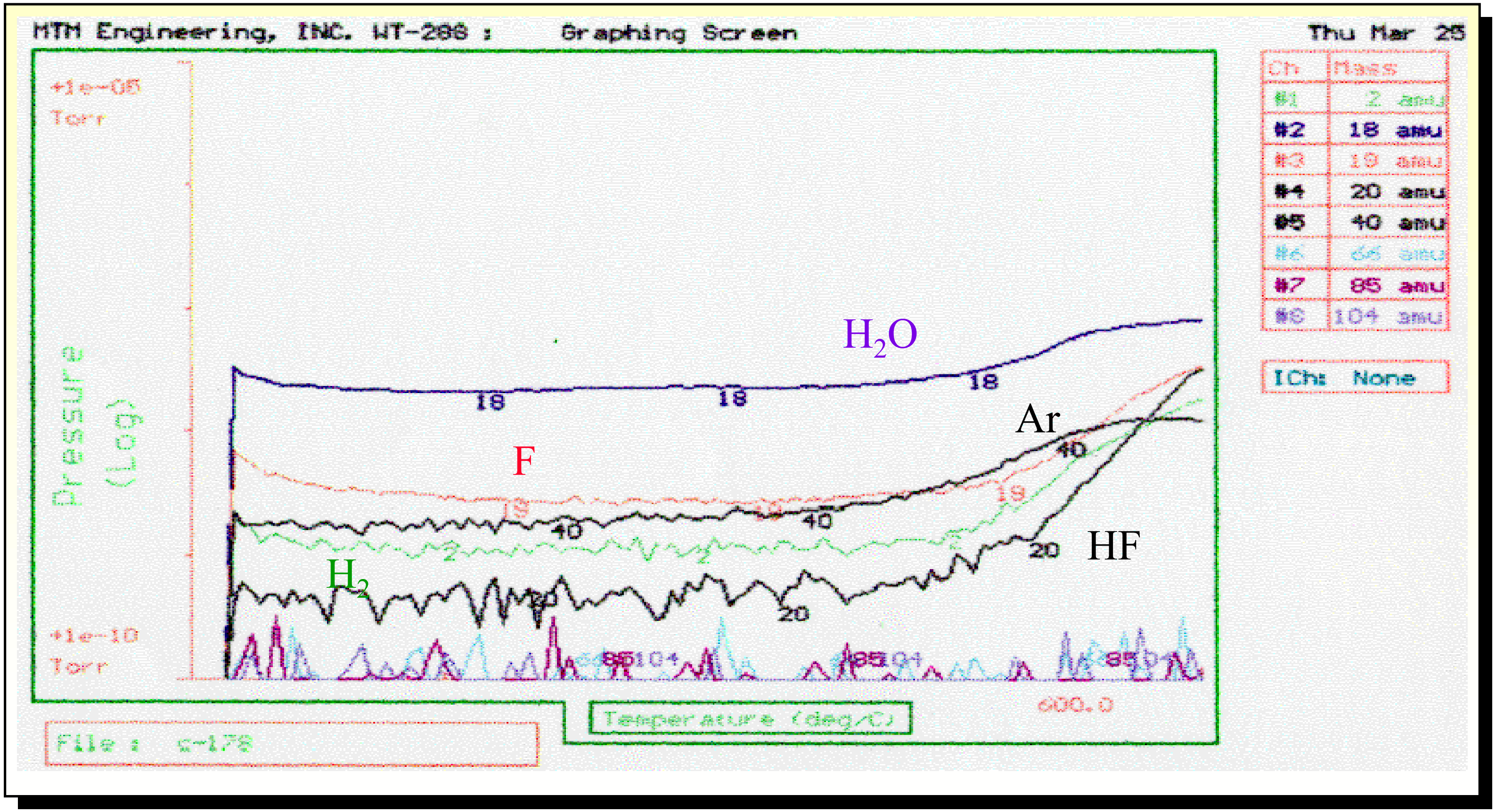
Embedded HSQ



- Use of liner inhibits low dielectric constant for HSQ in smaller spaces

Below 0.24µm spacing, FSG κ_{eff} is lower than HSQ due to impact of USG liner on effective κ

TDS Profile for $\kappa = 3.45$ HDP-FSG film



MTM Engineering, INC. WT-288 : Graphing Screen Thu Mar 25

Ch	Mass
#1	2 amu
#2	18 amu
#3	19 amu
#4	20 amu
#5	40 amu
#6	66 amu
#7	85 amu
#8	104 amu

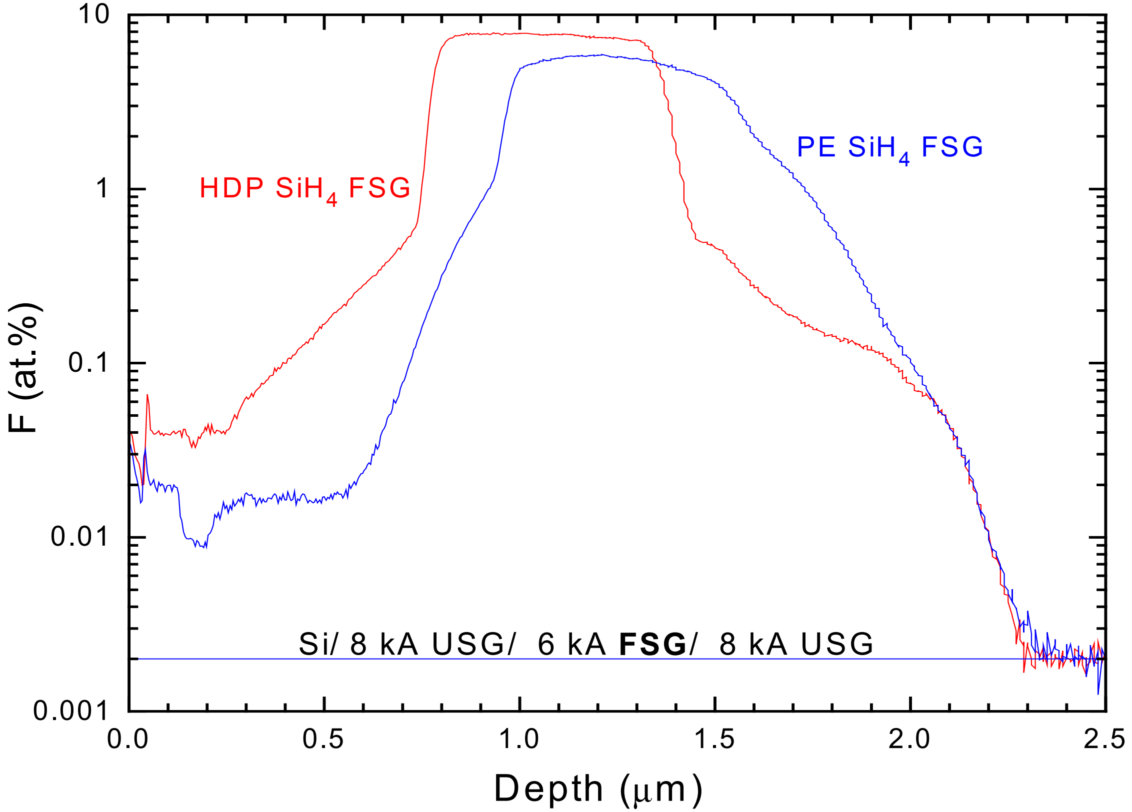
ICh: None

File : κ-178

No desorption of any species at temperatures lower than 500°C.

F Stability for different Processes

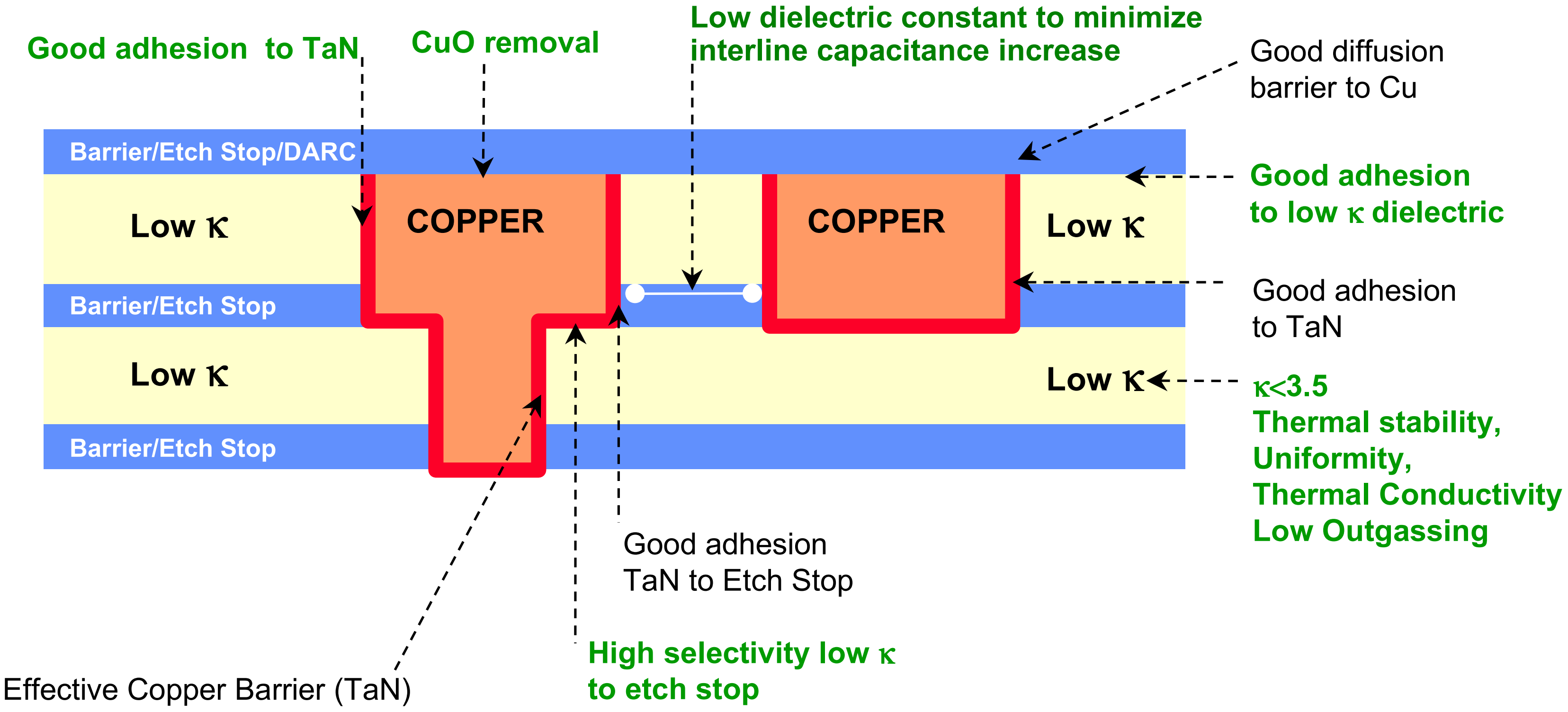
SIMS of F outdiffusion.



HDP-FSG is more stable than PE SiH_4 FSG.

Annealed at 410°C for 6 cycles in an N_2 ambient with 30 minutes each cycle.

DIELECTRIC FILM REQUIREMENTS FOR DUAL DAMASCENE INTEGRATION



Films must be compatible with:

Etch, CMP, Photolithography,Metallization modules

BLACK DIAMOND^{TM} LOW κ FILM
(κ = 2.6-3.0)

Simple Process Chemistry:

- Single wafer CVD reaction to form carbon doped oxide network
- Non-specialty chemicals as pre-cursors

Film Properties:

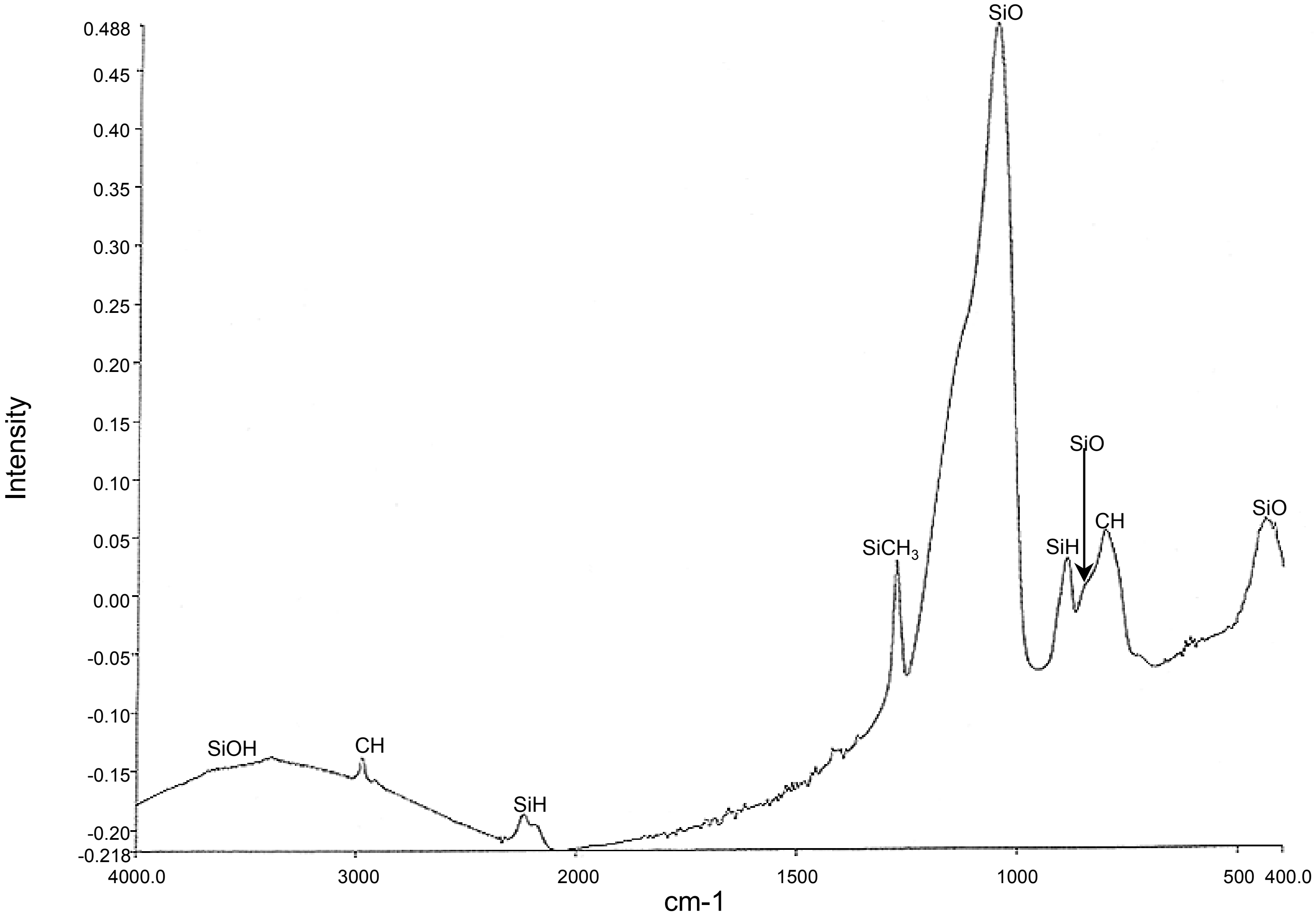
- Thermal and mechanical properties similar to silicon oxide

Integration:

- Silicon oxide like film properties simplify integration
- Compatible with copper/oxide damascene tool set

Black Diamond Film Composition

(FTIR)



Black Diamond Thermal Mechanical Properties Comparison

	Black Diamond	SiO_2	HSQ	Porous SiO_2	>20 at.% SiOC	Organic Polymer
Hardness (GPa)	1-3	7-8			0.4	0.1-0.3
CTE in plane (ppm/C)	5-15	~1.0	20	50-70	40-50	50-70
Biaxial E (Gpa)	10-15	70-80	5-10	2-3	5-7	2-3
Ther. Cond. (W/mC)	0.3-0.4	~1.0		0.05-0.07	<0.2	<0.1

Black Diamond has the most similar thermal mechanical properties to SiO_2 for $\kappa < 3.0$ materials

Issues for Organic and High C Content SiOC Films

- **Narrow process window for damascene etch**
  - Low etch rate and selectivity to SiN and photoresist

- **Poor ashing resistance**
  - Difficult sidewall polymer removal
  - Significant via sidewall pullback

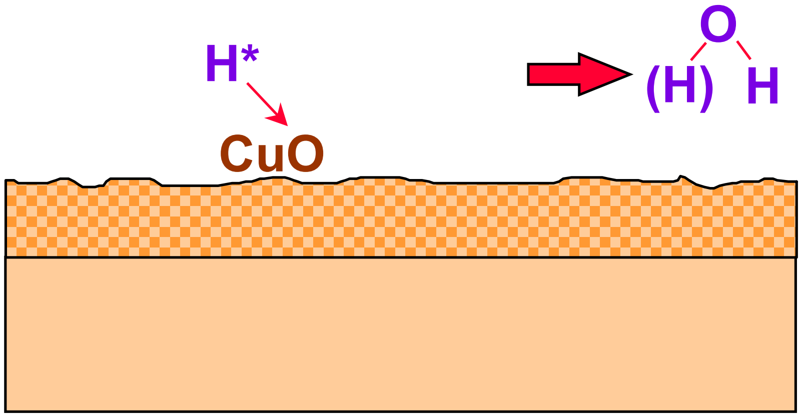
- **Possible leakage due to silicon carbide or dangling Si bonds**

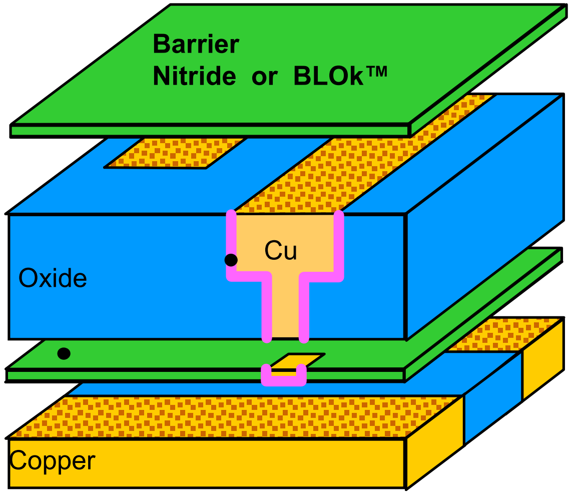
- **Poor thermal, mechanical properties**
  - Low hardness results in poor damascene structural integrity, incompatibility to CMP (peeling, scratches, etc.), Cu protrusions
  - High CTE and Low Young's Modulus affected via integrity
  - Low thermal conductivity causes excess Joule heating, resulting in poor EM lifetime and Cu protrusions

REACTIVE PLASMA COPPER OXIDE REMOVAL

Copper Pre Treatment (Remove Post CMP CuO)

$$3Cu_2O+2NH_3 \xrightarrow{300°C - 400°C} 6Cu+3H_2O\uparrow+N_2$$





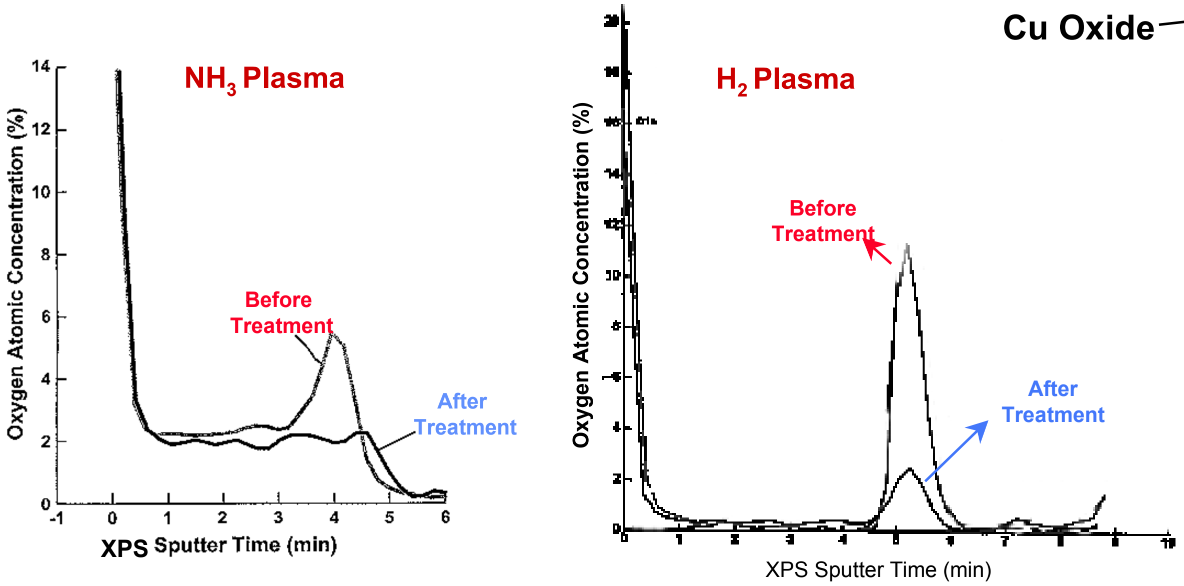
(1) Plasma generates atomic hydrogen
(2) Hydrogen reacts with CuO to form H_2O / OH + Cu
(3) Cu rebonds to form high quality large grain structure
(4) H_2O is pumped out

Published Papers:
(1) The reduction of copper oxide thin films with hydrogen plasma, Yasushi Sawada, et al., J. Phys. D:Appl. Phys. 29 (1996) 2539-2544.
(2) Surface cleaning of copper by thermal and plasma treatment… S. Hymes, et al., J. Vac. Sci. Technol. B 16(3), May/Jun 1998

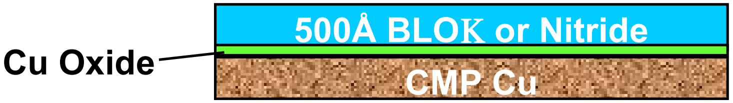
Cu DAMASCENE INTEGRATION

In Situ Plasma Treatment for Copper Oxide Removal

Oxygen Detection by ESCA/XPS



Wafer Without Treatment



Thin Cu Oxide layer interferes with adhesion

Stud Pull <1000PSI

Wafer with In Situ Plasma Treatment

Improves Adhesion

Stud Pull: >3000PSI *

In Situ Plasma Treatment Required for Good Cu/Barrier Adhesion

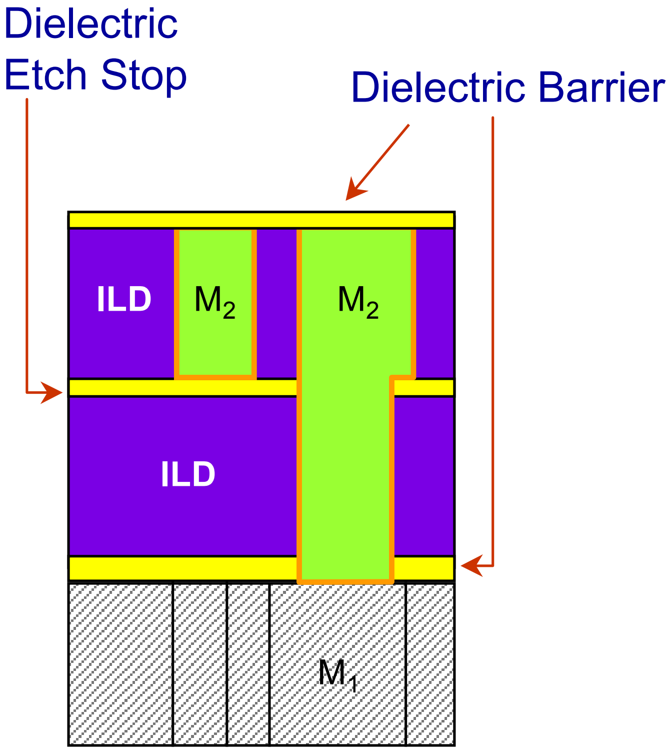
* Failed at epoxy/dielectric interface

** AMAT Electra Cu & Mirra Cu CMP + 500Å Barrier

** 10-30 sec. treatment

** BLOk Patent Pending

BLOκ^{TM}: Barrier Low κ

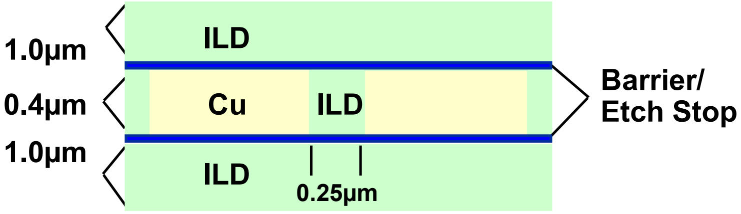


Why is a low κ barrier/etch stop necessary?

- Low κ dielectric materials are required to reduce RC time delay in <0.25 micron metal interconnects.
- Low κ barrier/etch stop has a *significant impact* on the effective κ value of the damascene structure.
- The current barrier/etch stop candidate is SiN which has a $\kappa > 7$.
- Applied Materials has developed a barrier/ etch stop candidate with $\kappa < 5.0$ (**B**arrier **LO**w **κ**).

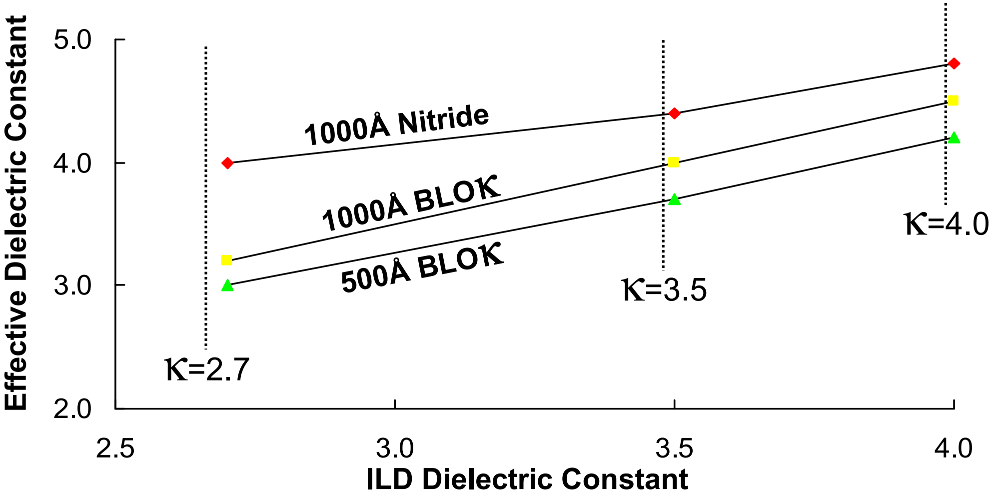
BARRIER IMPACT ON EFFECTIVE DIELECTRIC CONSTANT

Damascene Structure



Effective Dielectric Constant

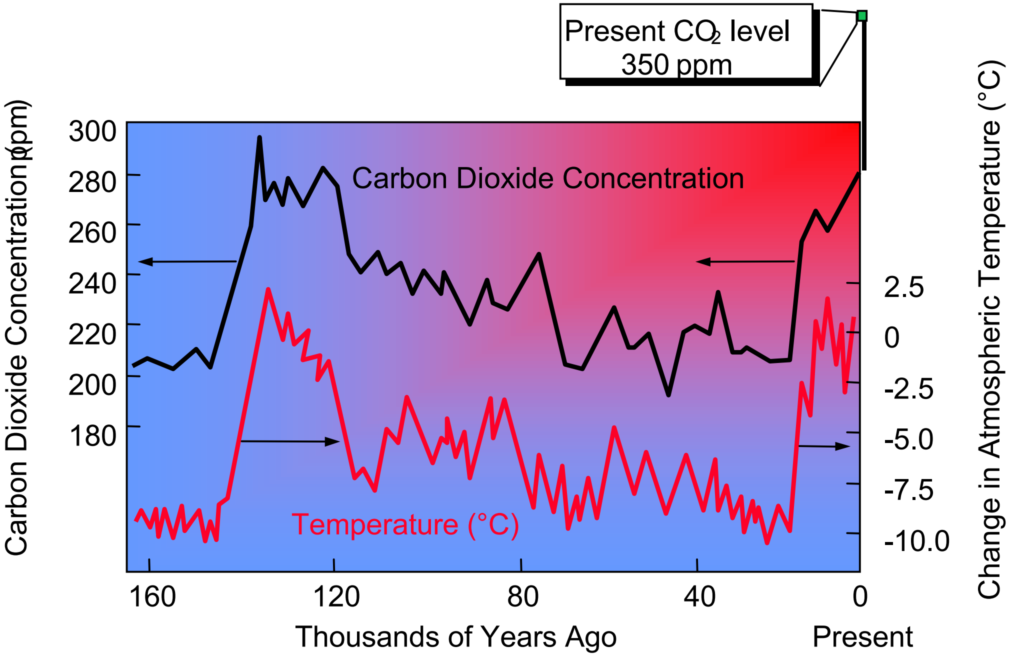
Barrier κ Value	ILD κ Value		
	USG κ=4.0	FSG κ=3.5	BD κ=2.7
1,000Å SiN (κ = 7.2)	4.8	4.4	4.0
1,000Å BLOk (κ = 5.0)	4.5	4.0	3.2
500Å BLOk (κ = 5.0)	4.2	3.7	3.0



Use of BLOκ Can Significantly Reduce Effective κ Value

* Data obtained using Raphael™ simulation

PFCs and Global Warming Potential



Gas	Lifetime (yrs.)	GWP (100yrs. ITH)	GWP (infinite ITH)
CO_2	50-100	1	1
CF_4	**50,000**	6,500	**850,000**
C_2F_6	10,000	9,200	230,000
SF_6	3,200	**23,900**	230,000
C_3F_8	7,000	7,000	130,000
NF_3	**740**	**8,000**	**18,000**
CHF_3	250	11,700	11,000

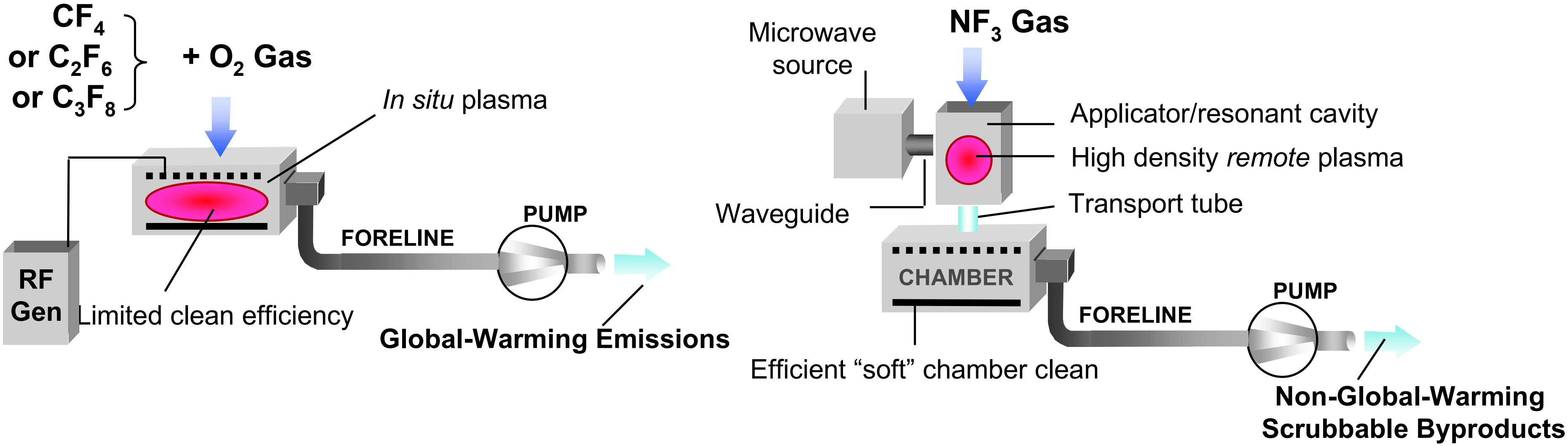
- **Global warming gases are causative agents***
- **“The world’s changing climatic conditions are more than the natural variability of weather.”✝**

- **PFC gases have long lifetime and high global warming potential (GWP)**

- 70 to 90% of PFC emissions from a semiconductor fab. are attributed to CVD chambers cleaning.
- The Semiconductor industry has taken a voluntary approach to reduce emissions.

- * Gribbin, The end of the ice ages? New Scientist, 1989.
- ✝ Conclusions of the IPCC (Intergovernmental Panel on Climate Change) - First Conference of the Parties, Framework Convention on Climate Change. Berlin, 1995.

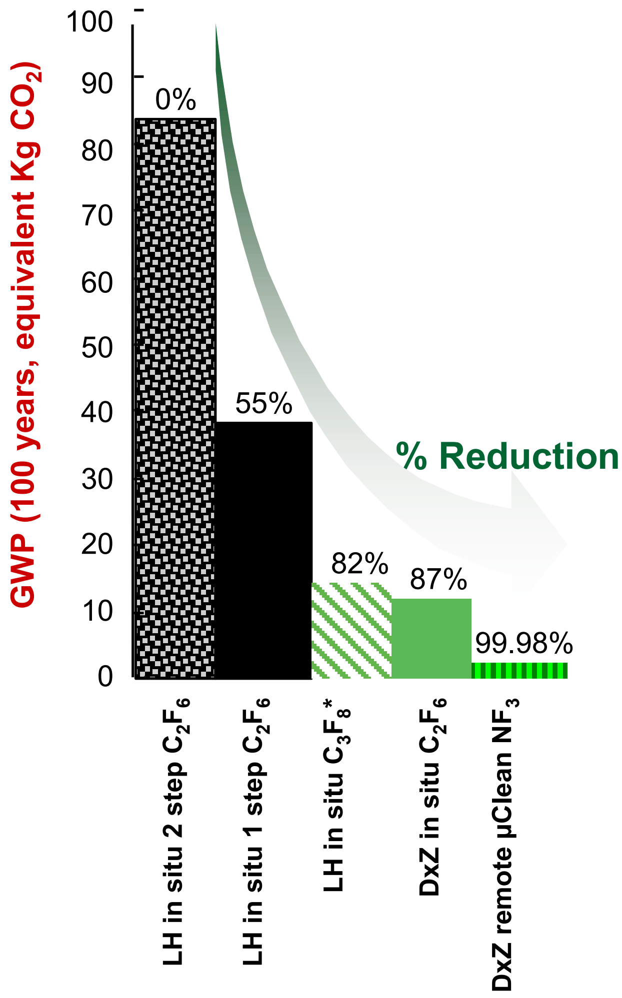
In-Situ Clean versus *Remote* Clean™



- *In situ* Clean
  - Results in corrosion of chamber components at high power density.
  - Limited etch rate, longer clean time.
  - Limited PFC Utilization Removal Efficiency (URE = 20-70%)
- *Remote* Clean™
  - Near complete Utilization Removal Efficiency of NF_3 (URE = 99%)
  - High etch rate (20-60% reduction of clean time)
  - No ion bombardment in main chamber("soft" clean)
  - Increased Mean Wafer Between Clean (3000 --> 5000 wafers)
  - Global Warming emissions reduced by one to two order of magnitude (Carbon equivalent).

Results

GWP Equivalent Kg CO_2 Per Micron of TEOS Oxide Film

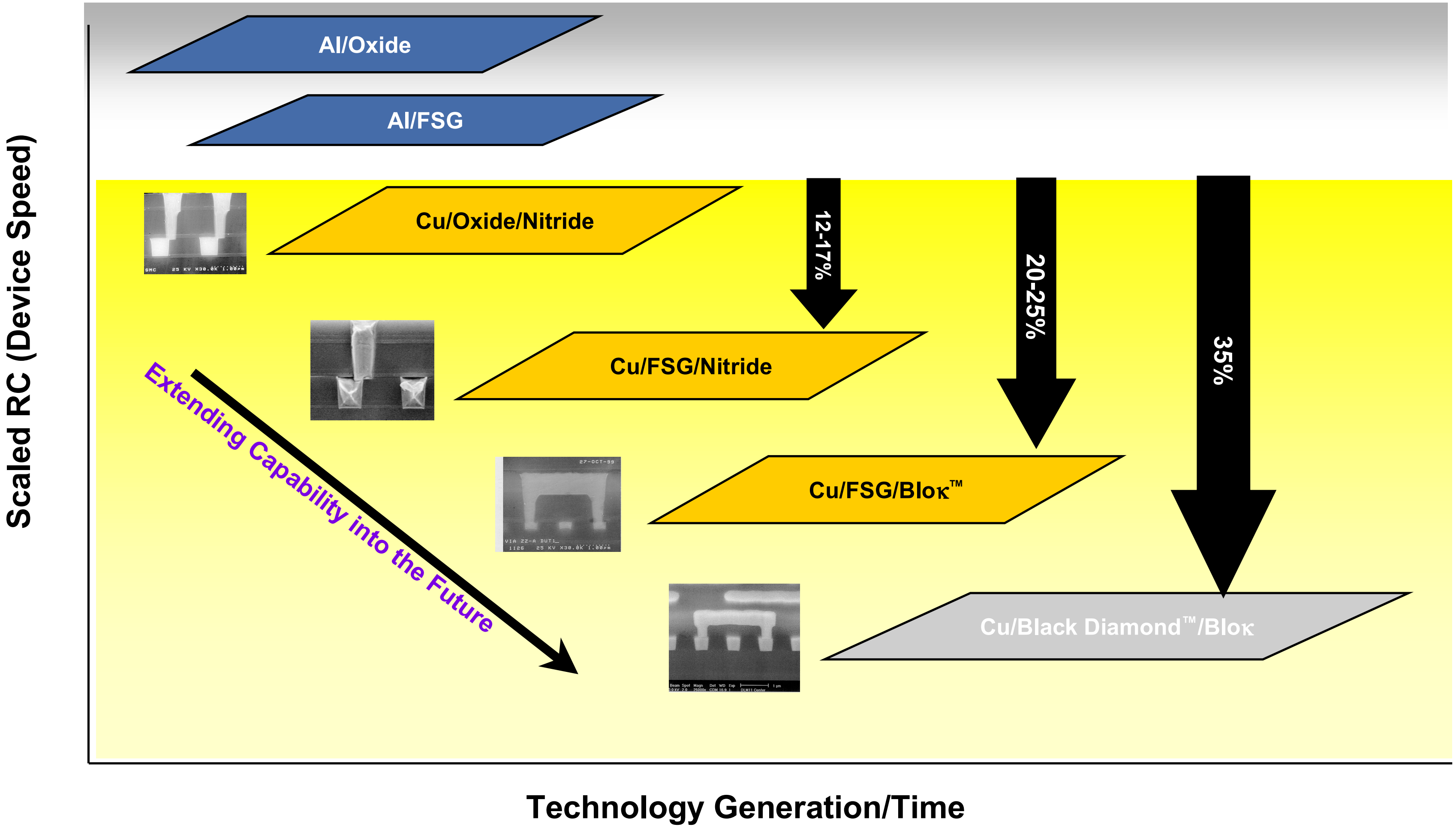


* Based on initial investigation

Awards

- The EPA honored Applied Materials with the 1999 Climate Protection Award for its Remote Clean™
- The Remote Clean™ received the prestigious R&D 100 Award sponsored by R&D Magazine
- Applied Materials Taiwan received the National Business Environmental Protection Award given by Taiwanese government.

Summary



Scaled RC (Device Speed)

Al/Oxide

Al/FSG

Cu/Oxide/Nitride

Cu/FSG/Nitride

Cu/FSG/Bloκ™

Cu/Black Diamond™/Bloκ

12-17%

20-25%

35%

Extending Capability into the Future

Technology Generation/Time