Materials for Next Generation Lithography and Advanced Back-End-of-Line Interconnects – An Overview

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Outline

• Introduction
  – Technology & Business Directions

• MOSAIC (BEOL) Program
  – Cu, low κ, CMP, cleaning, integration

• Next Generation Lithography Program
  – 157nm, EPL, EUV, ...

$ MM

PWB - Connectors - Semiconductor Packaging
Microelectronics
Circuit Delay and Interconnect Materials

- The diagram below illustrates the problem of “RC time delay” - the physical effect which dominates as metal interconnects crowd closer together
- **Cu interconnects** and **Low-κ dielectrics** are required for smaller, faster devices

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**Graph Description:**

- **Gate Delay**
- **Interconnect Delay, Al/SiO₂**
- **Sum of Delays, Al/SiO₂**
- **Interconnect Delay, Cu/Low κ**
- **Sum of Delays, Cu/Low κ**

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Why Copper and Low \( \kappa \) Dielectrics?

- Processing speed is determined by the circuit delay
- Circuit delay \( (\tau) \) is the inverse of resistance \( (R) \) x capacitance \( (C) \)
  \[ \tau = \frac{1}{RC} \]
- Minimizing delay increases speed:
  - Decrease metal conductor resistivity \( (\rho) \) to decrease resistance:
    - Aluminum \( \rightarrow \) Copper
  - Decrease insulator dielectric constant \( (\kappa) \) to decrease capacitance
    - Silica (glass) \( \rightarrow \) low \( \kappa \) dielectrics

Moving to Cu/low \( \kappa \) increases speed \( \sim 3x \) over Al/SiO\(_2\)
Cu/low \( \kappa \) technology enables the production of chips at 0.13 \( \mu \)m feature sizes and below
The Concept of MOSAIC

MOSAIC
PROCESS INTEGRATION

PHOTORESISTS
DUV, 193 nm,
Next Generation Lithography

ELECTROPLATING
Copper,
Alternate Metals/Alloys

PROCESS CONTROL
Bath Analyzer

SEED/BARRIER LAYERS
Solution,
MOCVD (UP Chem)

ANCILLARIES
Developers, Removers,
Rinases, Other

WASTE RECOVERY
of Shipley Products

ILD
Full Range of k,
Photo-ILD

CMP
(Rodel)
Copper Electroplating: Bottom-Up Fill

- Selection of additives in plating formulation determines conformal vs. “bottom-up gapfilling
Fabrication of Inlaid Copper Wiring by Electroplating

- 0.15µm dense trenches
- 0.11µm isolated trench
- 0.12µm x 1.2µm (10:1 AR) trenches
- 0.22µm dense vias

- High aspect ratio (10:1), 100nm structures filled using current generation EP Cu products
Effect of Additives on Cu Electrodeposition

- FIB microscopy shows void-free gapfill @ [Additive] ≥ 50% of nominal level

- Modulation of [additive] in bath increases time for self-annealing to reach minimum resistivity

Data obtained in collaboration with IMEC
Waveform Modification for Improved Uniformity

DC Waveform

Reverse Pulse Waveform

• 0.20µm trenches, AR 4:1, 250Å Ta barrier, 1000Å Cu seed, 1µm EP Cu

• Bottom-up fill mechanism leads to “bump” plating over dense features with standard POR
• Plating recipe incorporating a Periodic Pulse Reverse waveform polishes back high current density regions, improves within-die uniformity
• Improved uniformity is directly correlated with improved CMP performance
Seed Layer Enhancement

- Discontinuous seed layer (as-deposited, or due to etching of thinly plated areas) leads to patchy initiation of plating, resulting in poor gapfill (voids).

- Seed Layer enhancement deposits additional Cu on discontinuous base layer and makes adjacent regions of Cu seed contiguous. Uniform initiation of plating eliminates voids.

Courtesy of Semitool
Cu Electroplating: Challenges for the Future

- Seed and barrier layer chemistries for 100nm node and below
  - Repair, make thinner, eliminate

- Co-optimization of EP Cu and CMP chemistries
  - Improved planarization and defectivity across 300mm

- Development of specialty Cu formulations for improved device electrical performance
Nanoparticle Fabrication for Porous ILDs

- Fabrication of structurally-tailored polymer particles is a core competency of R&H
- Particles are made in sizes ranging from µm to nm
- Particle dispersions are made in high purity and at scale
Porogen Approach to Formation of Nanoporous ILD Materials

1. Spin coat solution
2. Hot plate cure 90°C - 250°C
3. Furnace anneal 400 - 425°C

Ammonia Free Process
Polymeric Porogen Particles

- Transmission electron micrograph of a thin section of polymeric porogen nanoparticles embedded in a silsesquioxane matrix
- Average size of particles in TEM is 20 nm
- Modification of polymerization conditions can produce particles of 1-5nm diameter with narrow size distribution
Porous Organosiloxane Films

- Incorporation of porogen particles into organosiloxane matrix, followed by thermal decomposition of the porogens produces nanoporous films.
- Dielectric constant and refractive index track porogen loading.
Porous Low $\kappa$ Dielectric Films from Polymer Nanoparticles

$\kappa = 2.3 - 2.4$

20% porous organosiloxane film

Average pore radius = 1.3 nm

$\kappa = 1.8 - 1.9$

50% porous organosiloxane film

Average pore radius = 4.8 nm

- Uniform pore formation equivalent to porogen particle size distribution
- Porogen compatibility with both inorganic (Si-O) and organic matrix materials

Standard processing - 200 mm wafer:
Spin speed 3000 rpm
Hot plate cure 90°C/60sec & 150°C/60sec
RTP furnace cure 425°C/1 hr
Photoresist Patterning on Nanoporous ILD

Initial results:
(lithography not optimized!)
- Good pattern formation
- Interfacial profile control
- Adhesion

Process Conditions
- Substrate: 200 mm 1-20 Ω silicon <100>
- ILD Layer: 8,000 Å porous organosiloxane
- Porosity: 30% porous (Est. k= 2.1)
- ARC: none
- Resist: UV210-0.6, 5766 Å
- Soft BaKe: 130º C/60s
- Expose: ASML5500/300 (0.63NA, 0.850σo, 0.425 σi)
- Post Exposure Bake: 130º C/60s
- Develop: MF CD-26, 60 sec. single puddle
Low $\kappa$ Dielectric: Challenges for the Future

- Demonstration of viable nanoporous organic ILD
- Highly porous ($\kappa < 2.0$) ILD capable of withstanding standard CMP and integration processing
- Ultra-low $\kappa$ ILD ($\kappa < 1.7$) and beyond??
- Photoimageable ILD
Shipley- SVC

- Environmentally-friendly, high performance ancillary chemistries for semiconductor applications
  - Photoresist strippers
  - Edge bead removers for photoresist, ILD
  - Post-etch residue removers
  - Post-CMP cleaners
  - Cu bevel etch

- Aqueous-based chemistries
- Biodegradable and non-toxic
- Non-corrosive to Ti, W, Cu, Al alloys
- No: catechol, hydroxylamine, or SARA Title 3 chemicals
- Ultra high purity: low ppb level mobile ionic contamination
PRX-417 Post-Etch Residue Remover

- PRX-417 completely removes polymers on the bottom and inner walls of high-aspect ratio vias without metal undercut

Before Clean

<table>
<thead>
<tr>
<th>Material</th>
<th>Before Clean</th>
<th>PRX-417, Static Bath, 5-10min., 23°C DI Rinse, 5 min</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEOS</td>
<td></td>
<td>Via CD = 300 nm, Aspect Ratio = 3:1</td>
</tr>
<tr>
<td>TiN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Al-Si-Cu</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti</td>
<td></td>
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<tr>
<td>CVD Doped Oxide</td>
<td></td>
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</tr>
<tr>
<td>SiN</td>
<td></td>
<td></td>
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<tr>
<td>PECVD Undoped Oxide</td>
<td></td>
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</tbody>
</table>

Via CD = 400 nm
PRX-417 Post-Etch Residue Remover

- PRX-417 can remove low-k dielectric sidewall polymers without damaging or degrading low-k films or properties.

Before Clean

CVD Oxide
SiN
Cu/Low \( \kappa \)

Clean removal of sidewall polymer; no Cu corrosion

PRX-417, Static Bath, 15min., 23°C
DI Rinse, 5 min

Compatibility with organic ILD (FLARE)

15 min clean
5 min clean
No clean

Note: all copper has been etched away

Hydroxylamine Formula
• **Short-term**: Non-hydroxylamine based photoresist removal and post-etch cleaning
• **Effective** aqueous or solventless cleaning chemistries
• Cleaners, EBRs, and related ancillaries for Cu-low $\kappa$ Dual Damascene processing
  – Integration with complex stacks of multiple new materials
• Post-etch, post-CMP particle removal at 100nm node and below
Copper Damascene Integration

- Oxide/nitride stack
- AR3 coating
- UV210 photoresist coating
- ASML 5500/300 patterning
- LDD26 developer
- Low-κ porous ILD
- AR7, ViPR

- AR3 etch
- Oxide etch
- PERR

- Photoresist strip
- Post-etch strip
- SVCstripers
Copper Damascene Integration

- PVD Ta or TaN barrier
- PVD copper seed

- Seed layer chemistries
  - EP Cu
  - Waveform recipe

- Copper CMP
- Barrier CMP
- Post-CMP cleaners