Use of Air-Gaps to Lower IC Interconnect Capacitance

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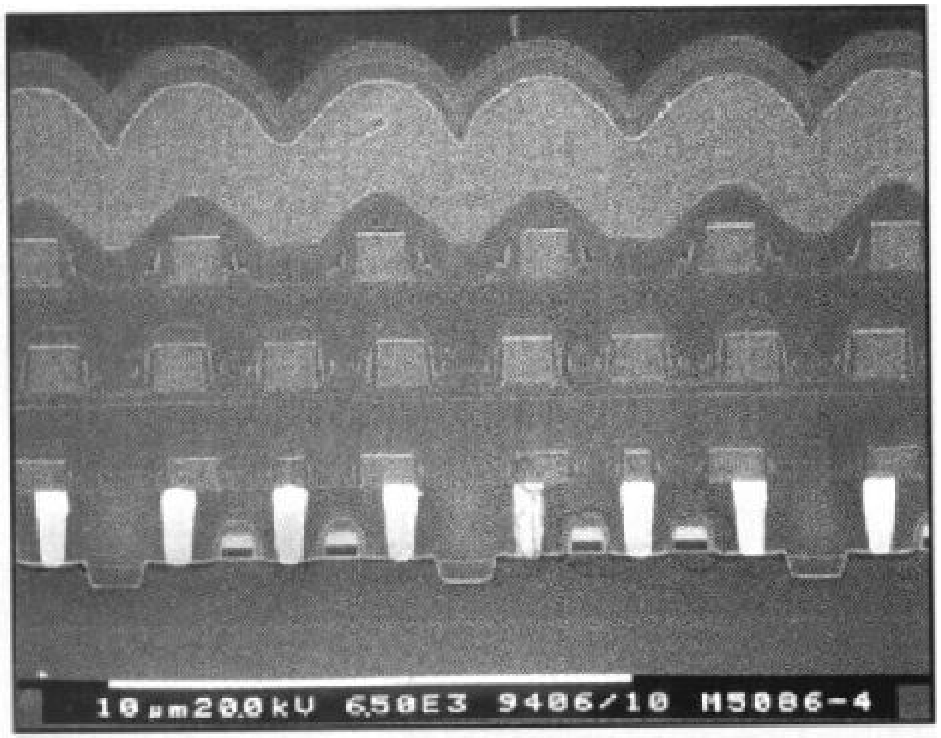
Outline

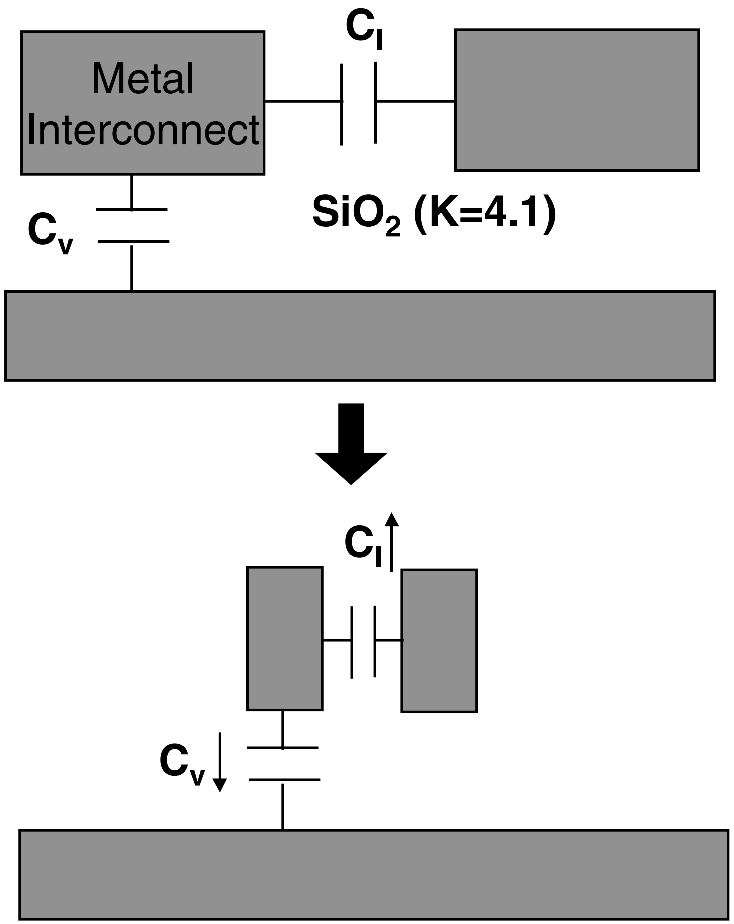
- Background and Motivation
- Ideal Air-Gap Structures
- Air-gap Processing and Integration
- Electrical Performance
- Electrical and Thermal Reliability
- Electromigration Reliability
- Summary

Cross Section of IC Chip

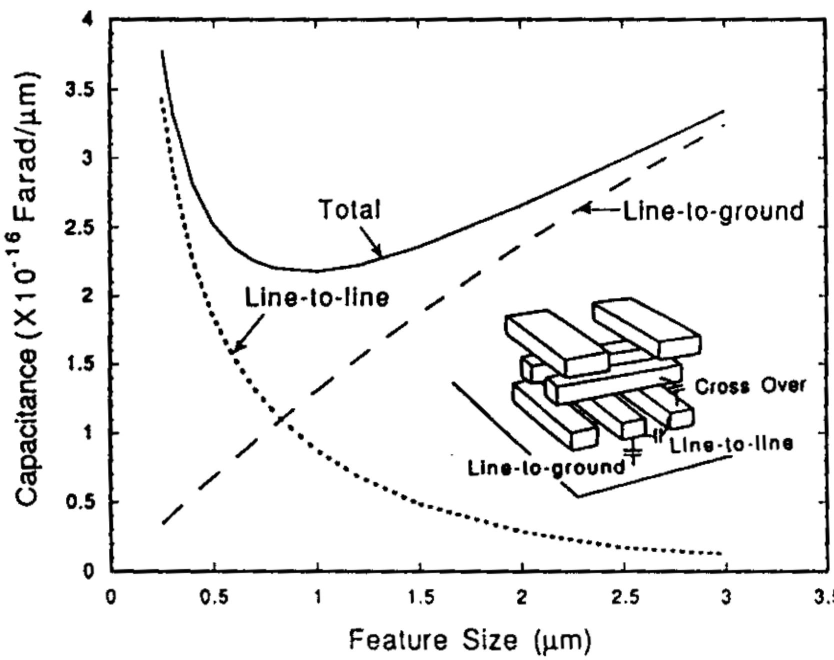


- Modern IC's use multiple levels of metal interconnects to electrically connect transistors

Interconnect Capacitance



$$C = K\varepsilon_0 \frac{A}{d}$$



S. Jeng, R.H. Havemann, and M. Chang, *Mat. Res. Soc. Symp. Proc.*, 337, 1994, p.25.

Lower Capacitance with Low-K Materials

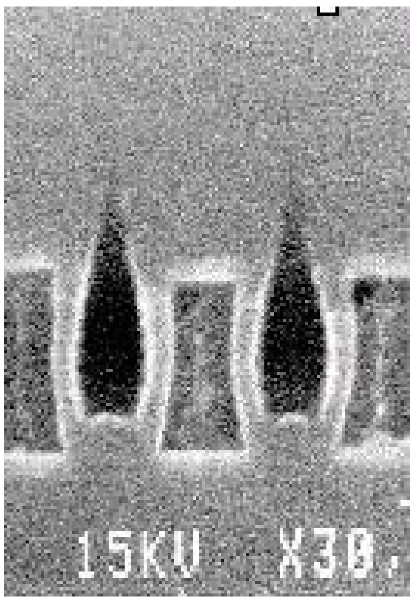
Material	Technique	Trade Name	Company	k
SiO_2	CVD			4.0-4.3
F_xSiO_y	CVD			3.4-4.1
HSQ	Spin-on	Flowable Oxide	Dow Corning Allied Signal	2.9
Nanoporous Si	Spin-on	Nanoglass	Allied Signal	1.3-2.5
F-polyimide	Spin-on			2.6-2.9
Poly(arylene) ether	Spin-on	FLARE VELOX	Allied Signal Schumacher	2.6-2.8
Parylene AF4	CVD		Novellus Watkins Johnson	2.5
Aromatic hydrocarbon	Spin-on	SiLK	Dow	2.65
PTFE	Spin-on	Speedfilm	Gore	1.9
DVS-BCB	Spin-on		Dow	2.65
Hybrid SQ’s	Spin-on	MSQ	Dow Corning	<3.0
Amorphous FC, HFC	CVD	FLAC, F-DLC, CFx	IBM, NEC Novellus, HP, TEL	1.9-3.3
Amorphous SiOCH	CVD	Corral	Novellus	2.7
Amorphous SiOCH	CVD	Black Diamond	Applied Materials	2.7
vacuum				1.0

Table courtesy of Professor Karen Gleason at MIT

Low-K Material Issues

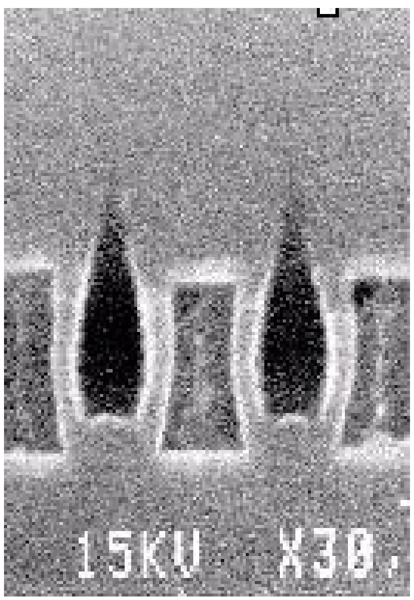
- Mechanical strength
- Dimensional stability
- Thermal stability
- Ease of pattern and etch
- Thermal conductivity
- CMP compatibility
- Moisture Absorption
- Complexity of integration

Air-Gaps: Historical Perspective



- Often referred to as dielectric voids and/or "keyholes."
- Semiconductor industry has traditionally tried to eliminate air-gaps: spin-on-glass, dep-etch-dep, TEOS, HDP-CVD.
- Difficult to integrate into process: cannot control size and shape of air-gaps.
- Potential reliability problems: electromigration, poor thermal conductivity, trap particles.
- Anecdotal accounts of capacitance decrease due to unintentional air-gaps.

Why Air-Gaps?



- Dielectric constant, K, approaching 1.
- Reduces dominating line to line capacitance.
- Interlevel SiO_2 left intact.
- Simple integration.
- Compatible with scaling trends - air gaps easier to form with higher aspect ratios.

- Good vehicle to study tradeoffs between performance & reliability

Environmental Impact

- No new materials or precursors
  - SiH_4, O_2, Ar
  - can use current toolsets (PECVD, HDP-CVD)
  - do not need new etch or CMP processes
- Known environmental issues
  - chamber clean

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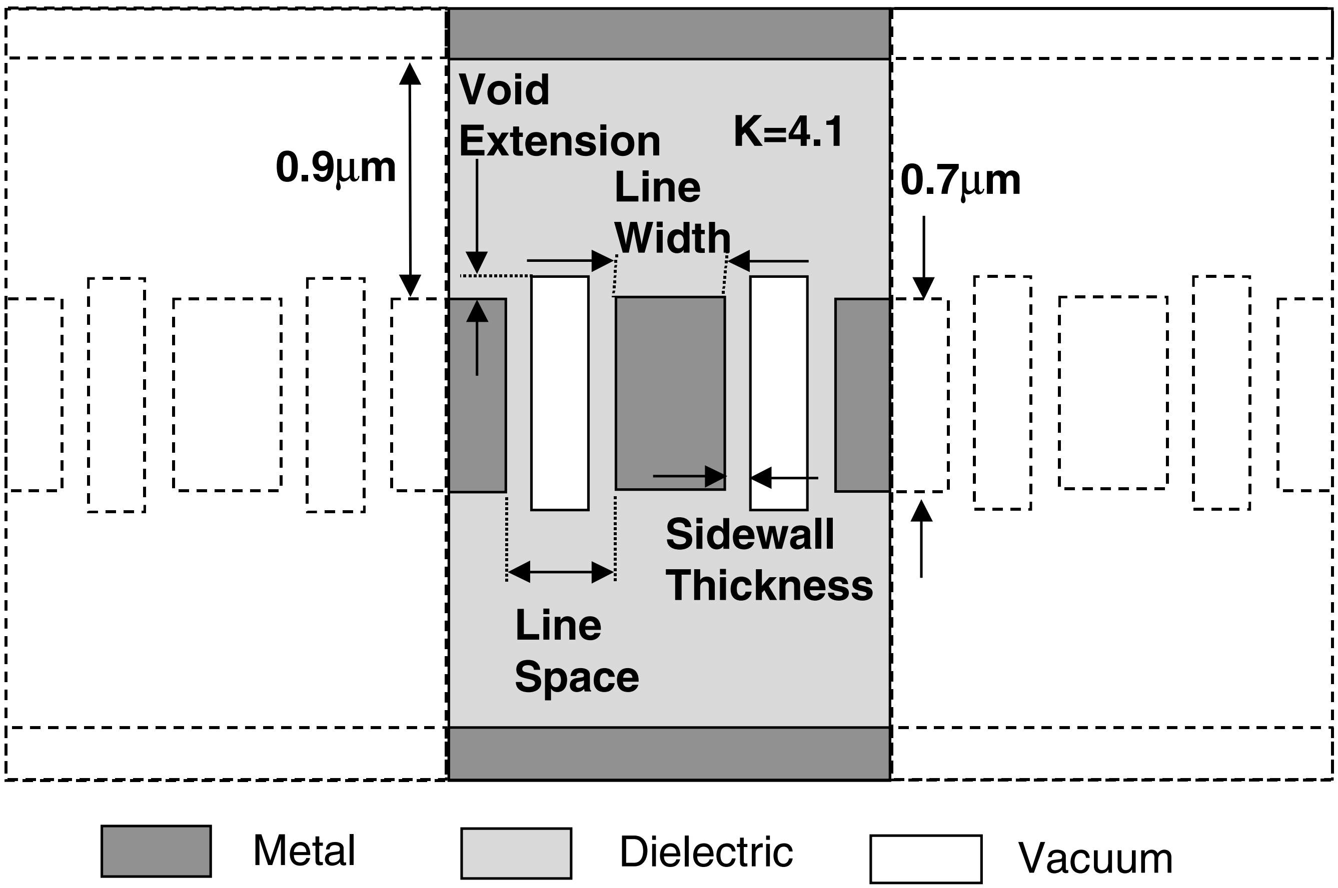
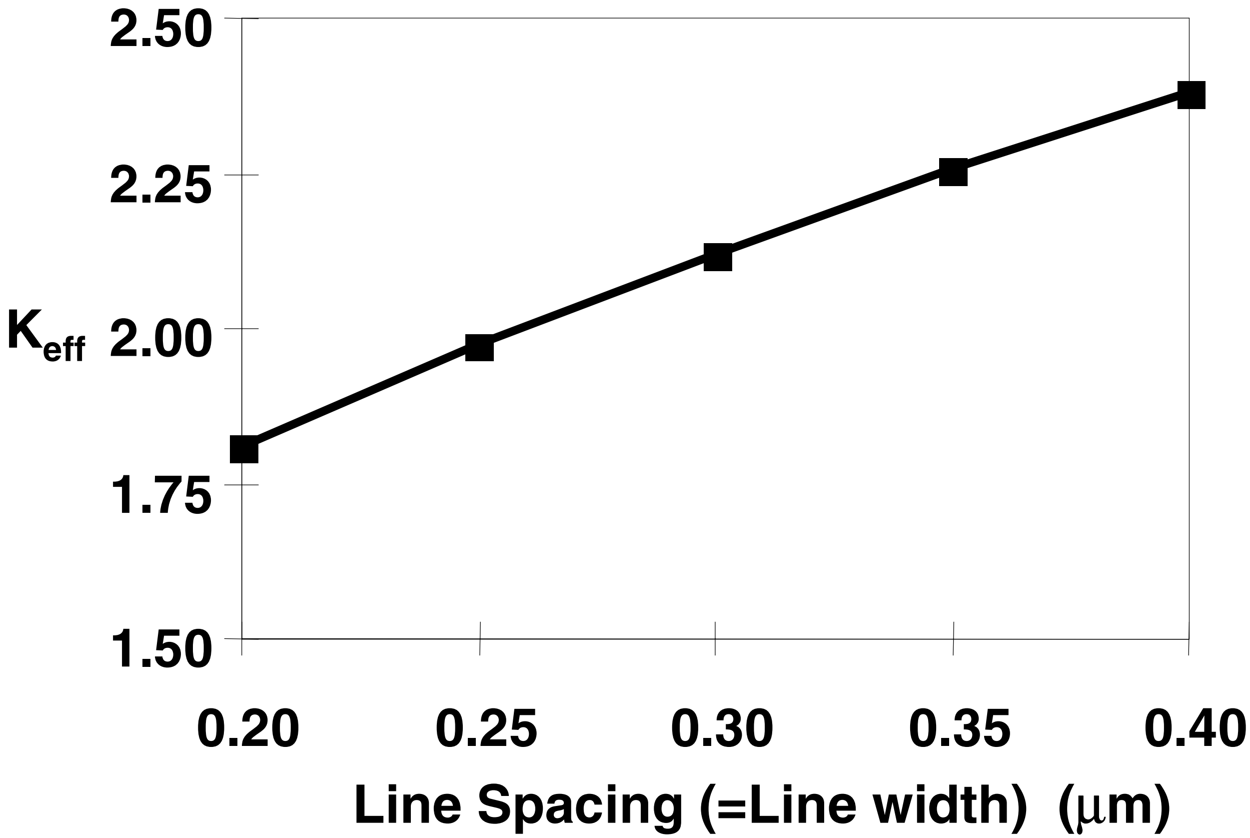
Raphael "Box" Air-Gap Simulation Geometry

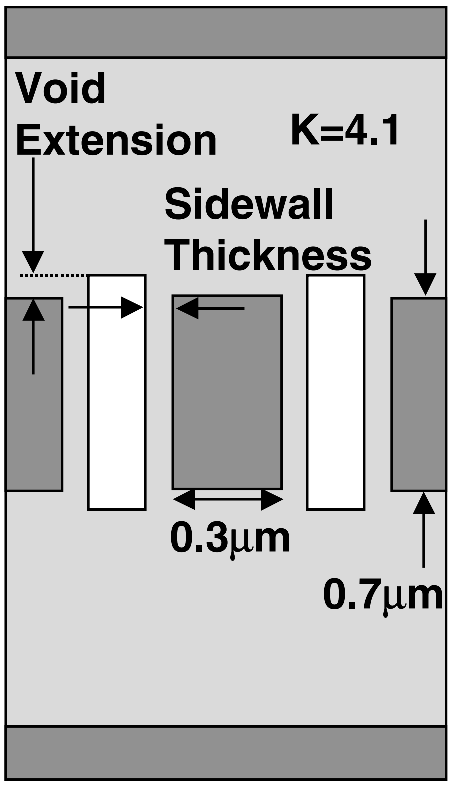


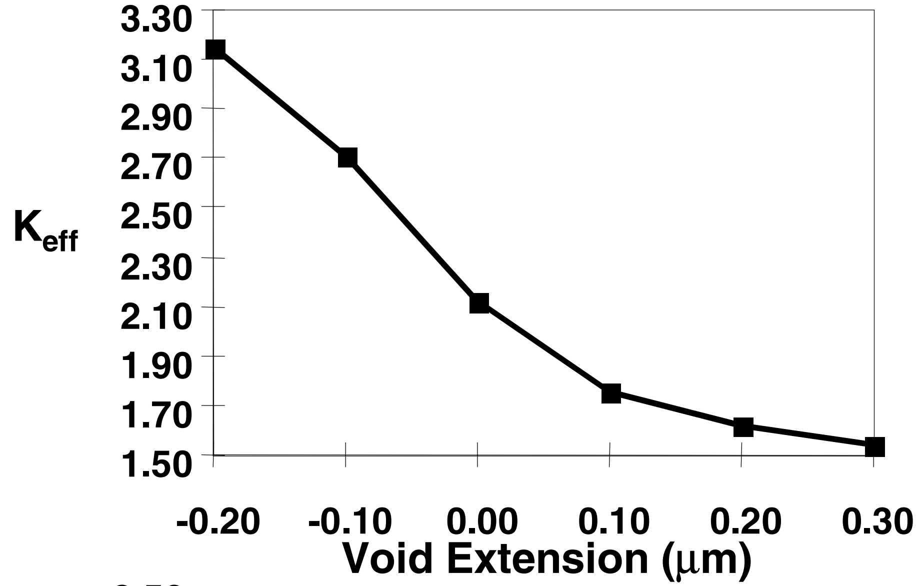
K_{eff} vs. Line Spacing

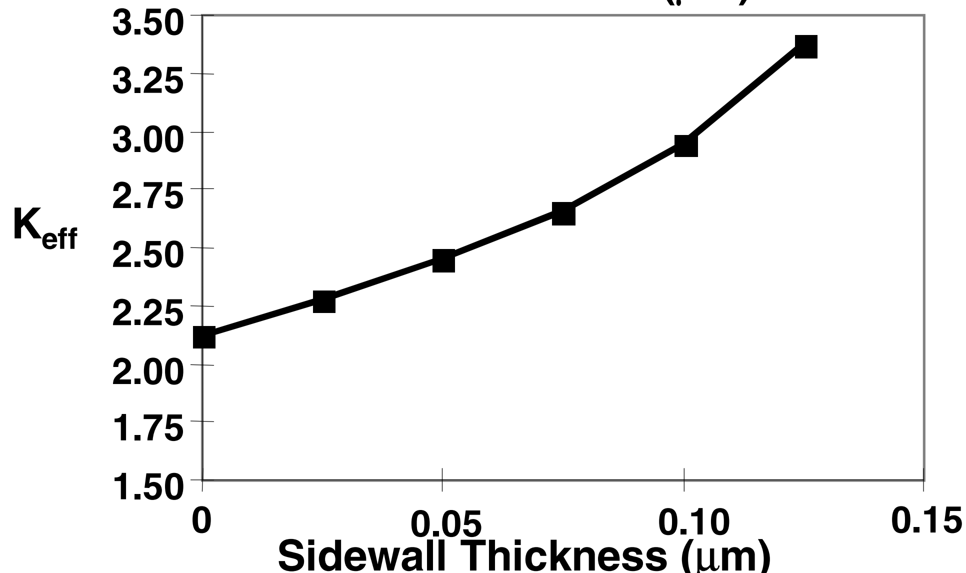
(Void Extension=0.0, Sidewall Thickness=0.0)



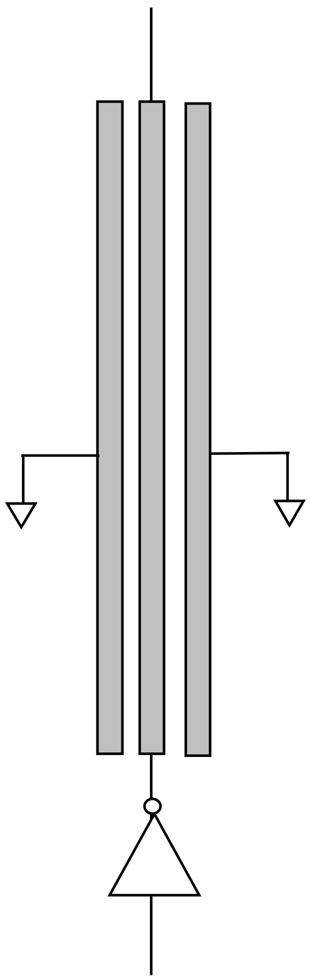
Dependence of K_{eff} Air-Gap Shape

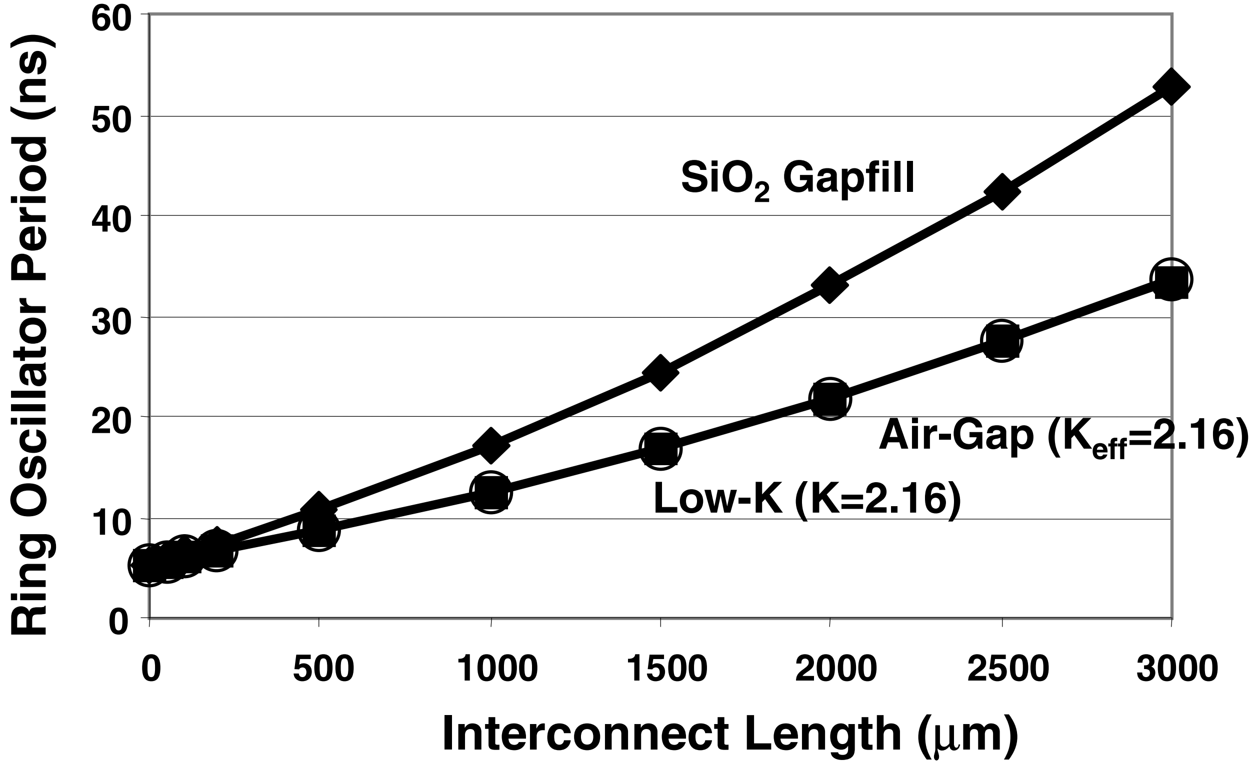




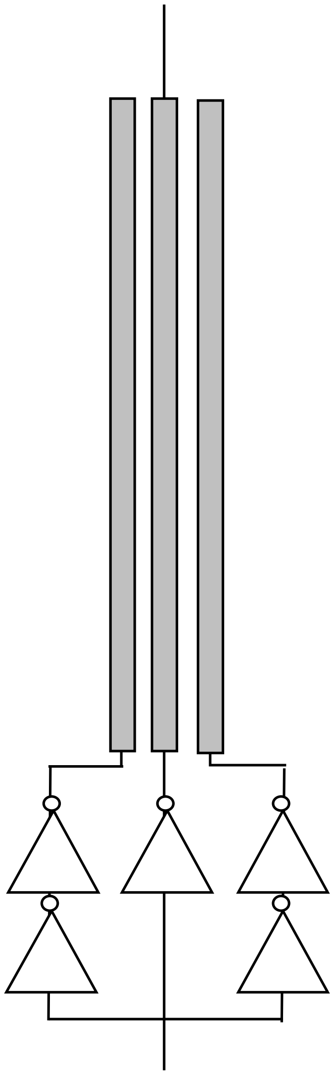


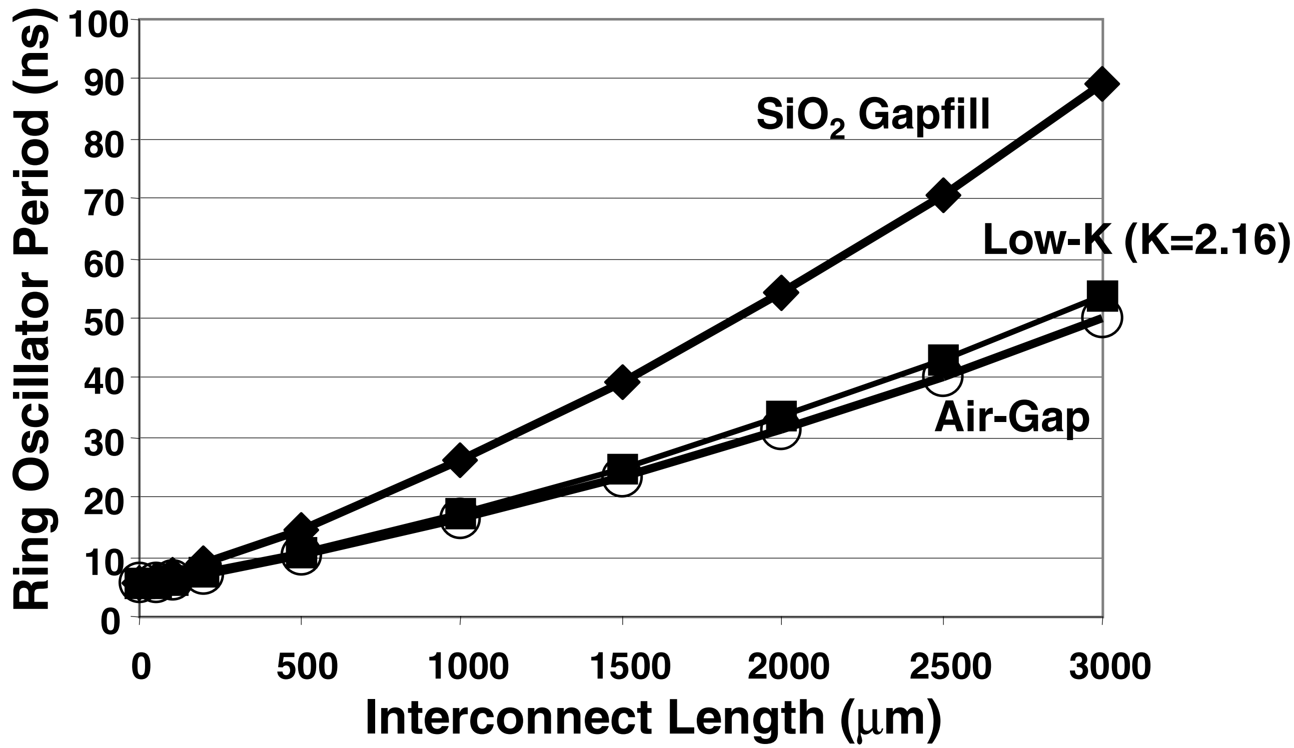
HSPICE Ring Oscillator Delay: Static Capacitance



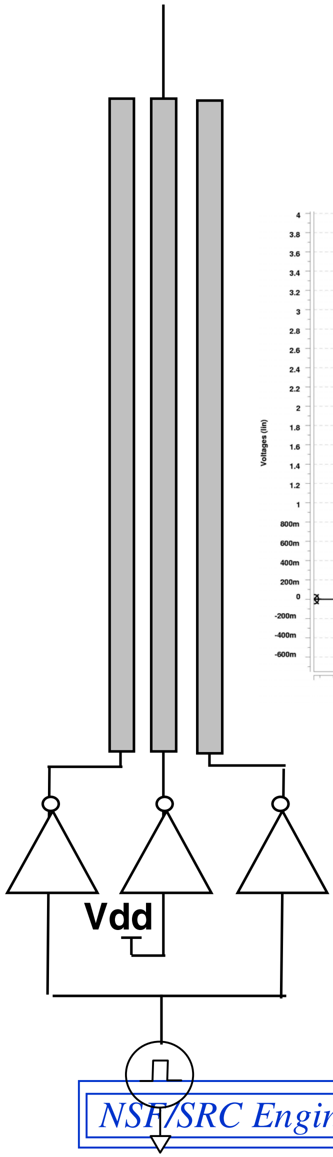


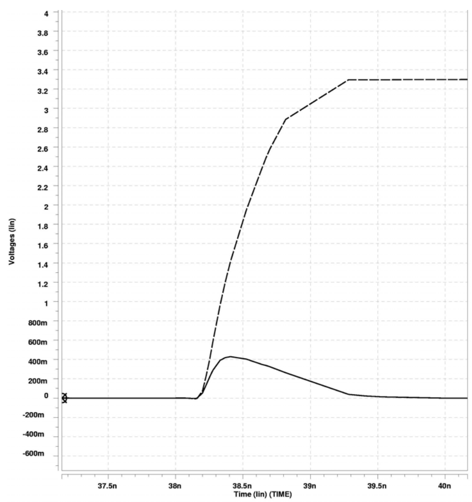
HSPICE Ring Oscillator Delay: Crosstalk Capacitance

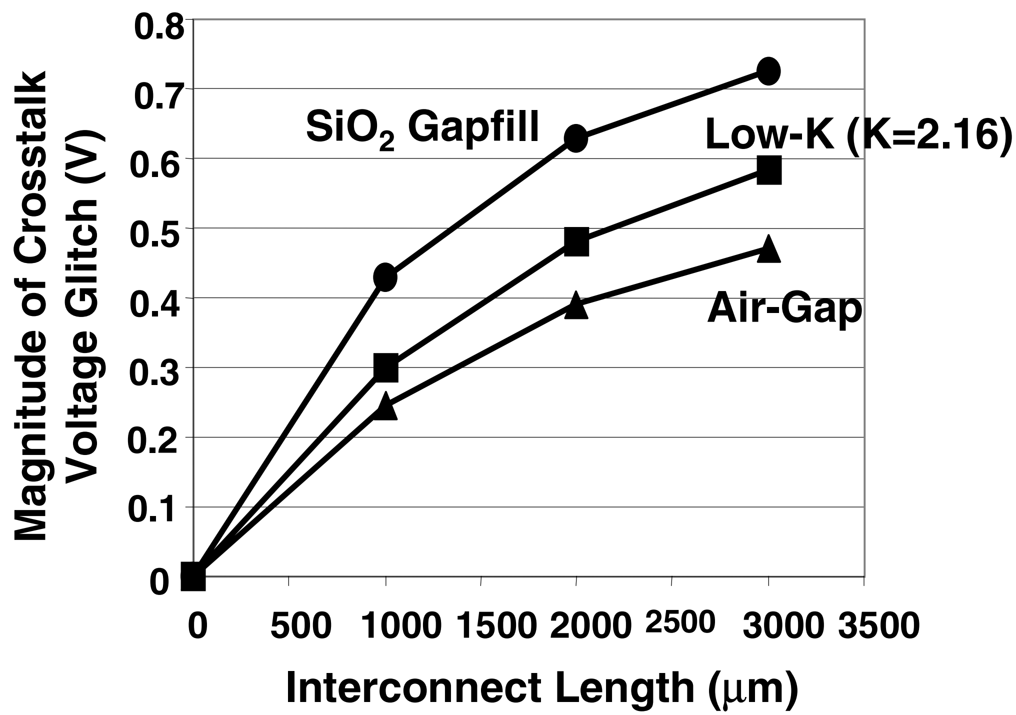




HSPICE Crosstalk Signal Integrity







Vdd=3.3V

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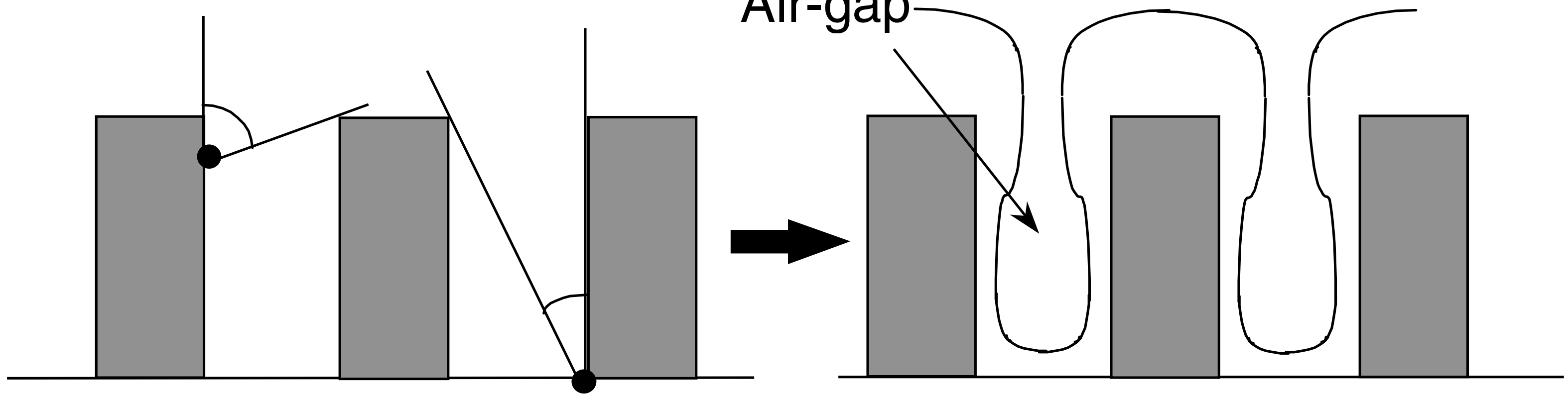
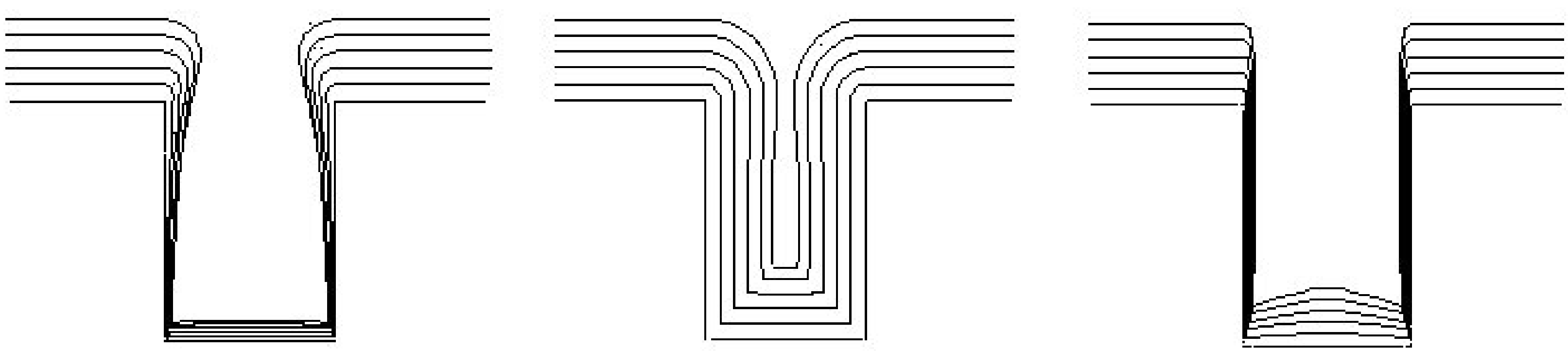
Air-Gap Formation

- Difference in view angle causes “breadloafing” during SiO_2 deposition.



- Greater “breadloafing” → Larger air-gaps

Deposition Topography



Isotropic Flux
High S_c

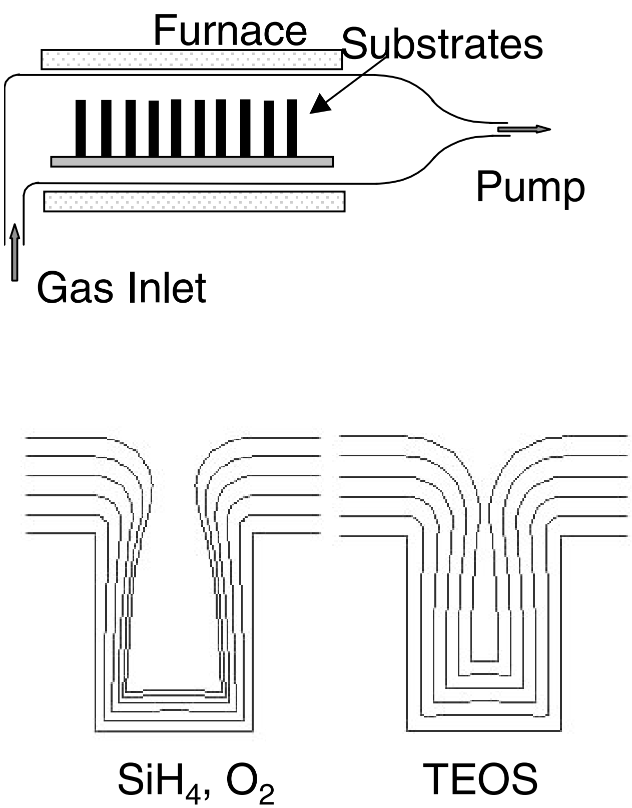
Isotropic Flux
Low S_c

Directional Flux
High S_c

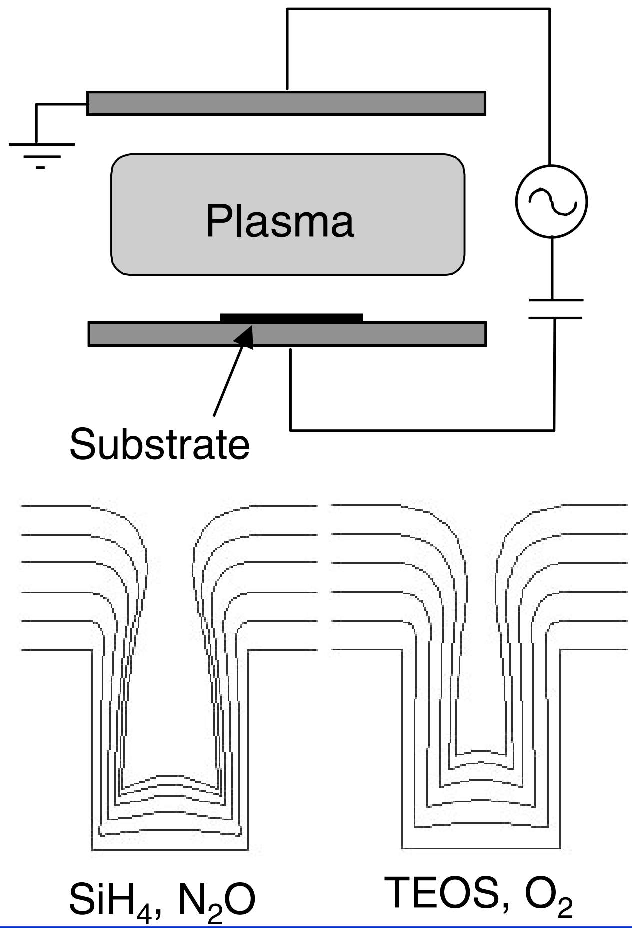
- Deposition topography depends on angular distribution of incident flux and sticking coefficient (S_c) of reactive species

SiO_2 Chemical Vapor Deposition (CVD) Technology

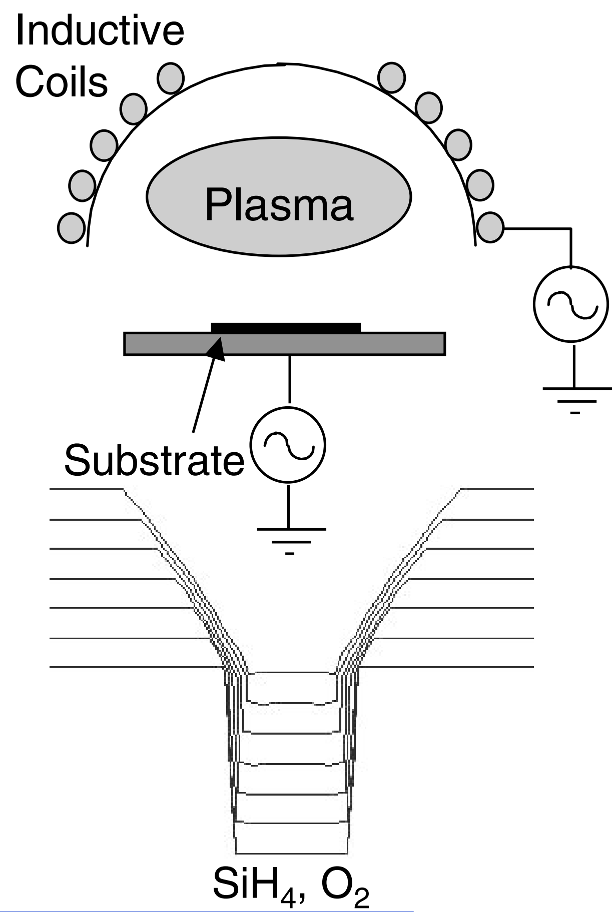
Low Pressure CVD



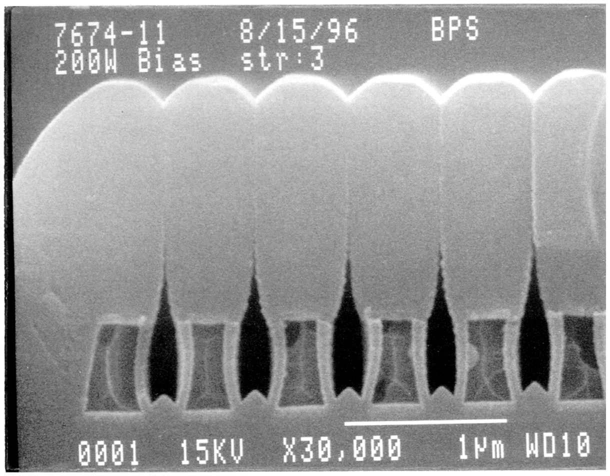
Plasma Enhanced CVD

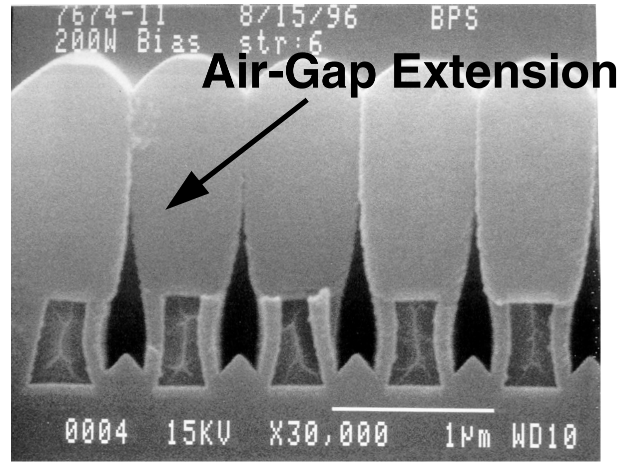


High Density Plasma CVD

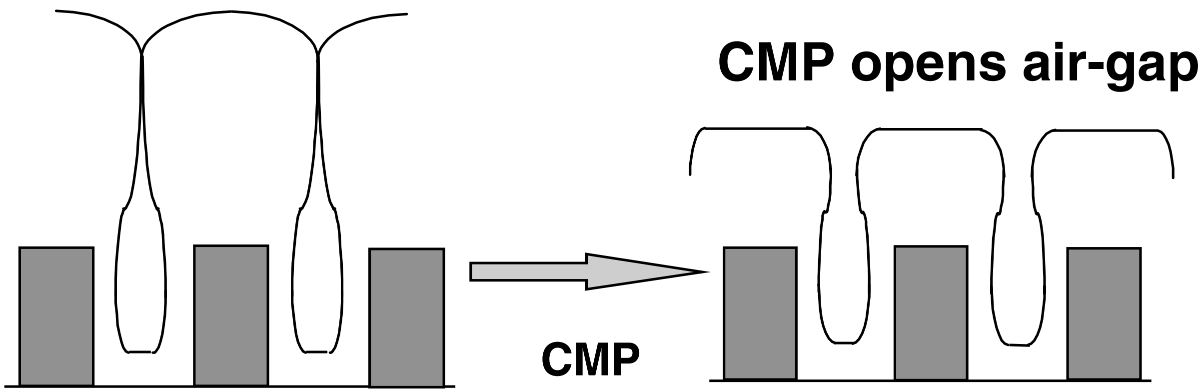


Integration Issue: Air-Gap Extension

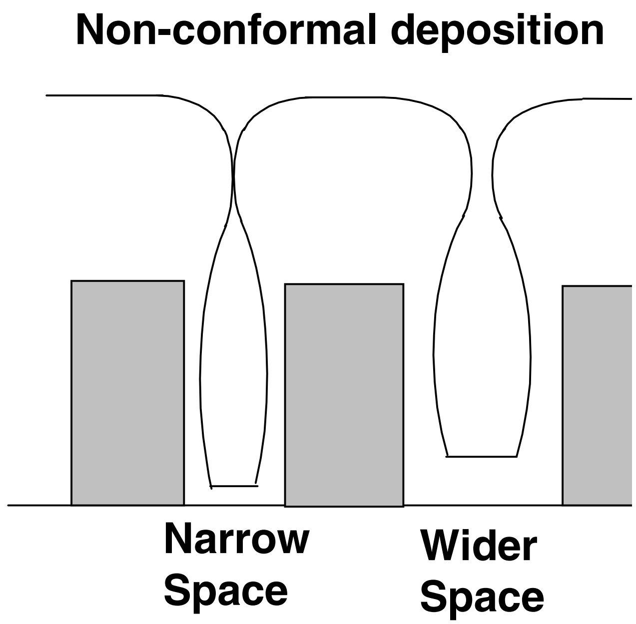


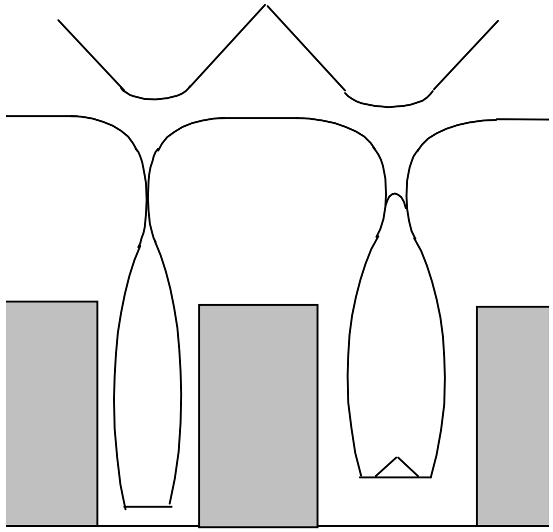


Line/Space = 0.3μm/0.3μm **Line/Space = 0.4μm/0.4μm**



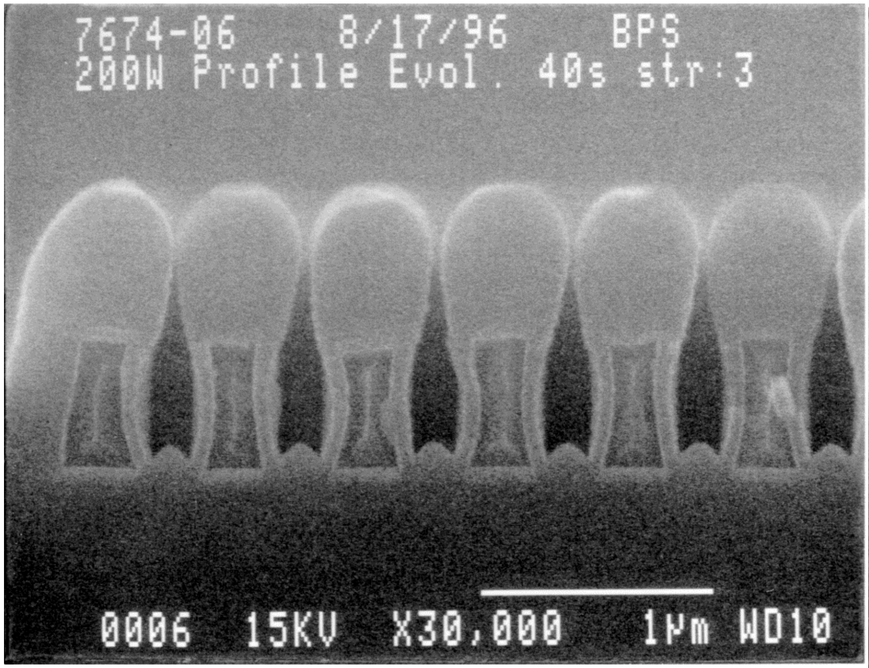
Controlling Air-Gap Extension



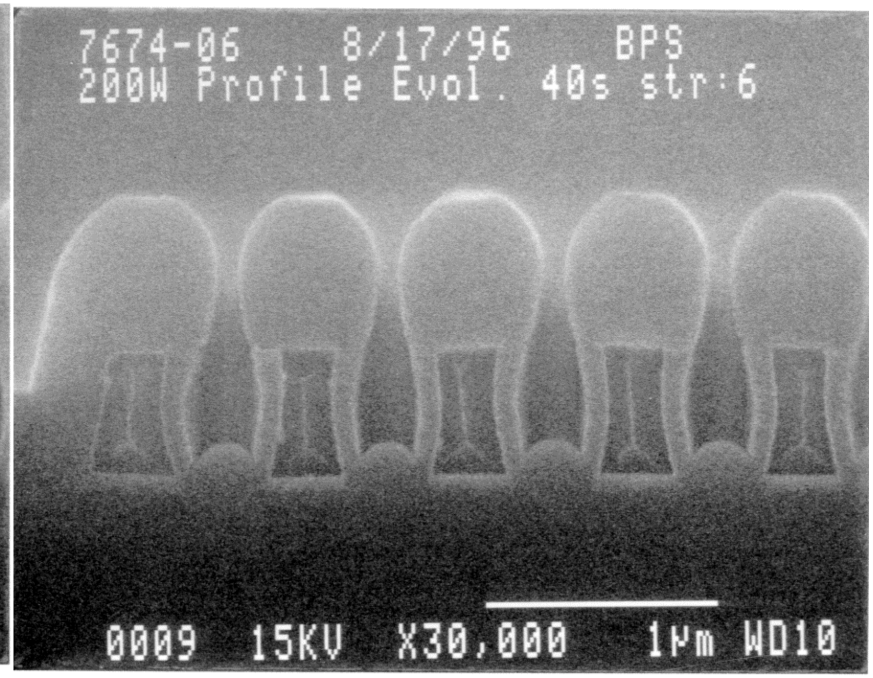


- First Step: Non-conformal deposition to form initial air-gap.
- Second Step: HDP-CVD to keep seam from forming, limit extent of air-gap above metal lines, and provide local planarization

Profile After First Step



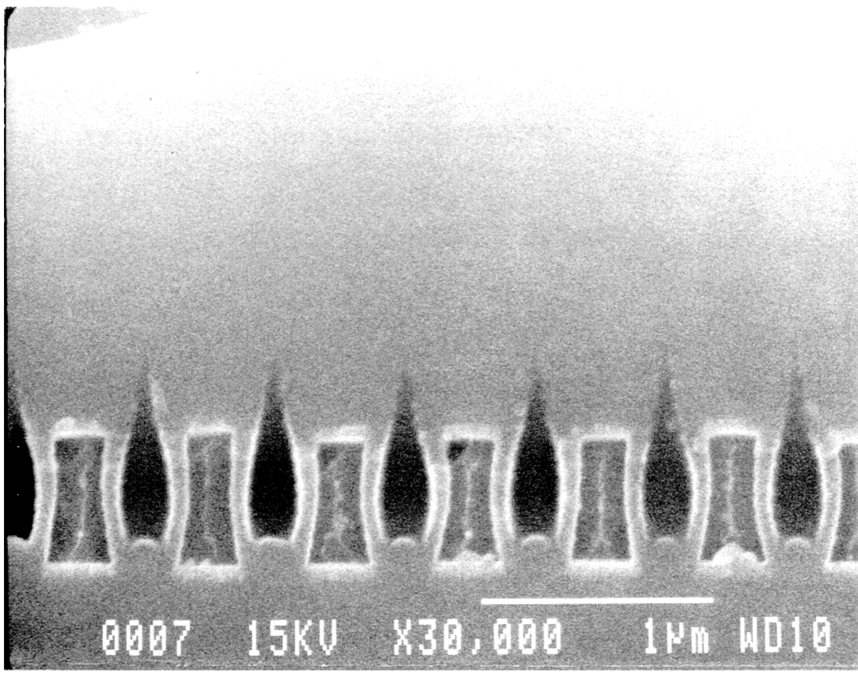
Line/Space = 0.3µm/0.3µm



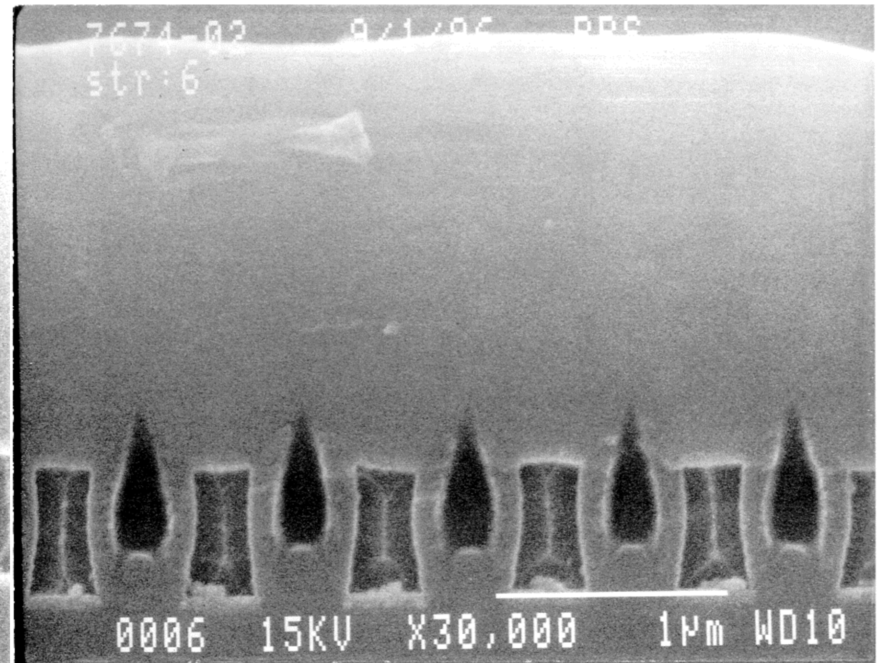
Line/Space = 0.4µm/0.4µm

- HDP-CVD: Modified recipe to produce non-conformal deposition
  - High Gas Flows
  - Low Substrate Bias

Profile After Second Step



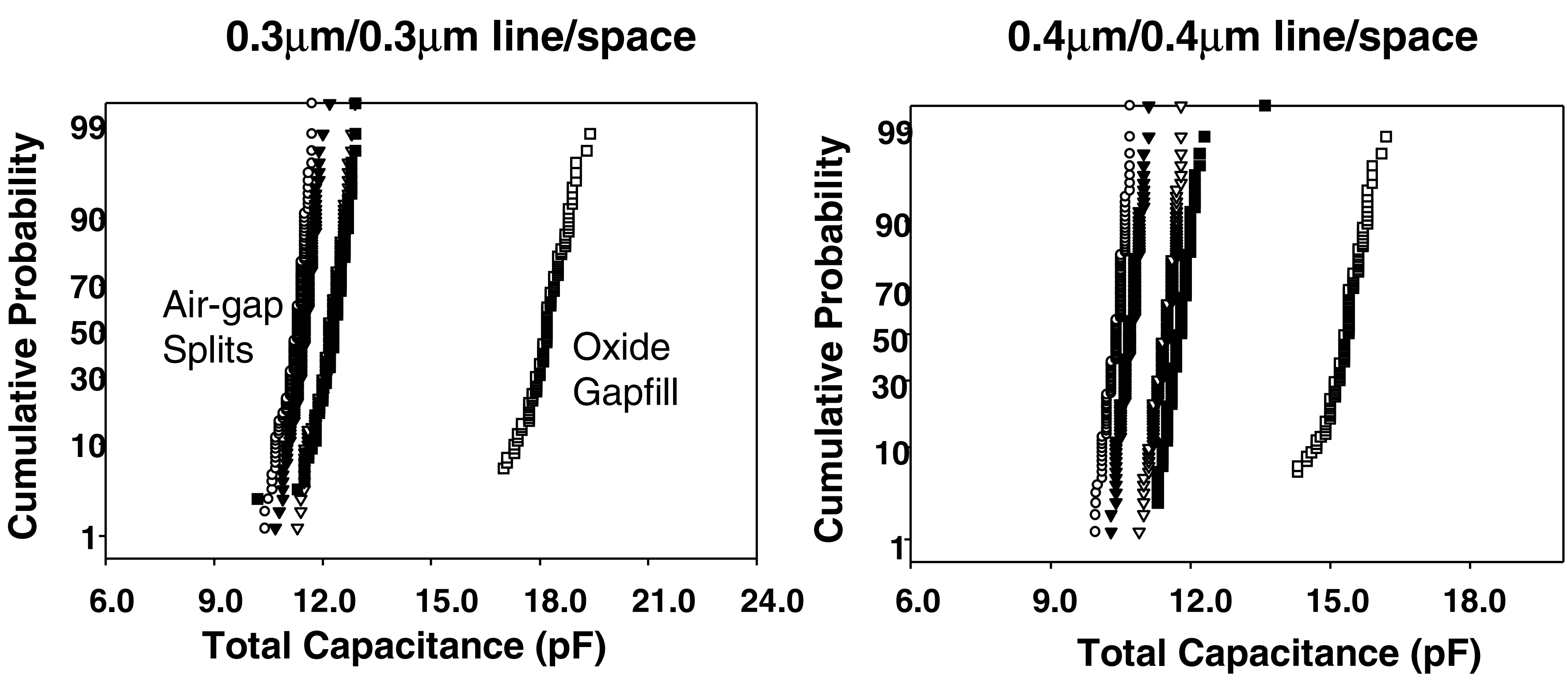
Line/Space = 0.3µm/0.3µm



Line/Space = 0.4µm/0.4µm

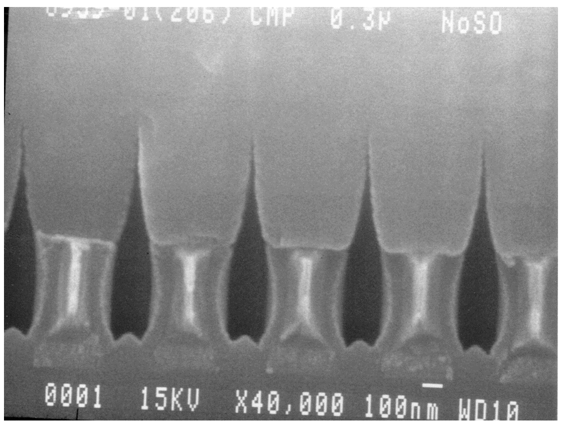
- HDP-CVD: optimized to prevent seam from forming, limit extent of void above metal lines, and provide local planarization

Experimental Capacitance Data

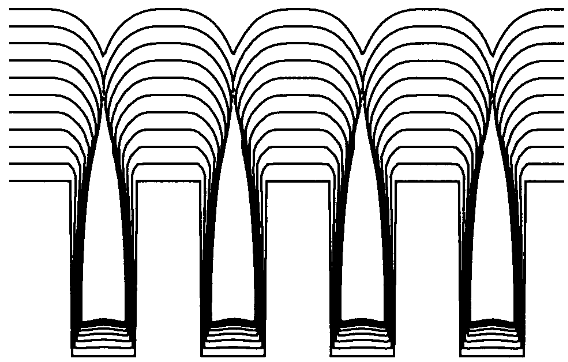


- ~ 33 to 40 % capacitance reduction from HDP oxide gapfill for 0.3μm lines/spaces

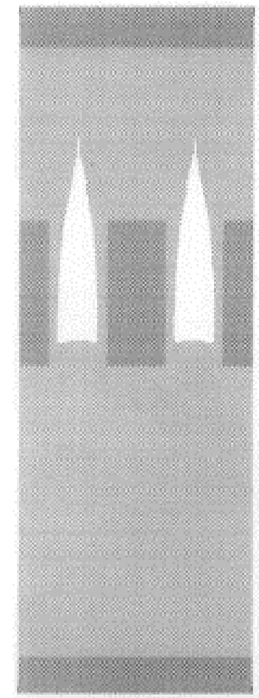
Profile and Capacitance Modeling of Experimental Results



Experimental Profile

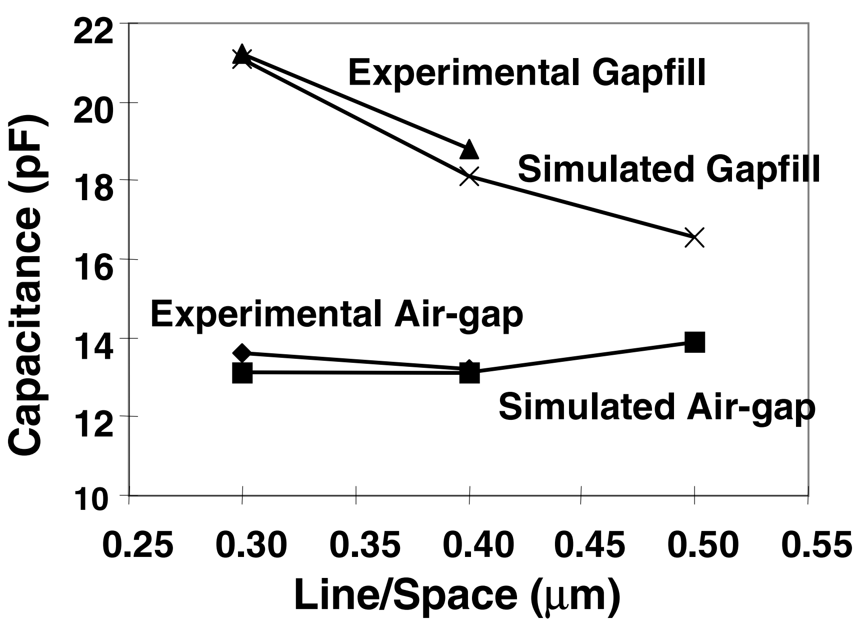


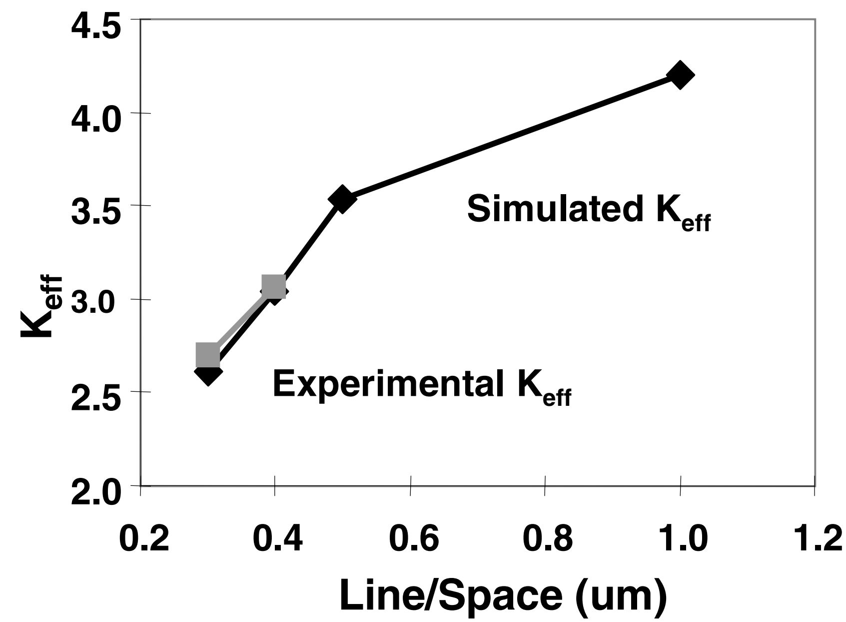
Deposition simulated using SPEEDIE



Capacitance calculation using TMA Raphael

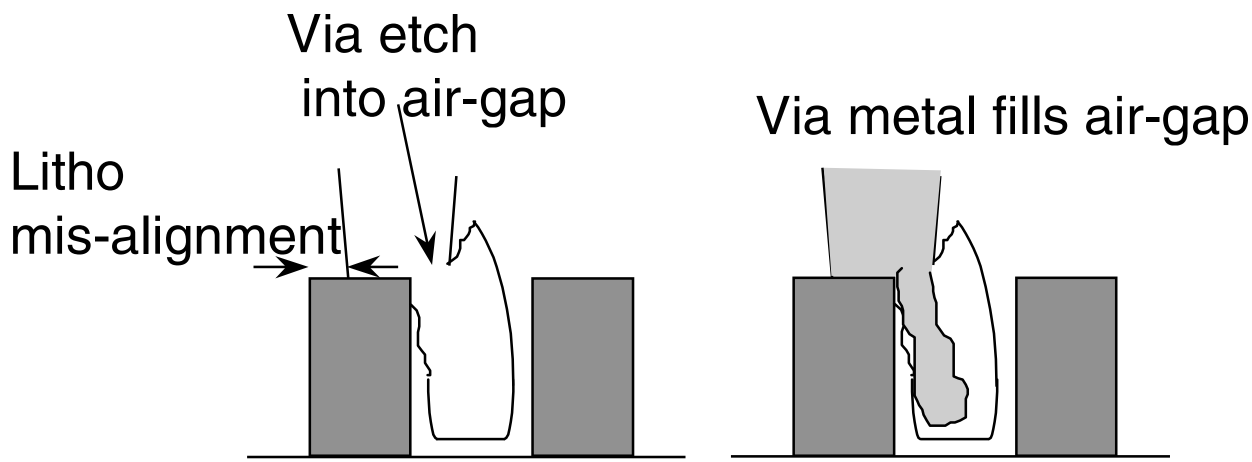
Capacitance vs. Feature Size

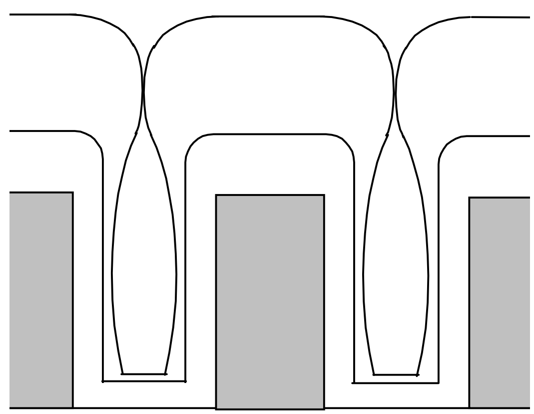




- K_{eff} of air-gap is geometry dependent

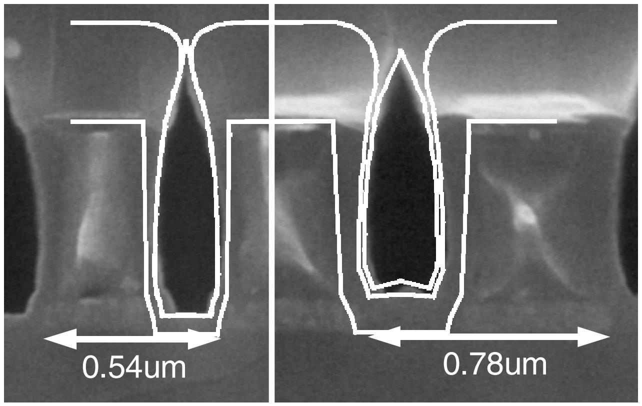
Integration Issue: Via Reliability



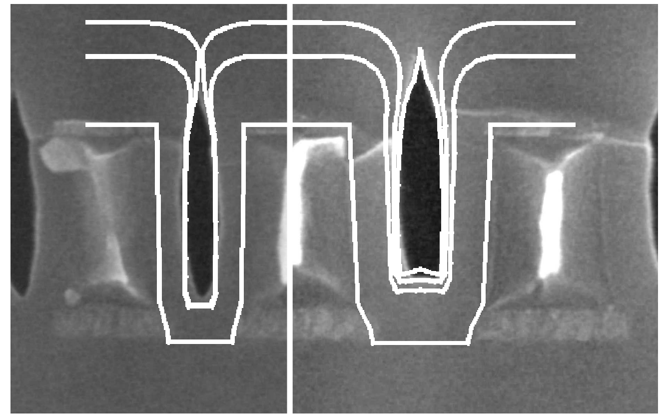


- First Step: Conformal deposition to control sidewall passivation thickness.
- Second Step: Non-conformal deposition to form air-gap.

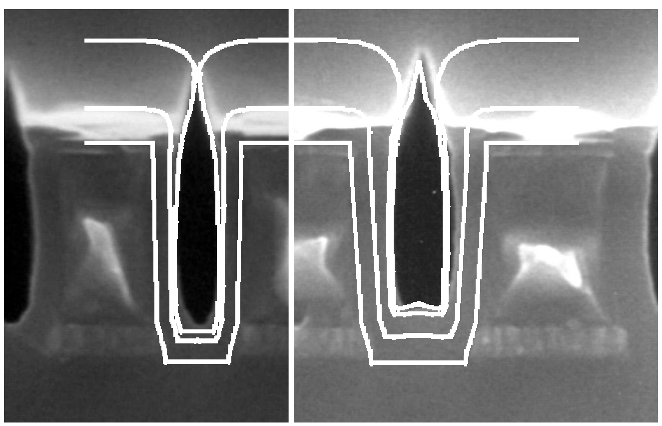
PETEOS and PESILOX to Control Air-Gap Sidewall Thickness



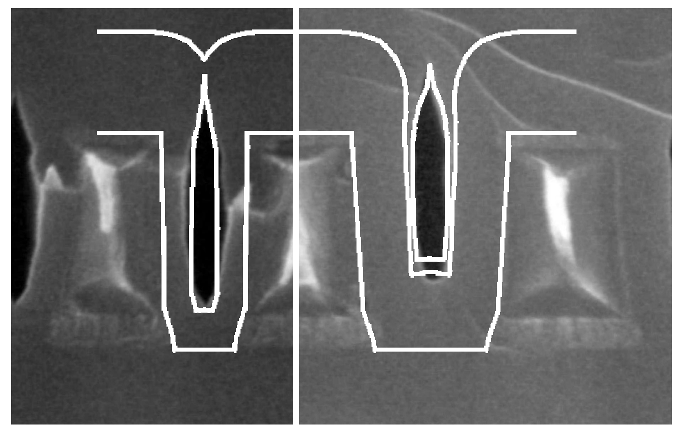
AG1: 3kÅ PESILOX



AG3: 2kÅ PETEOS, 1kÅ PESILOX



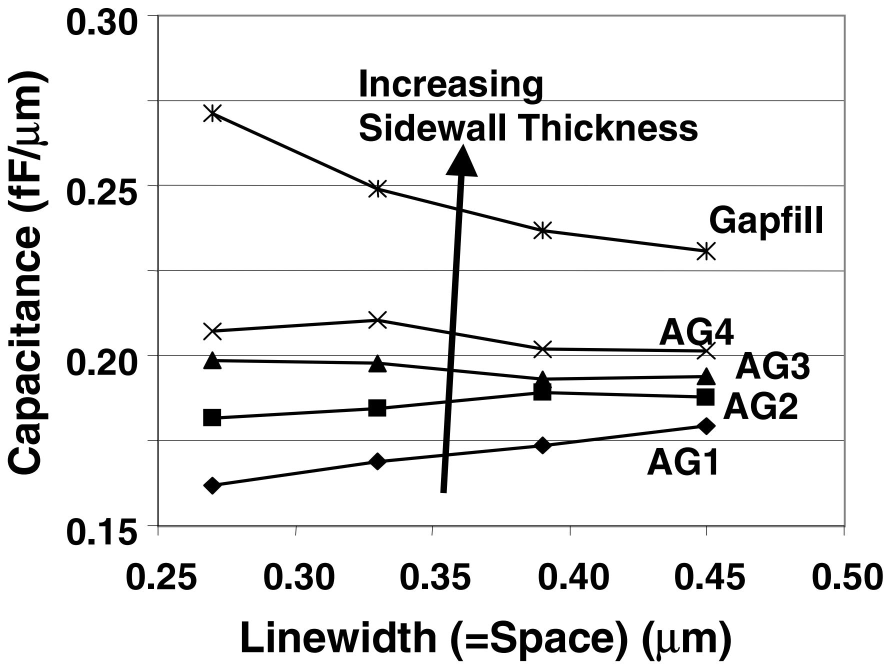
AG2: 1kÅ PETEOS, 2kÅ PESILOX

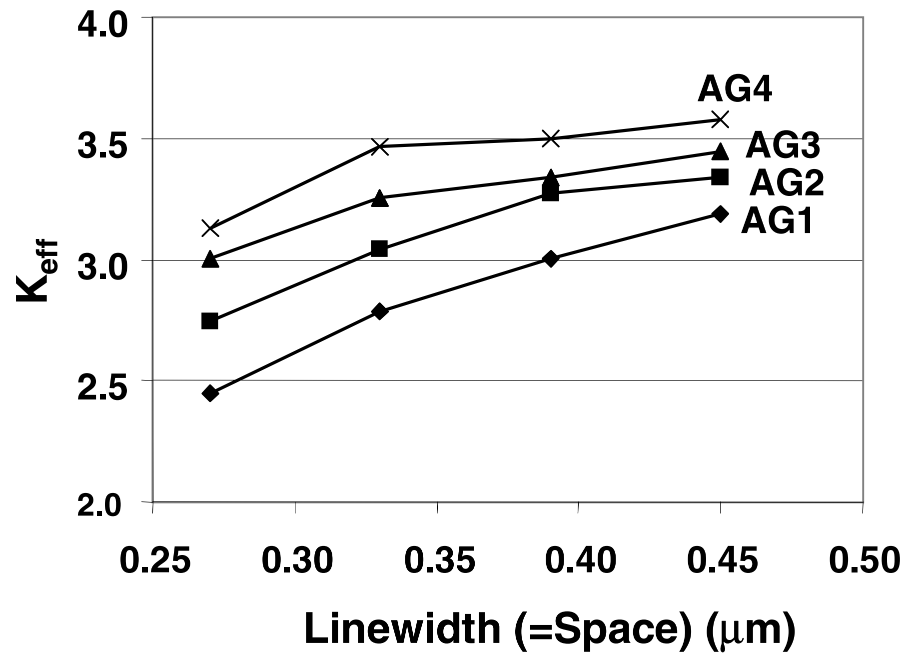


AG4: 3kÅ PETEOS

HDP-CVD used to pinch-off air-gaps

Extracted Capacitance vs. Feature Size





- Capacitance increases with sidewall thickness.
- Increase in via misalignment margin must be balanced against capacitance increase.

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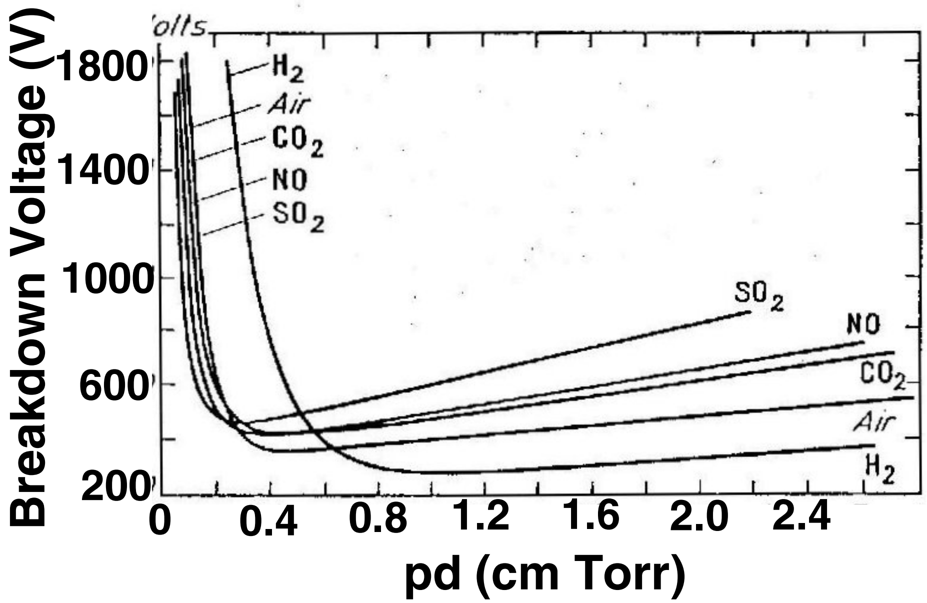
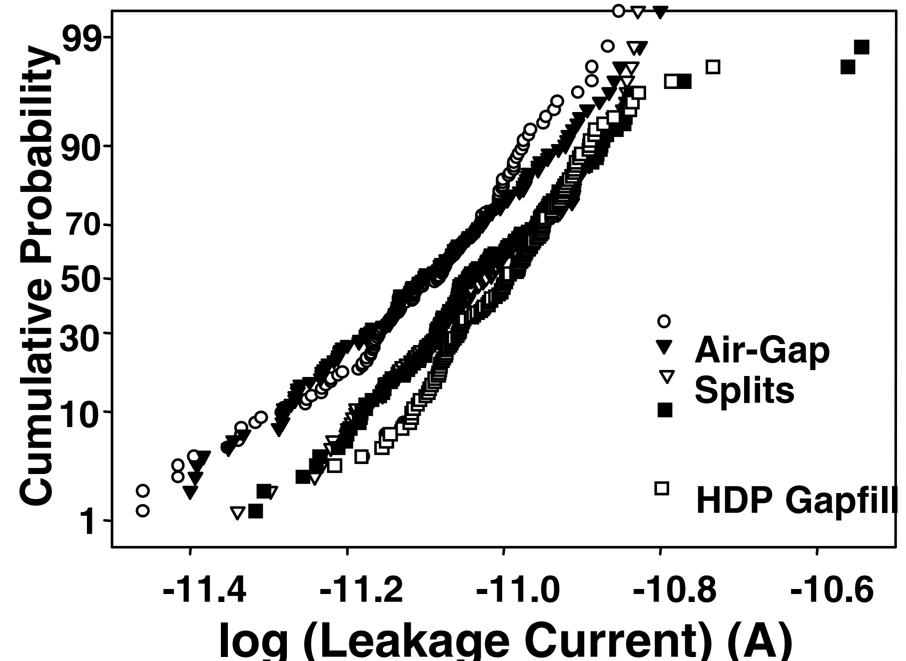
Electrical Reliability: Breakdown Voltage

Paschen's Curves*



Leakage Data
0.3µm/0.3µm line/space, 6.6V applied

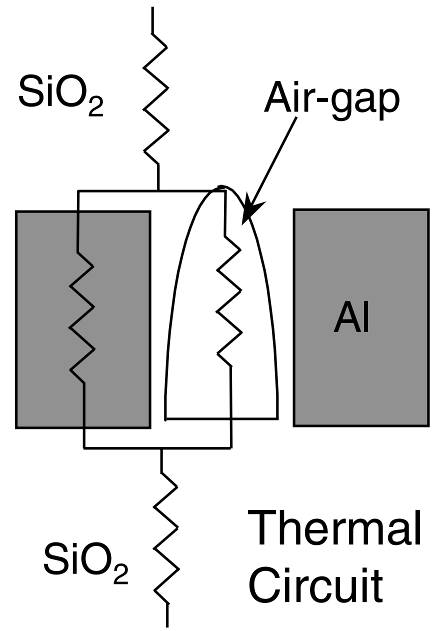


- Paschen's curves indicate that breakdown voltage increases dramatically at submicron dimensions.
- Leakage data indicates no breakdown well above operating voltage.

*Raizer, Yuri P., "Gas Discharge Physics", Springer-Verlag, 1997

Simulated Joule Heating and Thermal Reliability

Material	ΔT above $T_{substrate}$
Homogeneous SiO_2	4.9 K
Homogeneous low-K	76.7 K
Air-gaps w/ SiO_2 ILD	5.2 K



Thermal Resistance Circuit

- Heat conduction to substrate limited by interlevel dielectric
- Interconnects with air-gaps show comparable thermal performance to conventional SiO_2.

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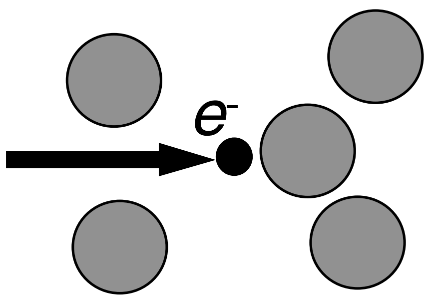
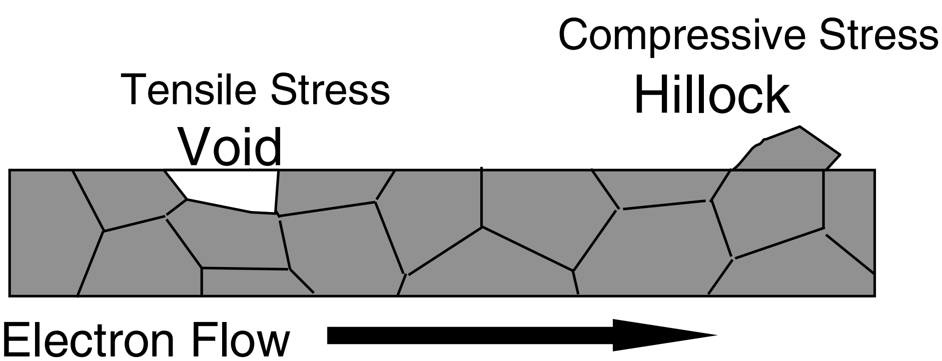
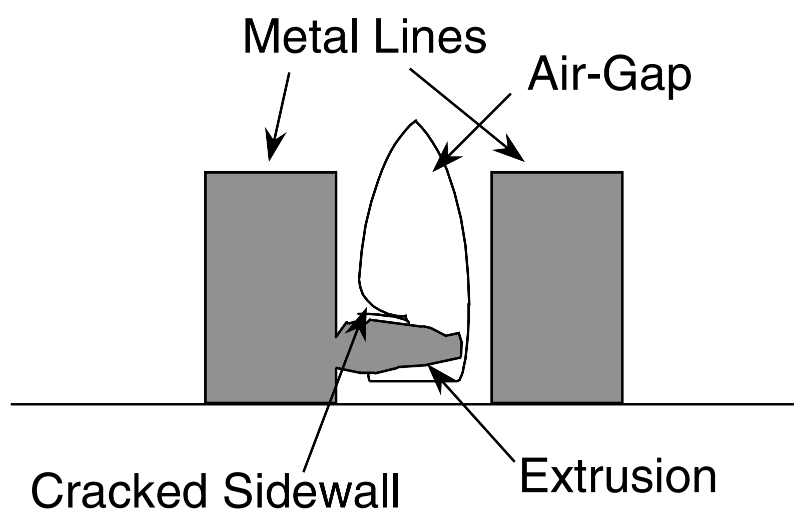
Electromigration Reliability



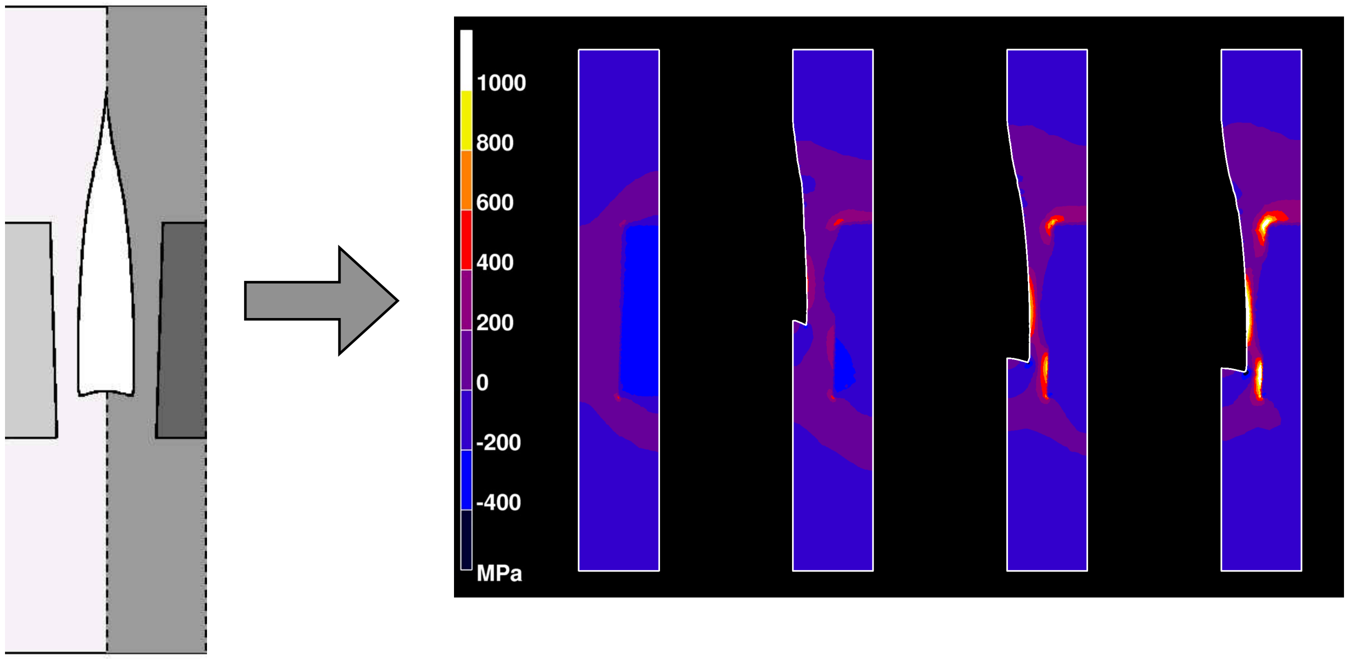
$$F = \frac{DC}{kT}\left(Z^{*} q \rho J + \Omega \frac{\partial \sigma}{\partial x} \right)$$

Metal atoms displaced by momentum transfer from electrons





Hydrostatic Stress Simulations

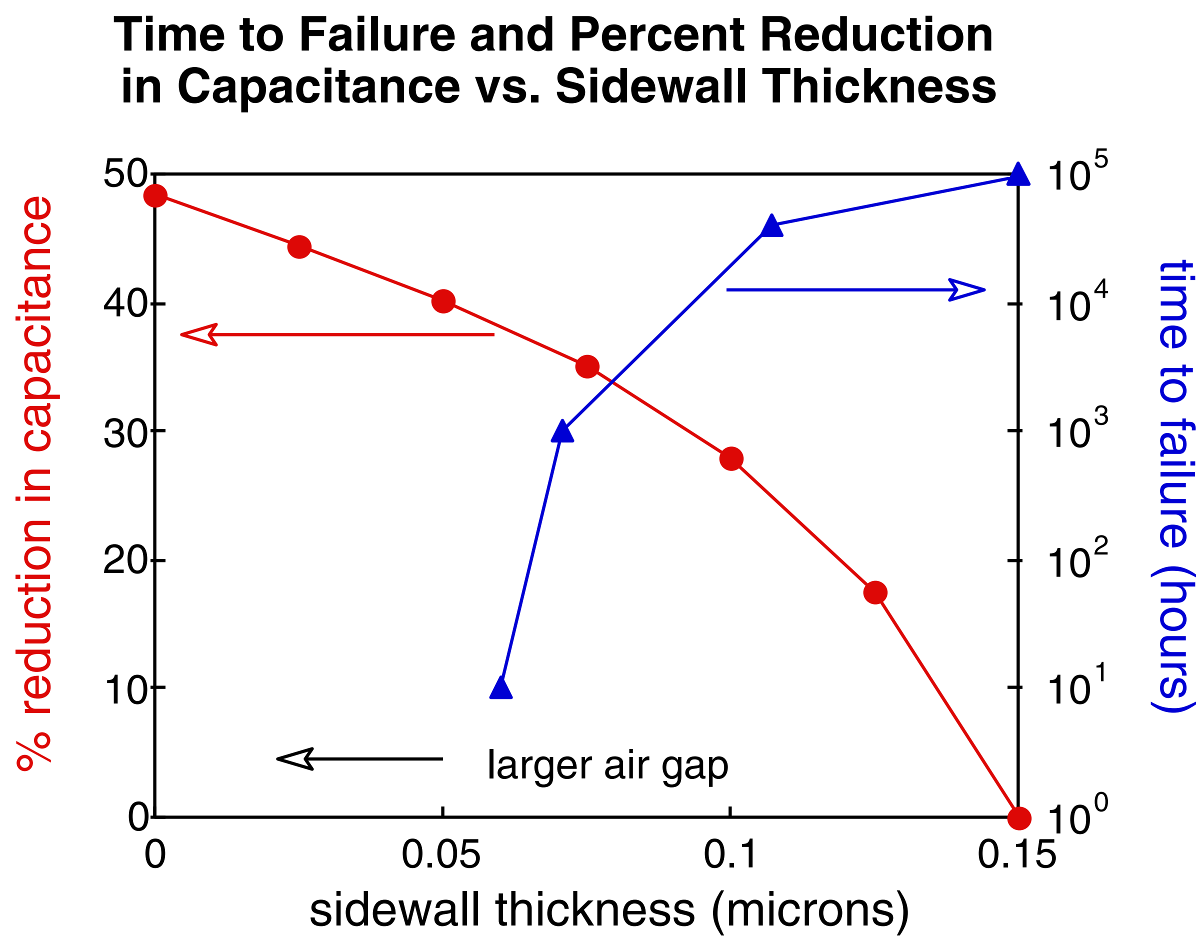


constants used:
Aluminum
E = 70 GPa
ν = 0.34
σ_{yield} = 200 MPa

Silicon Dioxide
E = 83 GPa
ν = 0.20

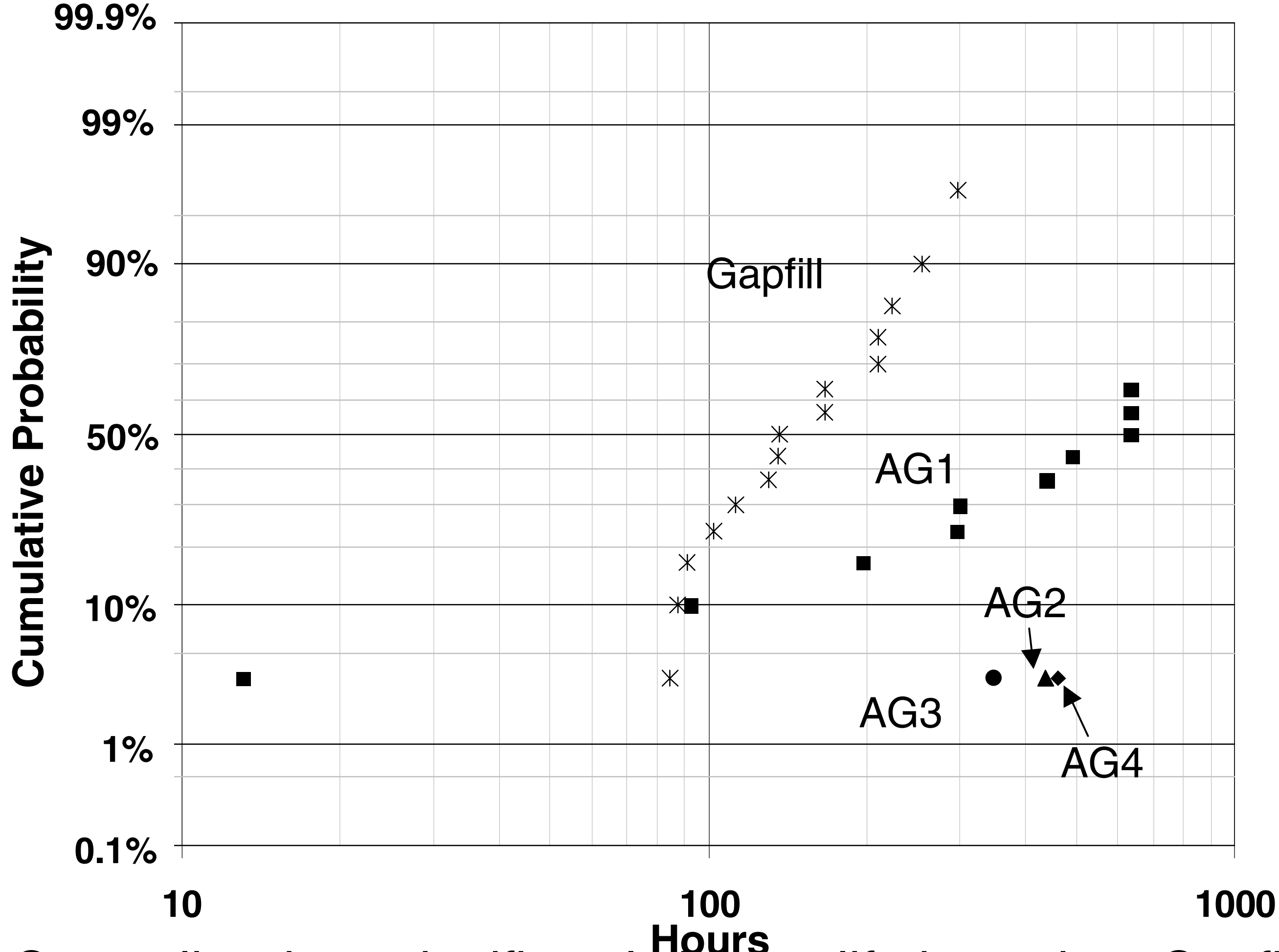
- Failure defined when dielectric stress reaches fracture stress.
- Stress in metal simultaneous with fracture stress in dielectric used to calculate electromigration lifetime.

Simulated Reliability/Performance Tradeoff



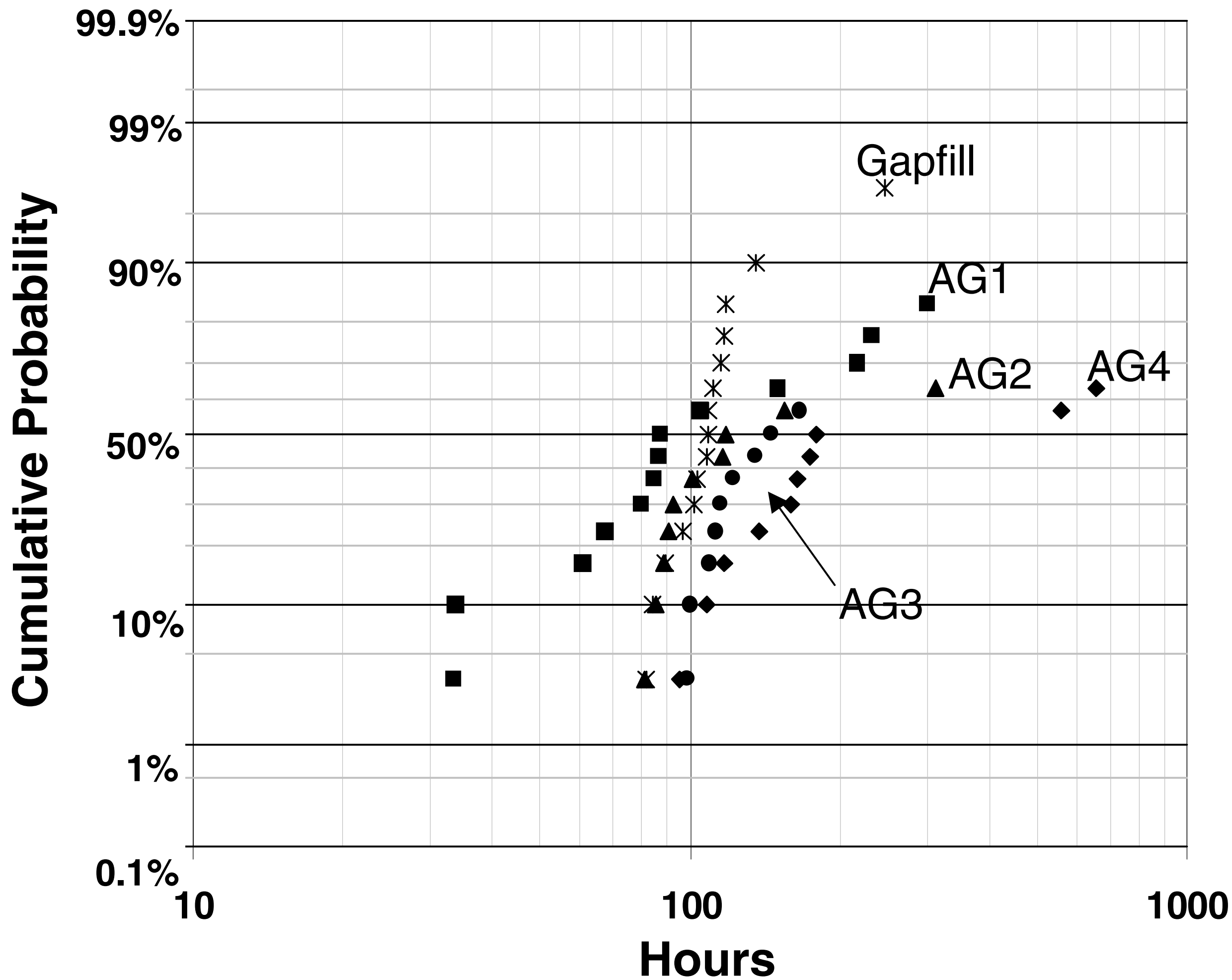
- Hydrostatic stress in Al when SiO_2 fractures is correlated with electromigration lifetime.

Electromigration Lifetimes: 0.27μm Linewidth



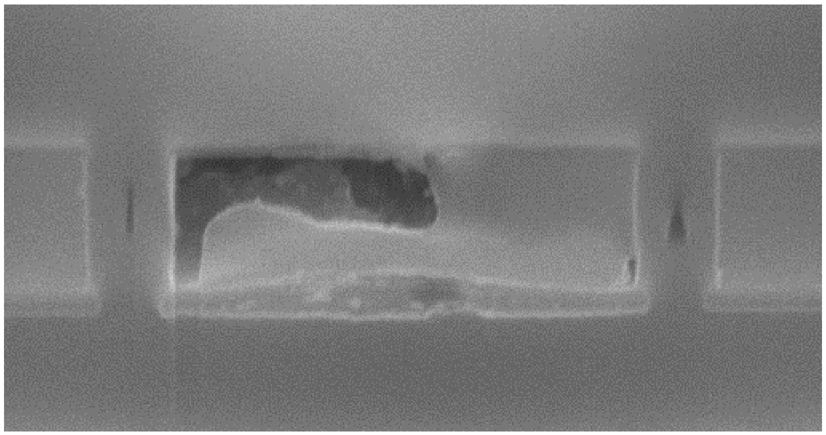
- Air-Gap splits show significantly longer lifetimes than Gapfill split

Electromigration Lifetimes: 1.26μm Linewidth

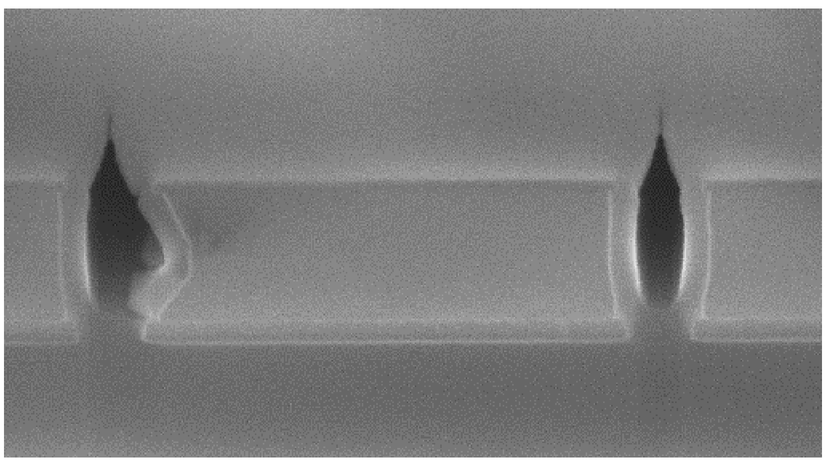


- Air-Gap splits show slightly better lifetimes than Gapfill split

FIB Mill Cross-Section



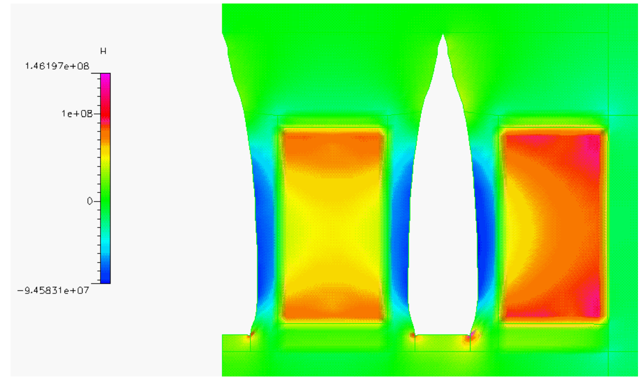
- Rigid gapfill dielectric unable to deform and reduce stress during electromigration.



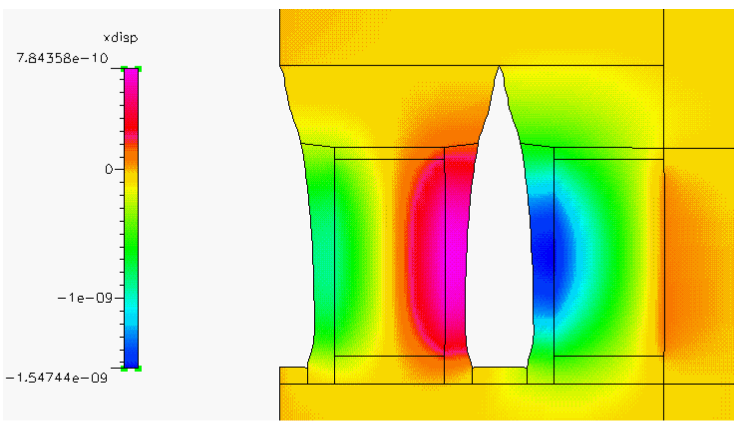
- Flexible air-gap sidewall deforms and reduces stress during electromigration.

Determination of Effective Modulus

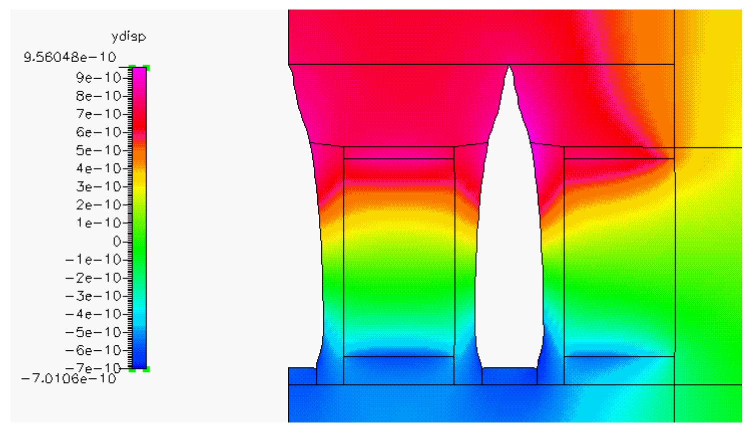
$$E = \frac{\sigma}{\varepsilon} \qquad \varepsilon = \frac{l - l_0}{l_0}$$



FEM plot of stress distribution



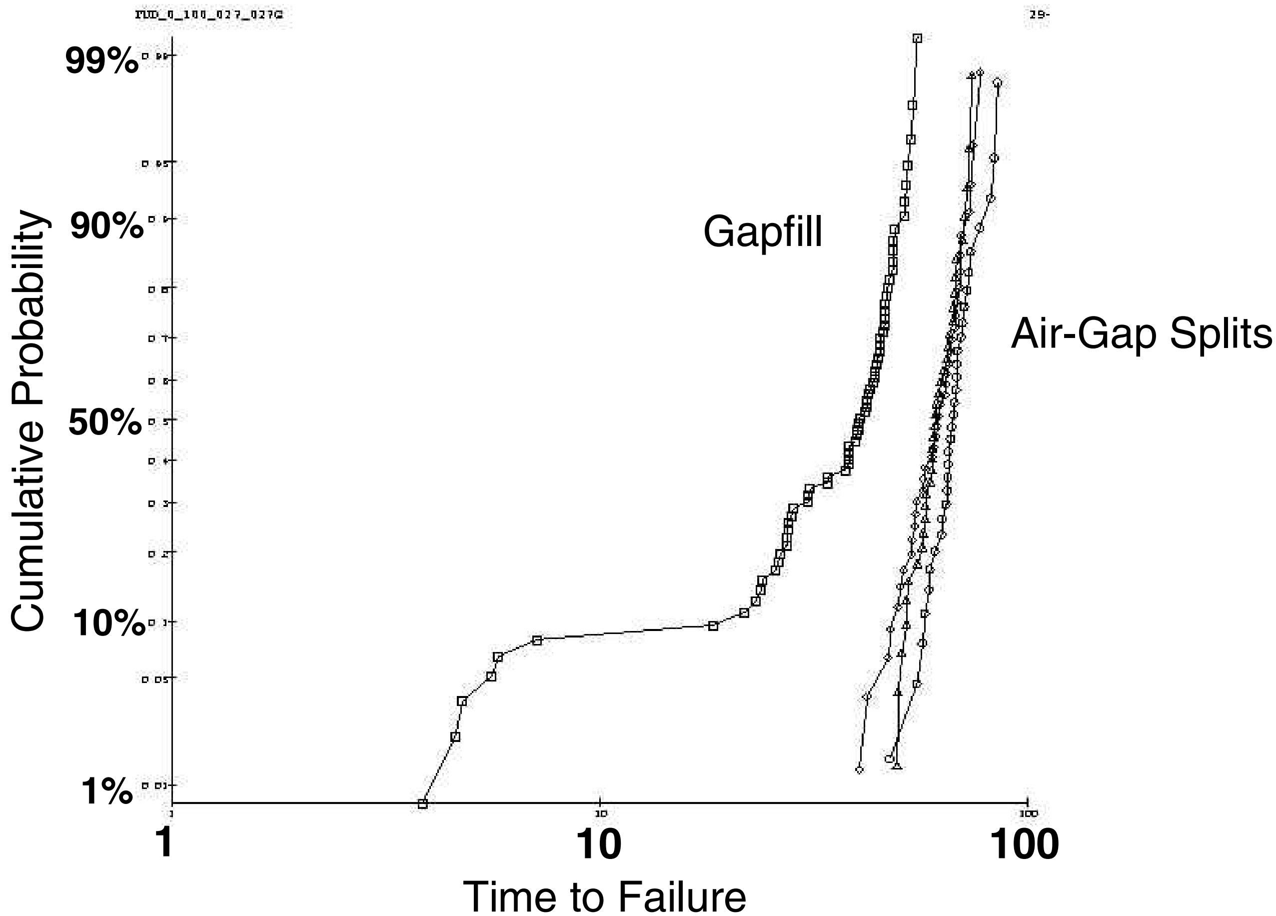
FEM simulation of x-displacement



FEM simulation of y-displacement

- Air-Gap Modulus of 10Gpa vs. Gapfill Modulus of 27GPa

MIT/EMSim Simulation Results



- Lower effective modulus increases electromigration lifetime

Electromigration Conclusions

- Air-gaps lower the effective modulus of the dielectric.
- Lower modulus reduces stress during electromigration.
- Effect of air-gap on modulus is greater in high aspect ratio lines.
- Air-gaps increase electromigration lifetime more in high aspect ratio lines.

Conclusions

- Demonstrated that capacitance reduction using air-gaps comparable to most low-K materials under investigation.
- Development of process techniques to reliably control air-gap shape and size.
- Application of process and capacitance simulators to interconnect modeling.
- Showed that electrical and thermal reliability of air-gaps comparable to homogeneous SiO_2.
- Showed that electromigration reliability of air-gaps can be significantly longer than traditional gapfill.