Future Challenges For Cleaning in Advanced Microelectronics

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Silicon Technology Development

Wafer Cleaning / Surface Preparation

- For many years, we just called it wafer cleaning. The perception was it is something that adds costs as a "non-value added process step."
- We later added "Surface Preparation" to recognize the importance of some wafer cleaning steps, e.g. pre-gate clean.

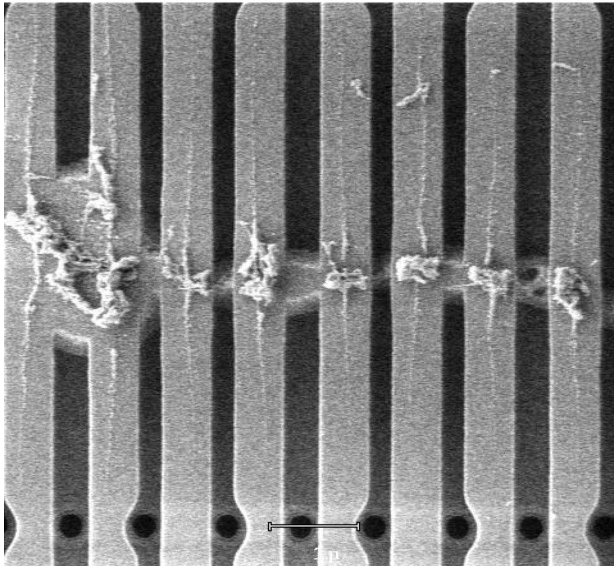
Wafer Cleaning / Surface Preparation

- We simply cannot achieve high yields without wafer cleaning / surface prep!
- Production-worthy CMP could not exist without post-CMP clean.
- Gate oxides wouldn’t work without pre-gate clean.
- Post-etch cleans for etch/resist residue removal are required for high yields.

Past Predictions

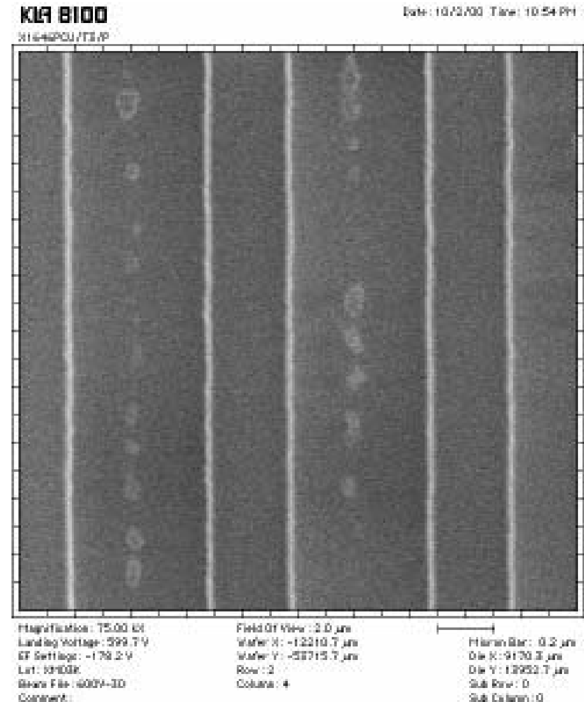
- In the early 1990's, several authors (including Allen) predicted move to all gas-phase wafer cleaning – e.g. plasma ash followed by plasma or vapor clean.
- This has not happened
- Gas-phase cleaning worked well for specific homogeneous material removal, but did not work well for removal of particle excursions or inhomogeneous process residues.

Residues Seen Post Ash + Dry Cleans



Blocked Trench Etch: Stringers

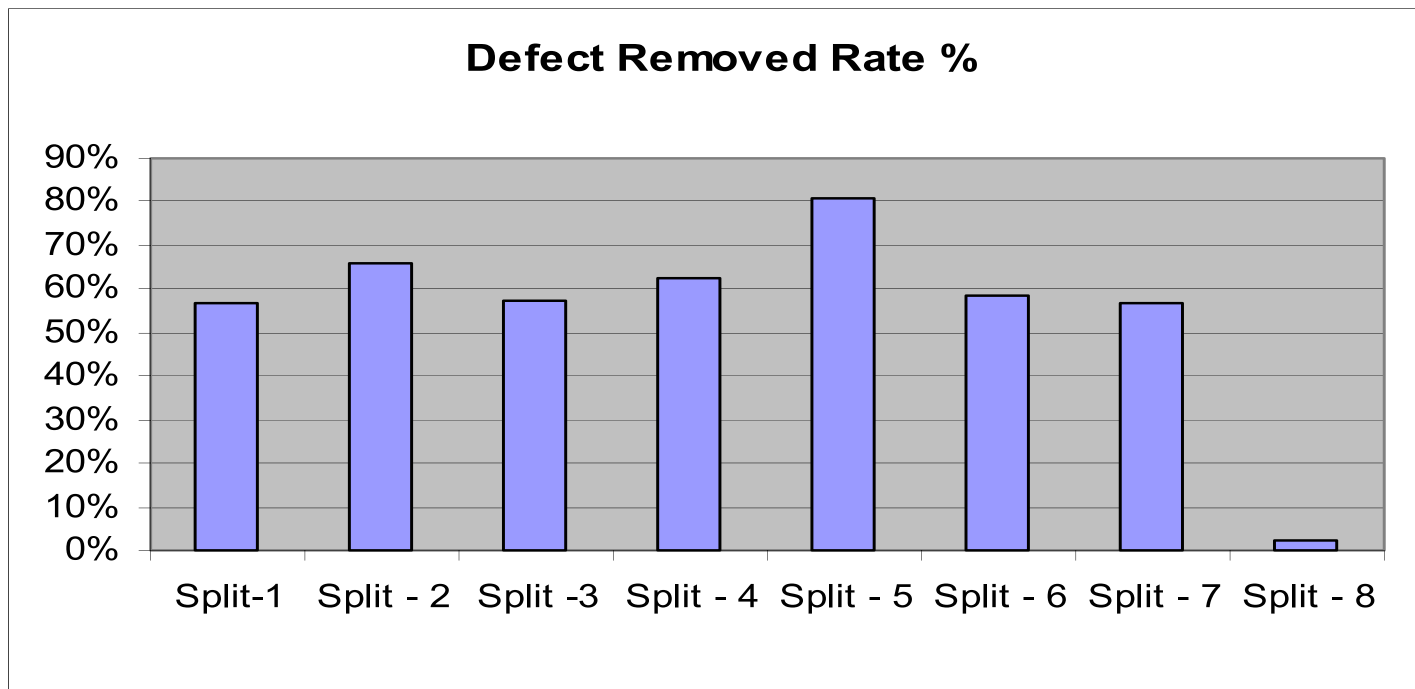
Via First Cu Dual Damascene process when post via etch clean was performed all dry (ash + plasma dry clean)



Crystalline Defect:

Post Trench clean in a Via First Cu Dual Damascene process. Post Trench clean was an insitu ash in the Trench etcher followed by a plasma dry clean

Cleaning Efficiency: Post Via Etch Clean Comparing Wet + Dry and All Wet Cleans



Split 1: Wet A
Split 2: Wet B, 3x
Split 3: Wet B, 2x
Split 4: Wet B, 1x
Split 5: Dry + Wet
Spit 6: Wet C + Wet B, 3X + Wet D
Split 7: Wet B, 3x + Longer Rinse
Split 8: Reference

Past Predictions

- Other authors predicted the convergence of wafer cleans – i.e. that a single cleaning chemistry/approach would have broad applications.
- This has not happened.
- Single cleaning chemistries don’t deal well with particle or process excursions. They also don’t work well for the large variety of new materials being introduced.

Wafer Cleaning Challenges New Materials

- In the 1980's it took us about 7 years to implement one new material – CVD W
- In the early 2000's, there is a proliferation of new materials
- Cu barriers (TaN)/Cu seed/Cu plating/Cu CMP
- Defect reduction & corrosion avoidance in Cu interconnect processing has been a huge challenge.
- Low-k dielectrics: FSG, OSG, Porous OSG's, Porous SOD's – dealing with F, then C, and now porosity. Cleaning & drying both critical.

Wafer Cleaning Challenges New Materials

- When we first introduced Cu with SiOx dielectric, single-step cleans showed some promise, but these ultimately could not deal with particle issues.
- We had to move to multi-step cleans, including extensive wet post-CMP cleans
- With the move to low-K, ULK, and porous dielectrics even more emphasis is required on multi-step cleans

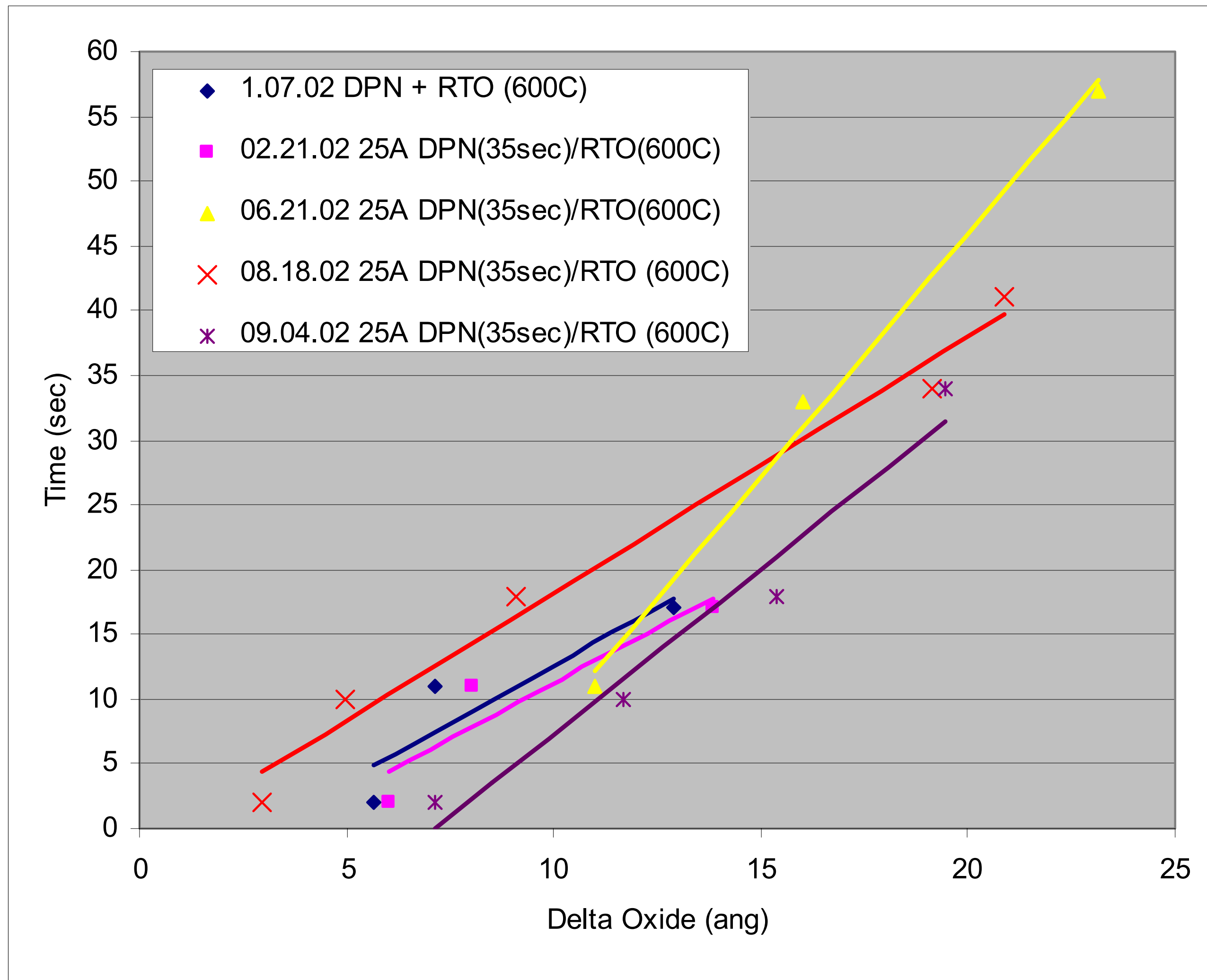
Wafer Cleaning Challenges New Materials

- For Al with SiOx, post-etch solvent cleans worked well to swell the polymer residues and then remove them
- For Cu/Low-K etch residues, aqueous and solvent mixtures are required – e.g. with chelating agents, buffering agents, plus water and solvents – to remove residues but not change the dielectric constant or the Critical Dimension

Wafer Cleaning Challenges New Materials

- Nitrided silicon dioxide gate diel.
- High-K gate diel. – HfSiON
- Poly-SiGe gate electrodes
- Metal gate electrodes
- Co silicide → Ni silicide
- Raised S/D (Si and SiGe)

Varying Etch Rate of Nitrided Oxide



Even somewhat similar films, when processed in new integration sequences can exhibit process variation that must be understood.

Wafer Cleaning Challenges New Materials

- The trend towards lower thermal budgets to enable ultra-shallow/ultra-abrupt junctions introduces cleaning challenges
- Lower thermal budget tends to lead to incomplete chemical conversion of layers, thus making chemical composition much less homogeneous
- Lower NiSi processing temp requires different approaches to NiSi cleaning

Wafer Cleaning Challenges New Materials

- Tantalum pentoxide for decoupling capacitors
- PZT ferroelectric for embedded FRAM, with Ir and IrOx electrodes and AlOx sidewalls.
- MRAM, Ovonic Memories
- SOI – PD and FD
- Strained Silicon (SiGe / Si)
- Double-gate structures – e.g. FinFET, Pi-Gate, etc.

Process/Equipment Trends

- Single-wafer wet cleans
- Implementation of clustered cleans
- Interconnect post-dielectric-etch cleans that can deal with high Aspect Ratios and porous low-K materials
- Advances in post-Cu CMP cleans
- New materials cross-contamination control

Single-Wafer Wet Cleans

- SW wet cleans could be used for 85% of all cleans today, i.e. they work technically, but not all are cost effective
- So, focus has been on enabling applications
  - Backside cleans for particles & metals
  - Cu removal from the wafer bevel to eliminate Cu peeling
  - Post-CMP clean (cannot allow wafers to sit after CMP before cleaning)

Single-Wafer Wet Cleans

- More single-wafer cleans are becoming cost effective as processes require better wafer-to-wafer interface control
  - Pre-gate clean for ultra-thin gate dielectrics (typically nitrided silicon dioxide today)
  - Pre-gate clean for high-K gate dielectrics
  - Post-etch cleans with low-K dielectrics, especially porous low-K materials

Clustered Cleans

- In the early 1990's, we did a joint SEMATECH, FSI, AT&T, and TI gate clustering project.
- We clustered an FSI Excalibur-II system to single-wafer RTO & RTCVD poly.
- For gate dielectrics down to about 2.8 nm, we saw little or no improvement in gate properties.

Clustered Cleans

- In 2002, TI is re-evaluating clustering of oxidation, plasma nitridation, and polysilicon deposition to improve the effective gate dielectric thickness for sub-1.5 nm gate dielectrics. (No capability to cluster a single-wafer clean at this time).
- We believe a 0.1-0.2 nm improvement may be possible, to help delay when we must implement a high-K replacement.

Clustered Cleans

- Post-CMP cleans are clustered to the CMP tools to avoid time lag between the CMP and cleaning
- For advanced post-Damascene etch cleaning, one proposal is to move to a dry plasma step to condition the photoresist with no over ash, followed by a wet process to remove the residue with no lag time or air exposure.

Clustered Cleans

- We will most likely use clustered cleans prior to high-K gate dielectrics, and also cluster to the gate electrode deposition.

Post-Damascene Etch Cleans

- Cleaning technology is needed to deal with very high-aspect ratio vias and porous low-k dielectrics, & not change the CD or dielectric constant!
- Supercritical CO_2 ($SCCO_2$) processing has shown a lot of promise.
- Some have attempted to use $SCCO_2$ to replace the entire ash and clean steps; this hasn’t work well with the loading effects of the bulk photoresist and the BARC layers.

Post-Damascene Etch Cleans

- For first implementations of $SCCO_2$ it may be better to do a soft ash (with small bias to control reactions with the low-K) followed by the $SCCO_2$/co-solvent residue removal.
- Key careabouts:
  - Ashing can change the composition of the porous low-K materials (change the K value!)
  - Processing can etch the low-K (change CD)
  - Drying of the porous low-K is required to control K; enabling feature is near zero viscosity for water displacement and near zero surface tension for subsequent removal of residual CO_2.

Post-Damascene Etch Cleans

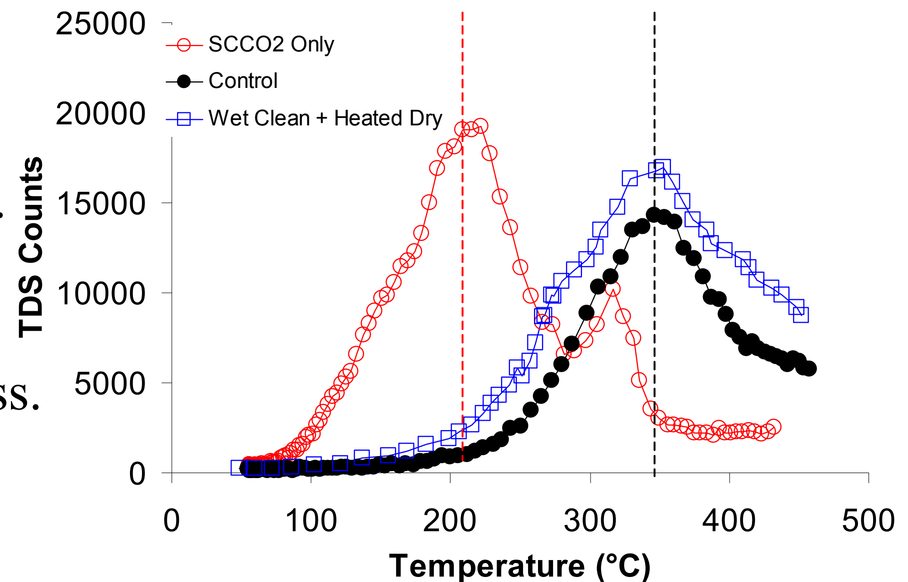
- $SCCO_2$ could find an application for just porous ULK drying – after a wet clean.
- Several researchers are also looking at $SCCO_2$ for trace contaminant removal – e.g. F^-/F_2, N_2, NH_3, etc.
- Will SCCO2 cleaning be cost effective?
  - It uses small amounts of co-solvent.
  - Can possibly recycle the CO2

$SCCO_2$ Process Results – MSQ ULK

Cleaning Conditions	κ-value (25°C)
As Deposited	2.25
Ash only (control)	2.55
Wet clean + Heated dry	2.67
SCCO2 clean	2.37

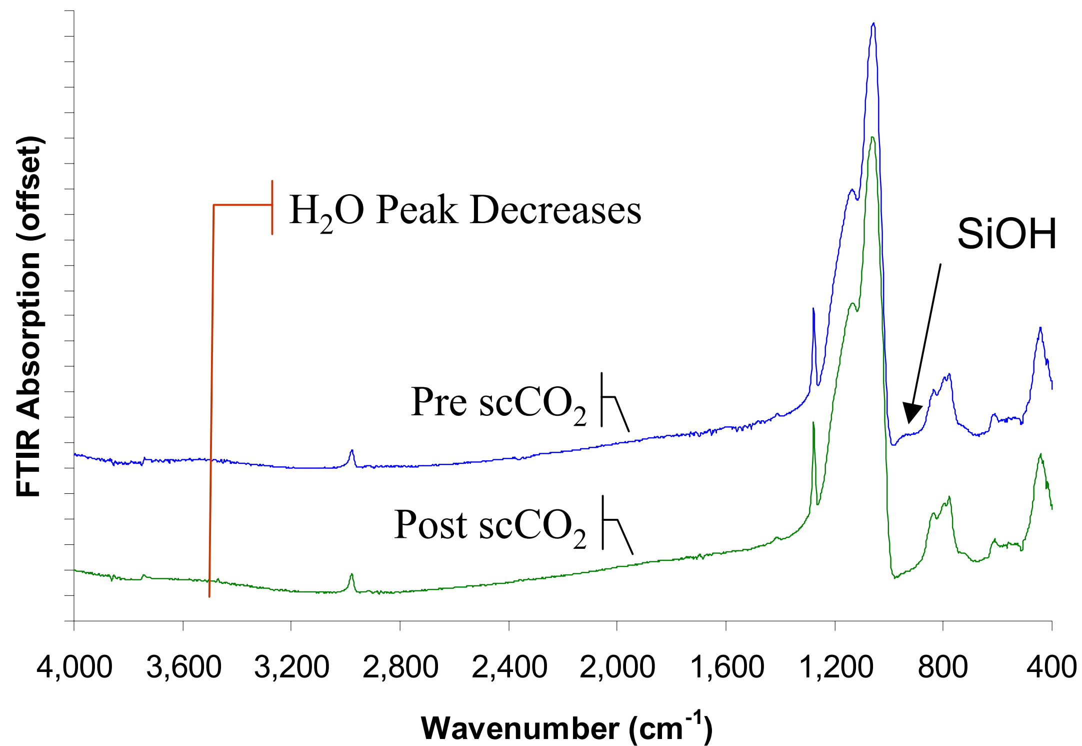
Dielectric constant measurements show best result with $SCCO_2$ clean of Porous MSQ ULK films.

Thermal desorption analysis explains k value results. Peak at 200C is due to physi-sorbed H_2O which has a minor impact on k, and is repairable. Peak at 350C is due to silanol, whose presence is evidence of film degradation from ash/wet clean process. SCCO2 shows much less silanol.



$SCCO_2$ Wafer Drying

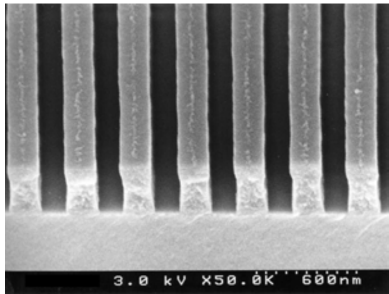
- Post wet clean drying of ULK
  - $SCCO_2$ doesn't damage porous MSQ ULK film
  - Silanol content is decreased



$SCCO_2$ Post Ash Cleans

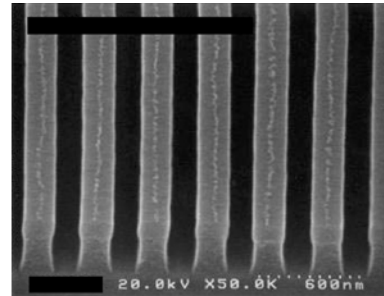
- Cleaning possible but familiar issues remain
  - Inadequate rinse process
  - Polymer / Dielectric selectivity
- Best process window still to be defined

NOT CLEAN



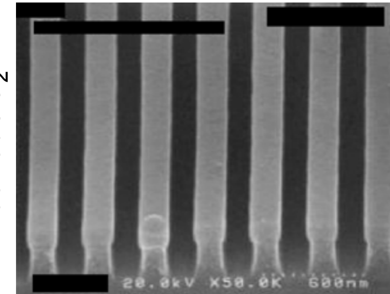
Post-$scCO_2$

PRE-$scCO_2$

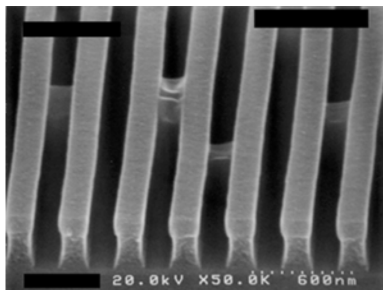


CLEAN

Post-$scCO_2$



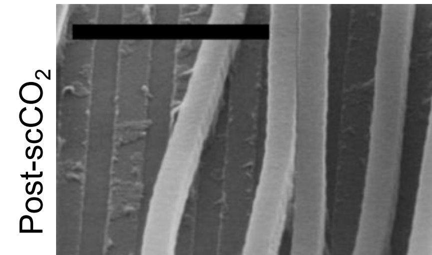
REDEPOSITION



Post-$scCO_2$

DIELECTRIC ATTACK

Post-$scCO_2$



$SCCO_2$ Cleaning

- Some cautions:
  - In processing systems, we have learned that pressure changes, gas flow changes, and temperature changes can generate particles due to physical and chemical processes
  - This may be a great challenge for producing very clean wafers with $SCCO_2$ systems – system design and process/wafer sequences will be very critical.

Post-CMP Cleaning

- Single-step post-Cu CMP cleans not working well
- Cu CMP residues difficult to remove due to photo-diode induced corrosion, Cu scratches, and CMP low-k damage.
- Follow up cleans required - e.g. dilute acids &/or solvents in scrubbers, spray tools, or immersion tanks.

Post-CMP Cleaning

- We need better Cu CMP clean processes
- And, we need better Cu CMP processes or a totally new Cu planarization process!

New Materials Cross-Contamination Control

- With so many new materials – starting with Cu, cross-contamination control has been a major effort for the wafer cleaning researchers.
- It you decide to manage cross-contamination control of all new materials by dedicated equipment it will be cost prohibitive to experiment with many new materials.
- A better approach is to understand what processes require dedicated tools

New Materials Cross-Contamination Control

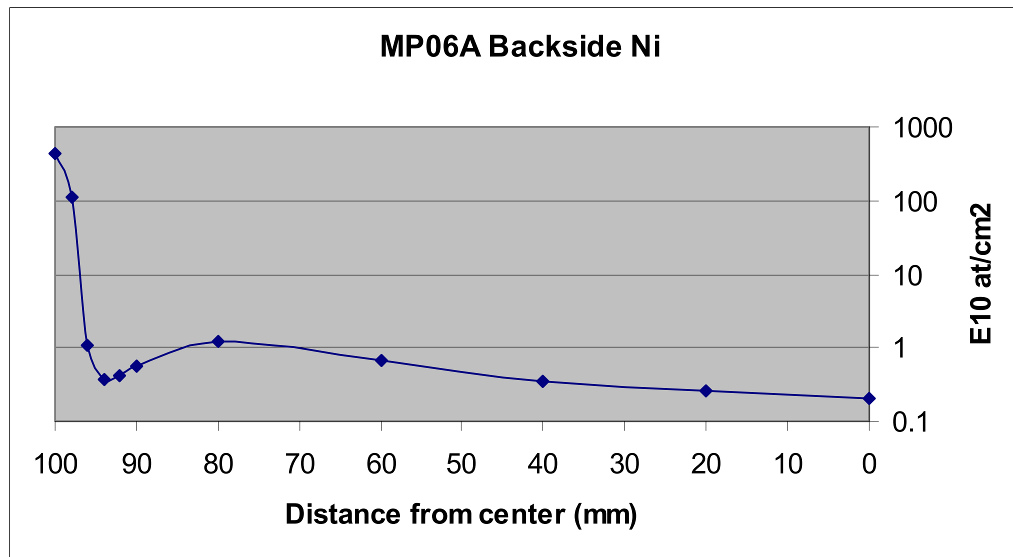
- Charlotte Tipton Appel and Trace Hurd spearheaded the Cu cross-contamination protocol development
- They performed experiments on wafers and tools and used TXRF & VPD ICP-MS for metals detection on wafers. They then used TOF-SIMS to evaluate local signatures within a wafer (e.g. tool wafer chuck related).

New Materials Cross-Contamination Control

- They developed effective wafer backside cleans to not have to dedicate lithography or metrology tools to Cu.
- They also developed protocols for chamber/chuck cleaning if a Cu wafer is broken in a shared tool.
- This same approach has been applied to NiSi, Ta_2O_5, ZrSiOx, HfSiON, PZT, Ir/IrOx, etc.

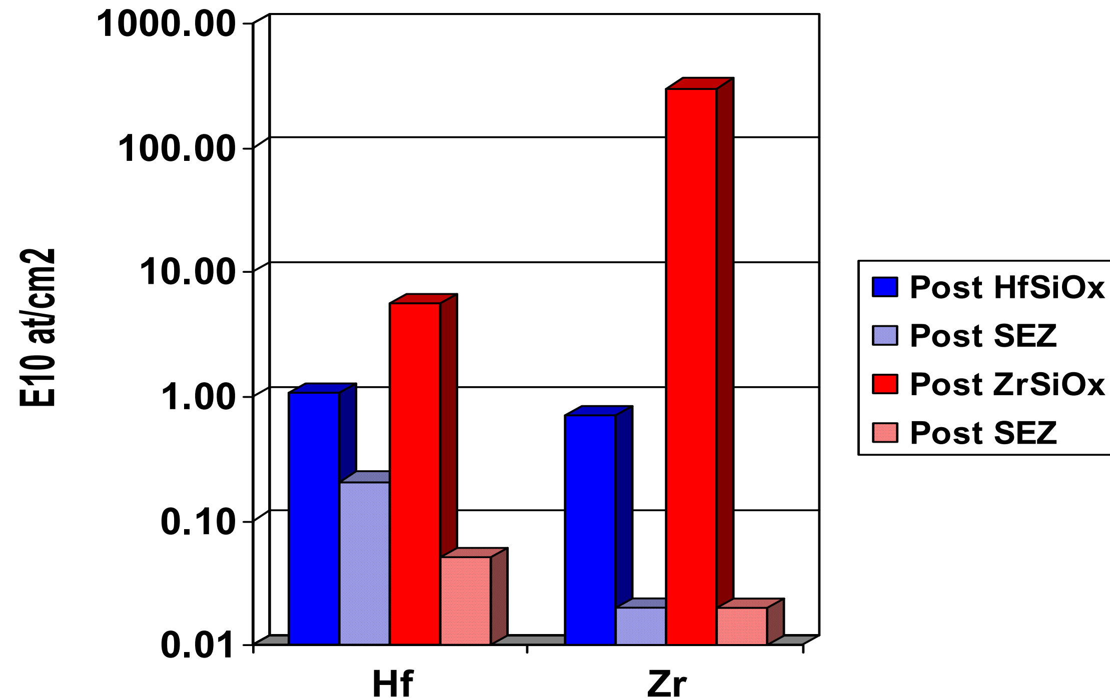
NiSi Example

- TXRF and VPD ICP-MS were giving conflicting data on Ni backside contamination coming from the Ni PVD chamber
- No Ni transferred to the PVD robot
- ToF-SIMS showed that Ni contamination was highly localized to the edge of the wafer (clampless deposition)



High-K Gate Contamination

- Hf/Zr backside contamination from silicate dep and removal backside clean
- VPD-ICP-MS Analysis



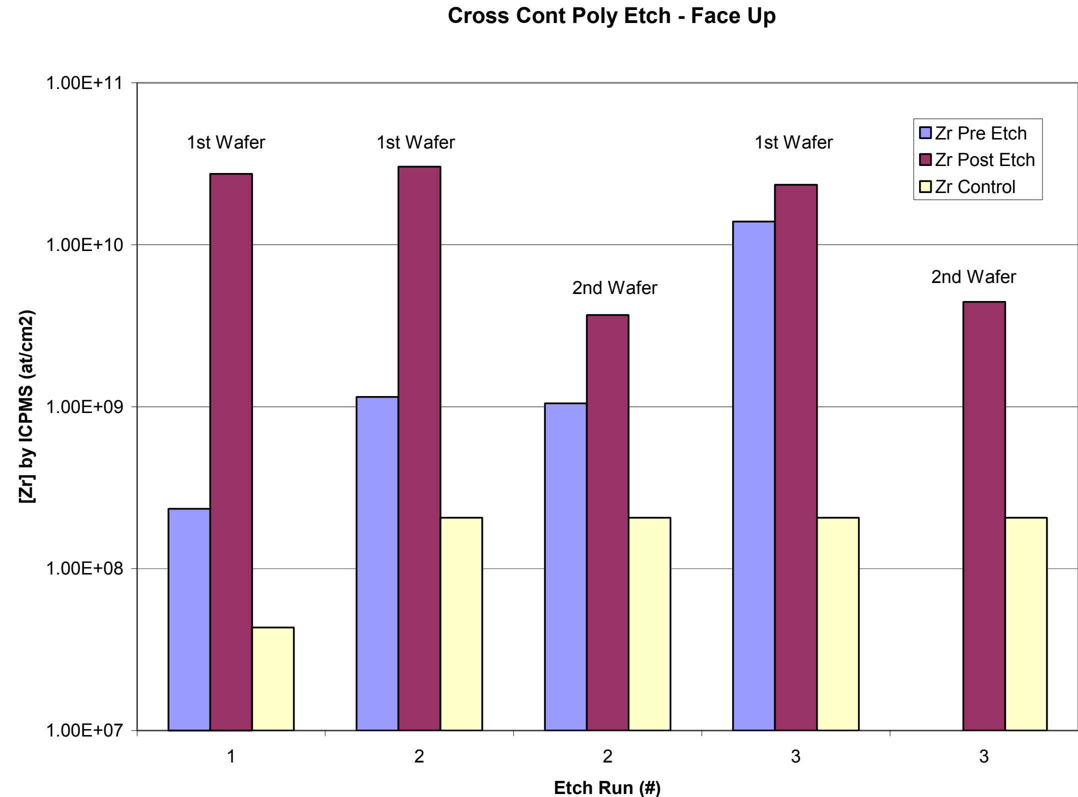
Vapor Pressure (torr)

Element / Compound	250C	500C	800C	1000C	1414C	MP (C)	BP (C)
Zr	1.58E-47	1.58E-29	5.01E-19	4.84E-15	4.61E-10	1855	4409
Hf	2.51E-52	2.51E-32	1.00E-20	5.23E-16	7.91E-10	2243	4603
ZrO2						2710	
HfO2						2774	

Poly Etch - ZrSiOx Cross Contamination

Wafer front side after timed etch in ER27P-B

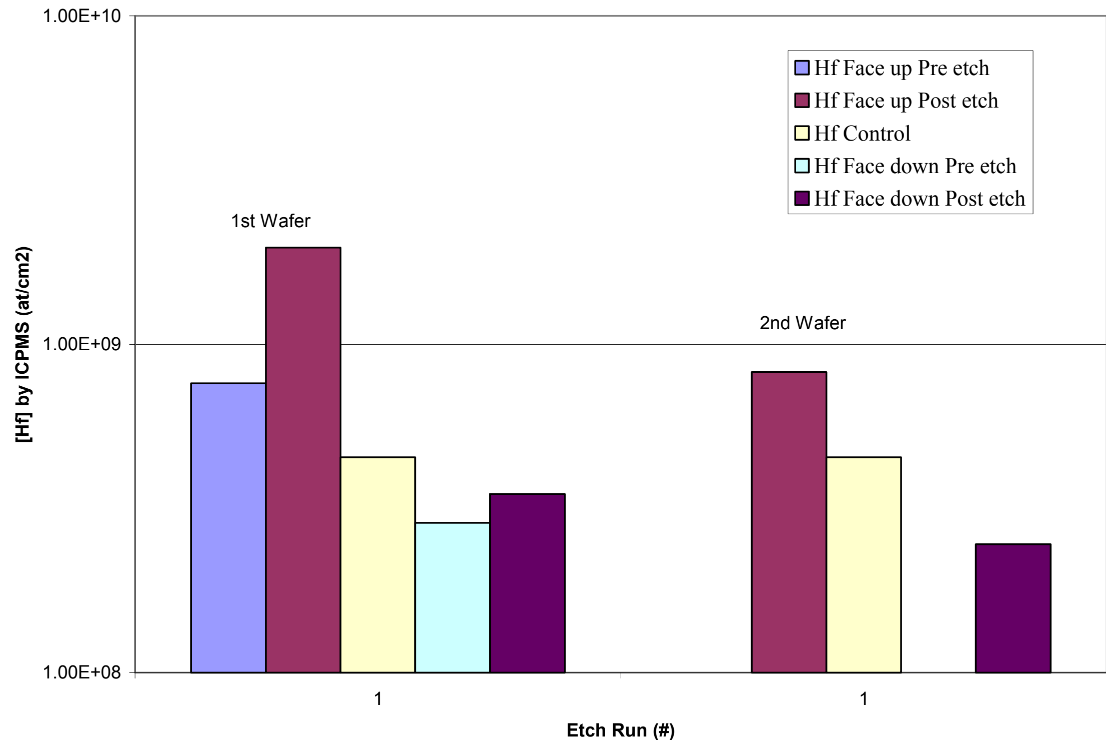
- Pre and post 3 lots.
- Zr rises to above FEOL spec on 1st wafer post.
- Drops to below FEOL spec on second wafer.
- Indication of background Zr level being created in tool.



Poly Etch - HfSiOx Cross Contamination

Wafer front and back side after timed etch in ER27P-B

- Pre and post 1 lot.
- Hf detected but << FEOL spec.
- Generally < E9 at/cm^2



ESH and Wafer Cleaning

- The move to dilute chemistries in wafer cleaning has positive ESH benefits (safer for workers and less chemical use)
- The use of $SCCO_2$ cleans with small amounts of co-solvents may dramatically reduce the total solvent usage
  - Reduced chemical use / waste / disposal
  - Safer for workers

ESH and Wafer Cleaning

- $SCCO_2$ drying could reduce IPA use for drying
- Will $SCCO_2$ cleans increase ozone depletion by CO_2 emissions? No, we will use CO_2 from other industry byproducts (that would normally be exhausted to the air) and not generate any new CO_2

CO_2 Calibration

- A 100 W light bulb lit for 10 hours requires generating 3 lbs of CO_2. (http://globalwarming.enviroweb.org/ishappening/sources/sources_co2_facts3.html)
- Human breathing releases 2.2 lbs CO_2/day/person; The DFW Metroplex's 5 million people emit approx. 458K lbs/hr. (http://cdiac.esd.ornl.gov/pns/faq.html)
- Combustion of 1 gallon of gasoline produces ~22 lbs of CO_2; traffic within a half mile radius of TI in Dallas produces ~23,000 lbs/hr CO_2. (Phil Matz, TI)
- At 40,000 wafer/month, on a 10 LM device, $SCCO_2$ post-ash cleans will utilize ~5,000 lbs/hr CO_2 (recycled from production at other sources). (Phil Matz, TI)

ESH & Wafer Cleaning

- We need to be diligent in the early ESH assessments of new chemicals before we get them implemented into routine process use.
- Early identification of ESH issues can help us pursue alternative up front – and eliminate delays and problems later.
- I am pleased to be a part of an industry that has been proactive in ESH issues!