Novel Deposition Processes for High-*k* Gate Stacks on Silicon and Germanium Substrates

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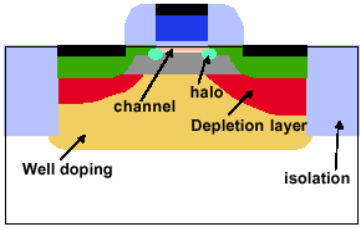
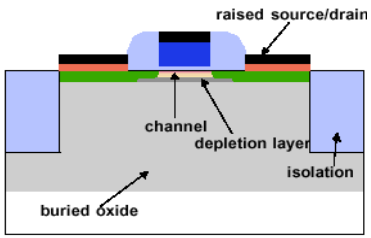
Outline

- Motivation and background
- Low thermal budget routes to high-*k* dielectric/semiconductor structures
  - ***UV-ozone oxidation (UVO) of ultra thin metal precursor layers***
  - ***Atomic layer deposition (ALD)***
- ALD as a tool for gate workfunction engineering
- UVO processing of ZrO_2 gate dielectric on Ge (100) substrates
  - ***Summary of electrical data from Pt/ZrO_2/Ge PMOSFET's***
  - ***Microstructure and interface abruptness***
- ALD of ZrO_2 and HfO_2 on Ge (100) substrates
  - ***Microstructure and dielectric/Ge interface***
- Conclusions

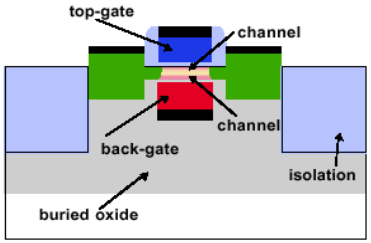
Future Device Technology



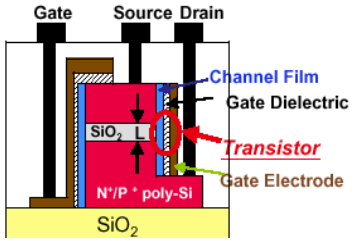
Bulk CMOS



FD SOI CMOS

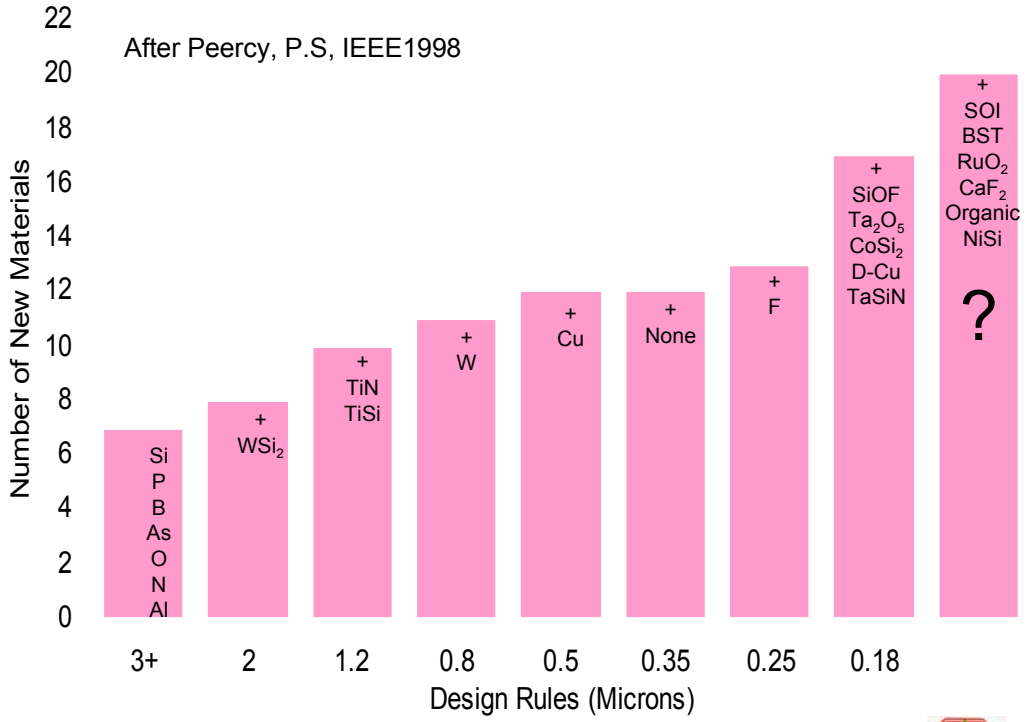


Double-Gate CMOS

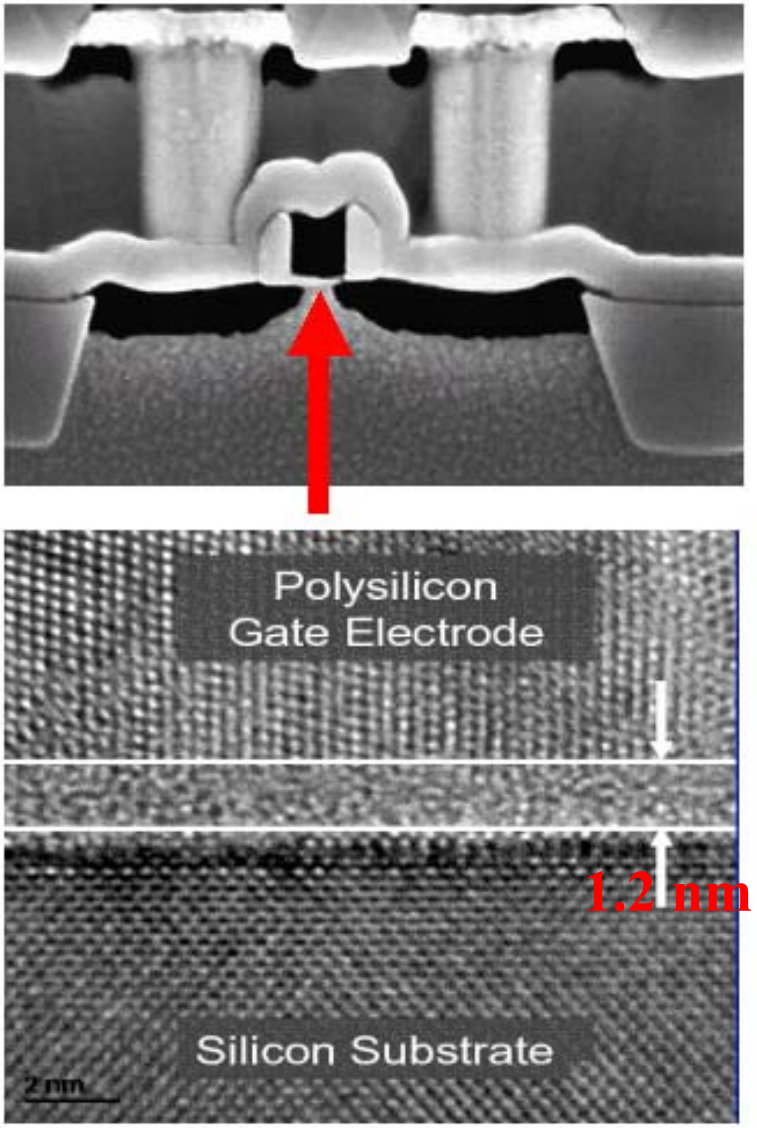


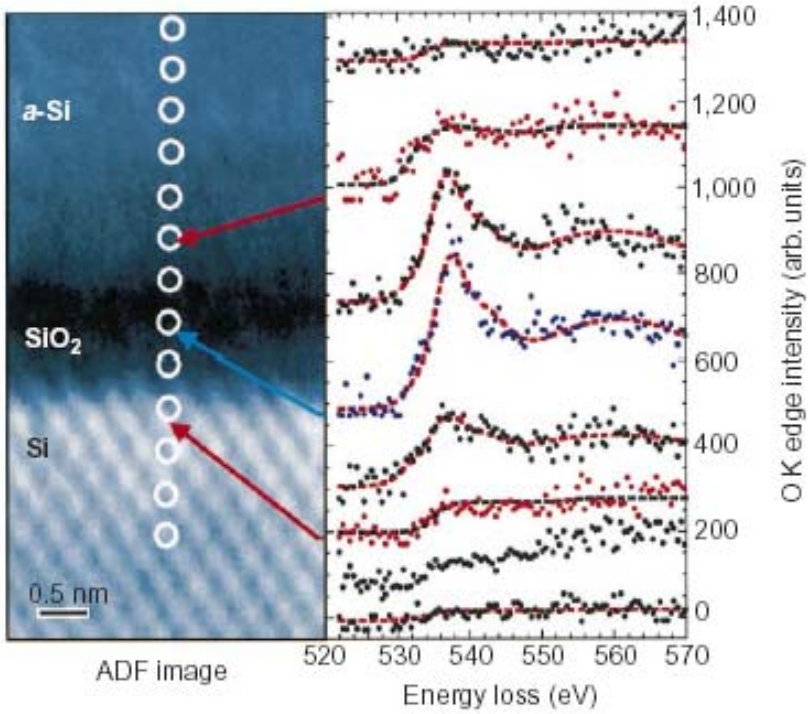
Vertical MOS

- New structures
- New materials
- New deposition processes



Physical Limits of SiO_2 Gate Dielectrics





- EELS O-K edge spectra recorded point by point across a gate stack containing a thin gate oxide.

D. A. Muller et. al., *Nature*, **399**, 758-761 (1999)

- Bulk SiO_2 properties (e.g. large bandgap) lost for films ≤ 8 Å in thickness

Gate Dielectric Technology Evolution

Transistor Drive Current $I_D \propto g_m \propto \frac{\kappa}{thickness}$

Today

1.5 nm SiO_2 $\kappa \sim 4$

Si

Near future

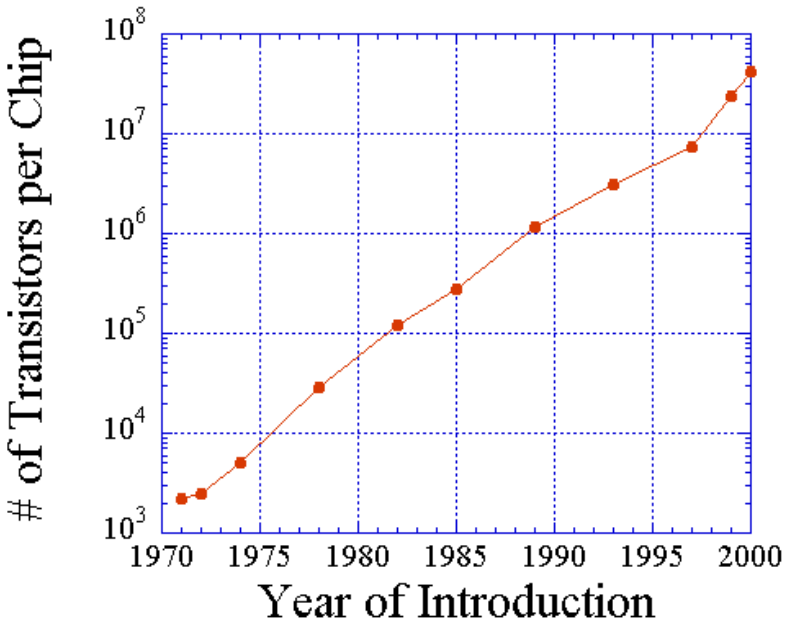
EOT > 1 nm

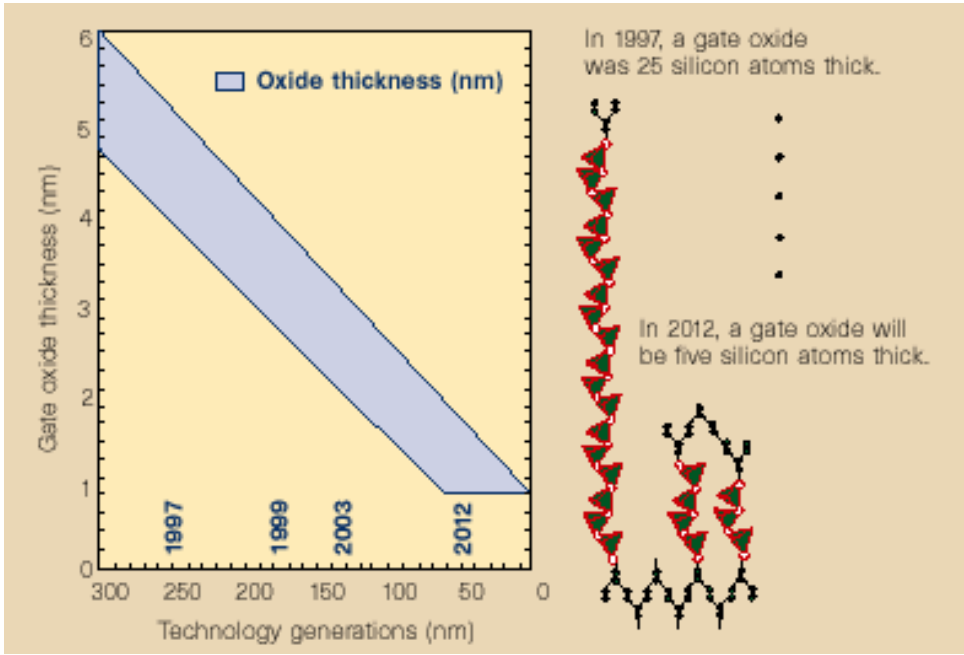
Si_3N_4 $\kappa \sim 8$

Long term

EOT < 1 nm

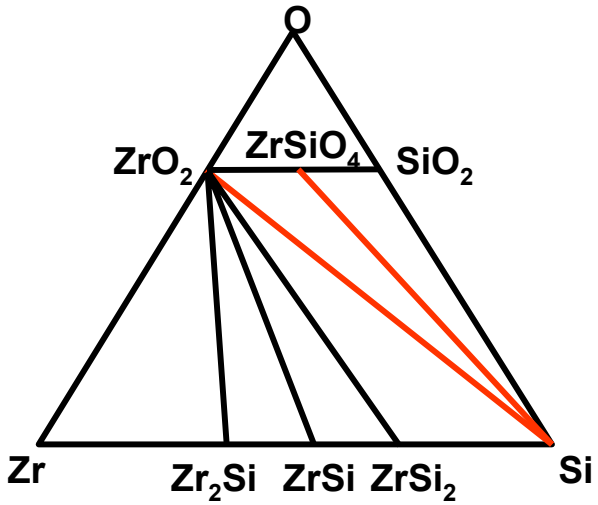
$\kappa \sim 20$





Desirable High-*k* Gate Dielectric Properties

Material Properties	Electrical Properties
κ > 15; uniform	Equivalent T_{ox} < 1 nm
Thermally stable on Si (no **need** for barrier layer)	Low leakage current at the same equivalent T_{ox}
No reaction with electrode (stop B penetration if poly-Si)	No mobility degradation (low interface trap density)



Ref.) Beyers et.al, J.Appl.Phys., 56, 147(1984)

Material	SiO_2	ZrO_2/HfO_2	Silicate (Zr,Hf)
Dielectric Constant	3.9	**~25**	15 ~ 25
Band Gap (eV)	8.9	**~5.7**	~6

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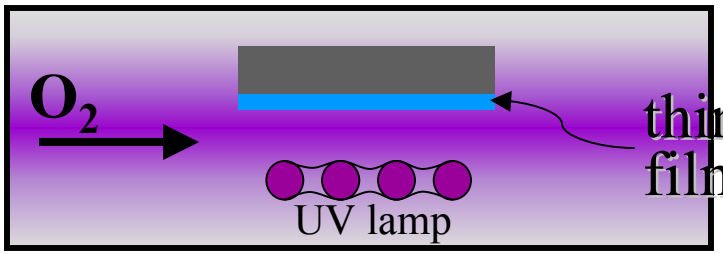
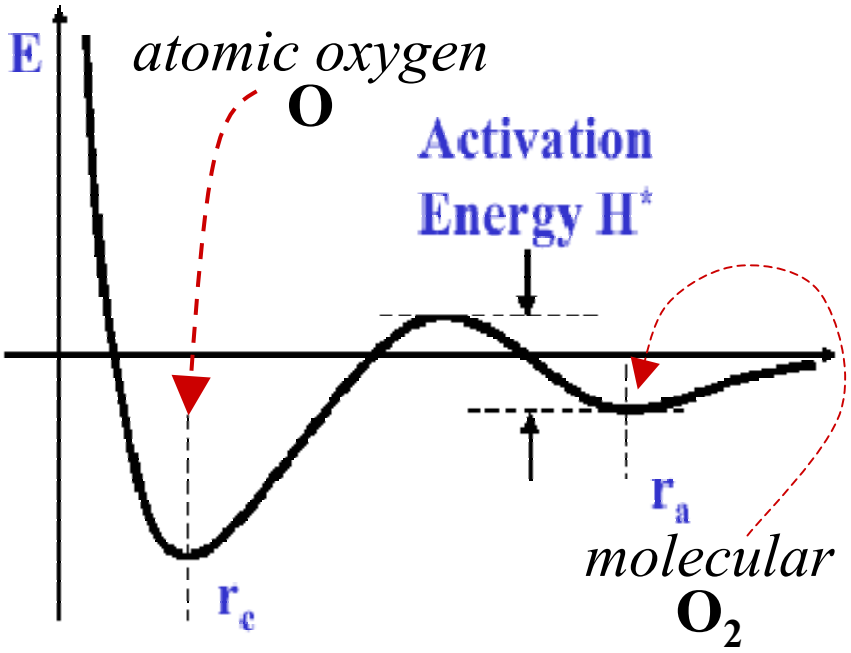
Growth of Metal Oxide Dielectrics: UV-Ozone Oxidation



UV light supplies atomic oxygen and ozone to surface through the following reactions:

$$O_2 + h\nu' \longrightarrow 2O$$
$$O + O_2 \longrightarrow O_3$$
$$O_3 + h\nu'' \longrightarrow O_2 + O$$



Benefits

- Low temperature
- No contamination
- Process simplicity

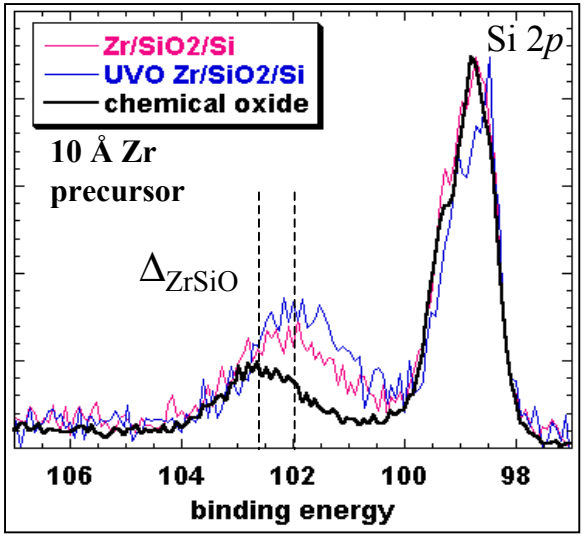
S. Ramanthan et al., APL 2001

UVO Metal Oxide Processing on a SiO_2 Surface

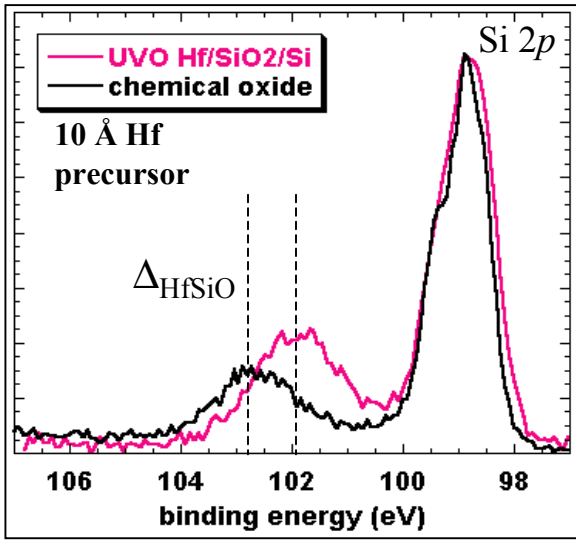
- **Because a metal precursor is deposited onto the substrate before the oxidation, an opportunity exists for reaction between the precursor and the substrate.**

- **XPS spectra of the Si 2*p* peak indicate a change in the chemical state of the SiO_2 present as native oxide on the substrate.**

- **Both hafnium and zirconium have greater oxygen affinities than Si and have a tendency to reduce SiO_2. through solid state reaction.**



$\Delta_{Zr\text{-}Si\text{-}O}$ = 0.64 eV



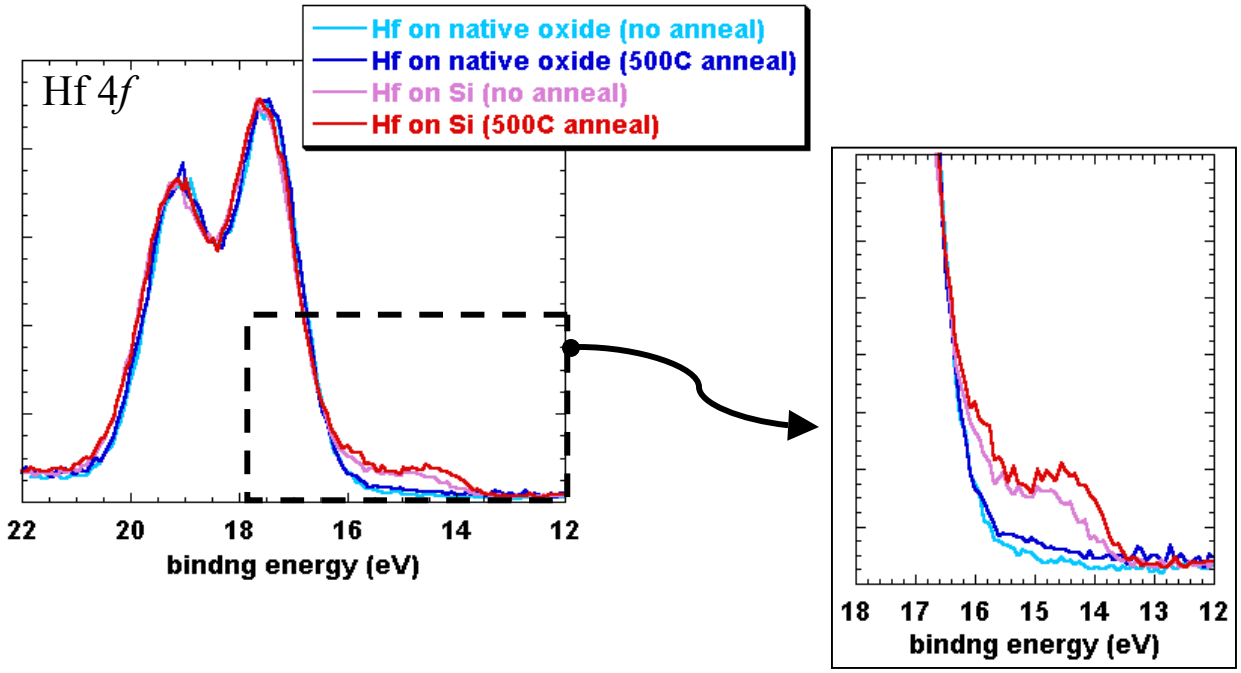
$\Delta_{Hf\text{-}Si\text{-}O}$ = 1.04 eV

Change in free energy for the oxidation reaction
$M_x + O_2 \rightarrow M_xO_2$
where M is a metal

	Zr	Hf	Si
ΔH^o	-1089 kJ/mol	-1222 kJ/mol	-910 kJ/mol

UVO Metal Oxide Processing on a Si (100) Surface

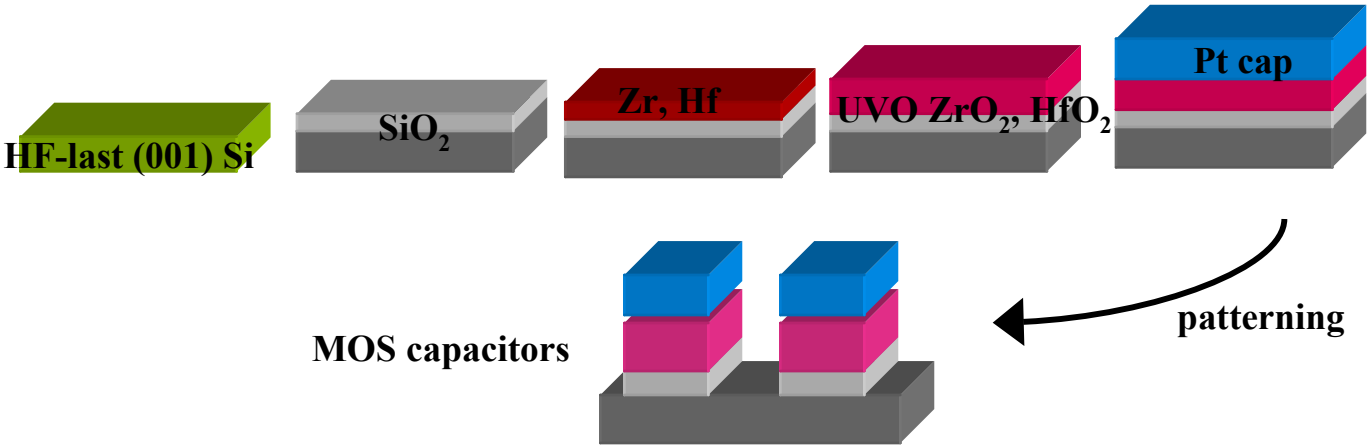
- **Deposition on bare Si leads to silicidation reaction as evidenced by Hf 4*f* XPS spectra**
- **Silicide does not oxidize during UV-ozone processing**
- **Presence of metallic phase at high-k/Si interface is not desirable for device applications**



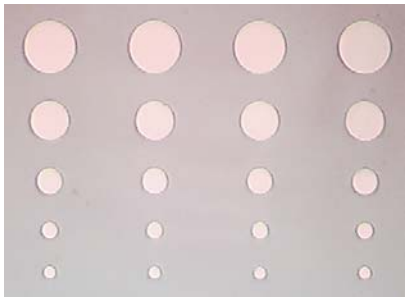
High-*k* / SiO_2 Gate Stack Grown *in-situ* by UV-Ozone Oxidation at 300 K

- **Electrical properties are measured using MOS capacitors**

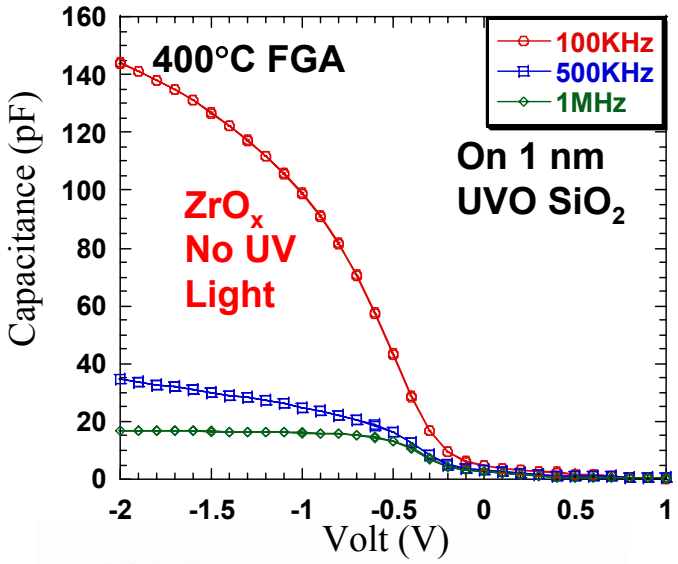
- **Metal electrodes are deposited *in situ* on the oxide preventing oxidation in atmosphere and incorporation of contaminants**

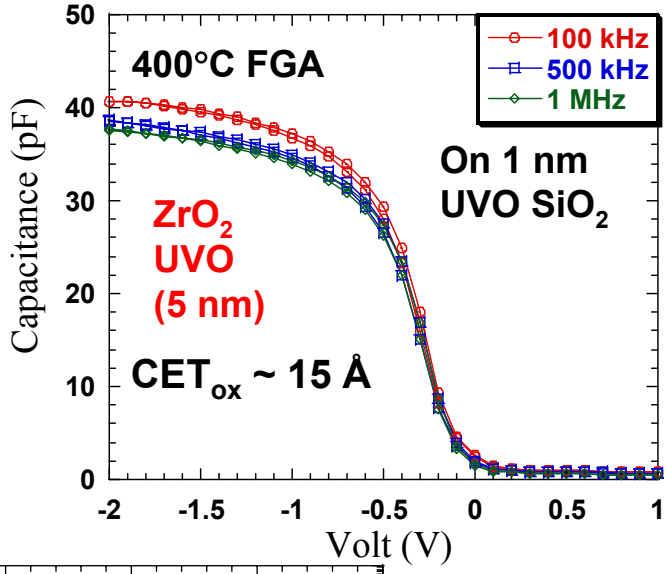


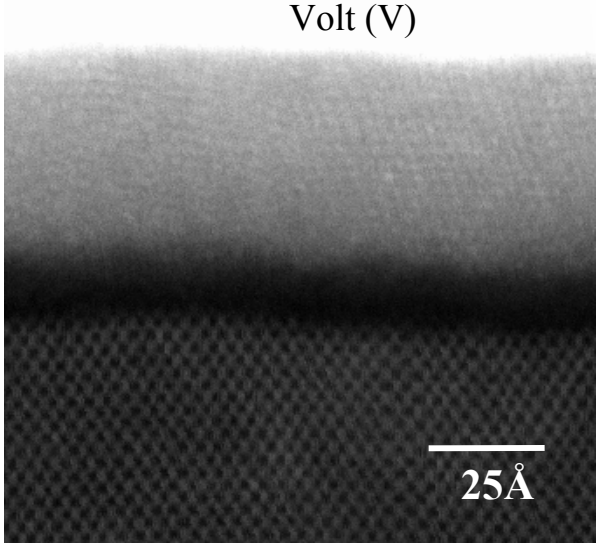
- **Capacitor structures are made through lithographic patterning and ion etching**
  Capacitor diameters(μm): 200, 150, 100, 66, 50

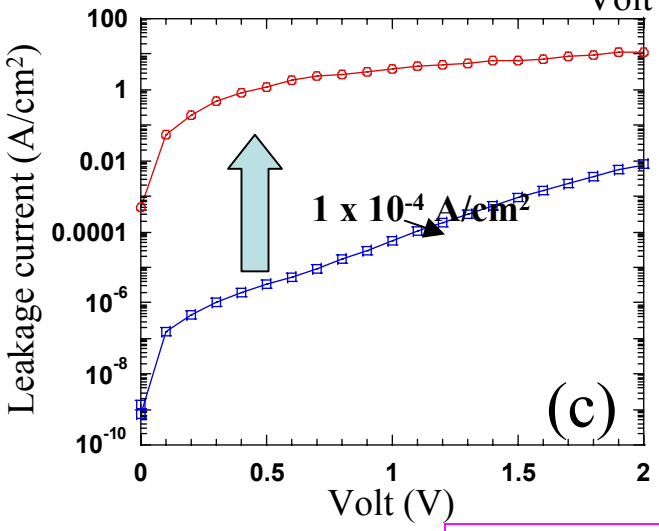


Dielectric Behavior: Oxygen Stoichiometry Effects







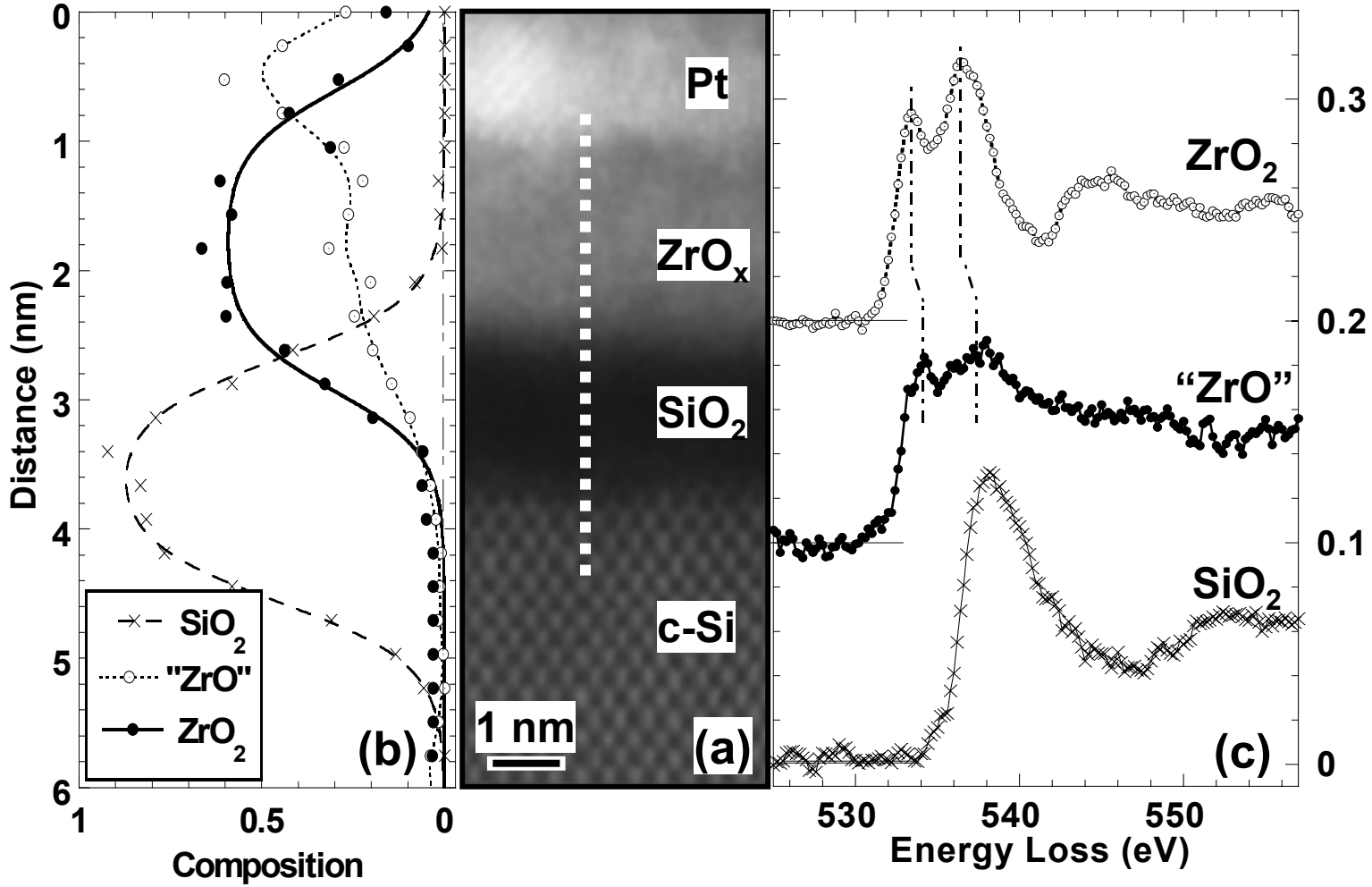


QM corrected EOT ~ 1 nm (Ramanathan, McIntyre, Guha and Gusev, **DRC 2002**)

Polycrystalline ZrO_2 film on thermal SiO_2/Si

S. Ramanathan et al., JAP 2002

Quantitative EELS Analysis: Partial Oxidation

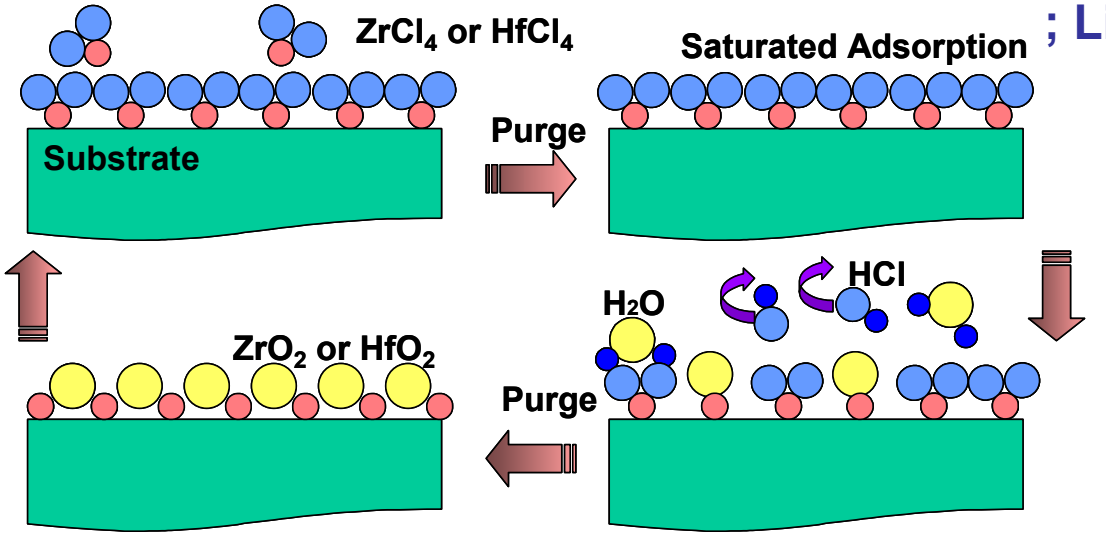


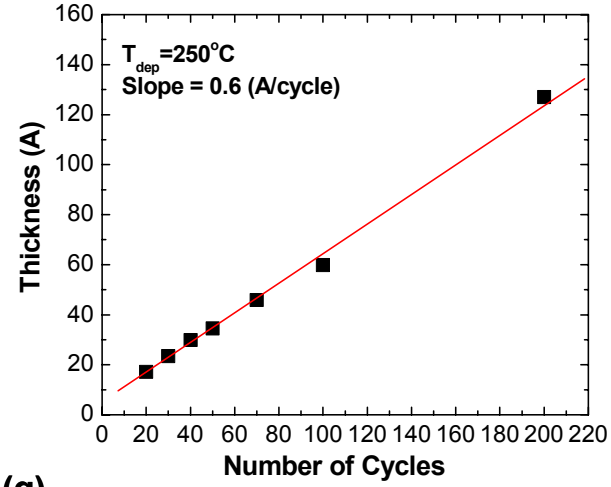
- Quantitative analysis of EELS O-K fine structure detects *additional* sub-stoichiometric ZrO phase

Philos. Mag. Lett. 2002

ALD (Atomic Layer Deposition)

- **Surface saturation controlled process**
- **Layer-by layer deposition process ; Linear sub-monolayer growth rate**

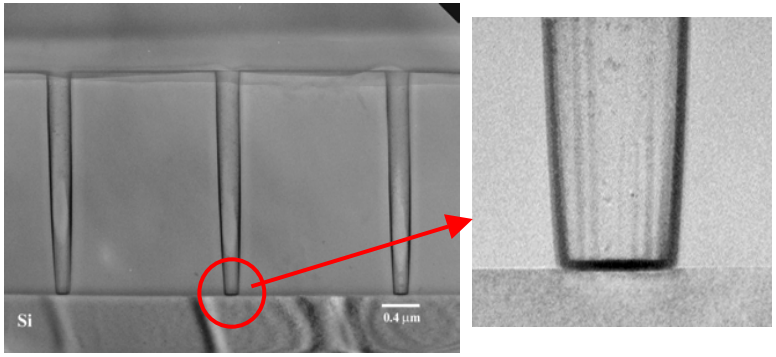


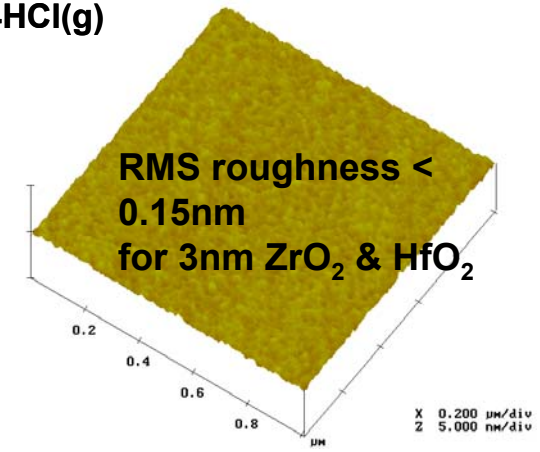


$ZrCl_4(ad.) + 2H_2O(g) \rightarrow ZrO_2(s) + 4HCl(g)$

$HfCl_4(ad.) + 2H_2O(g) \rightarrow HfO_2(s) + 4HCl(g)$

- **Excellent film quality and step coverage**





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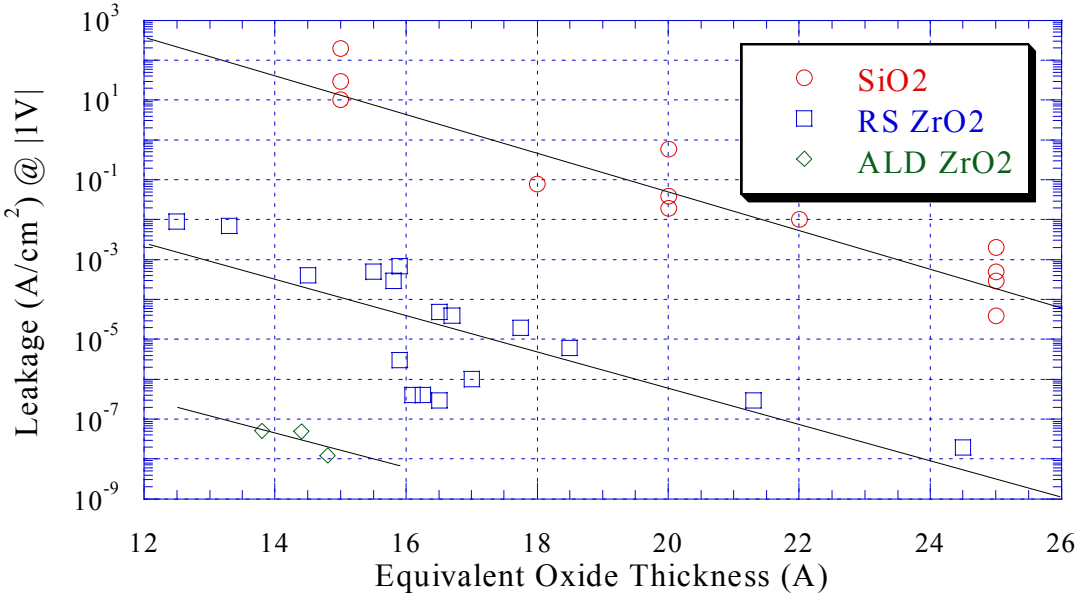
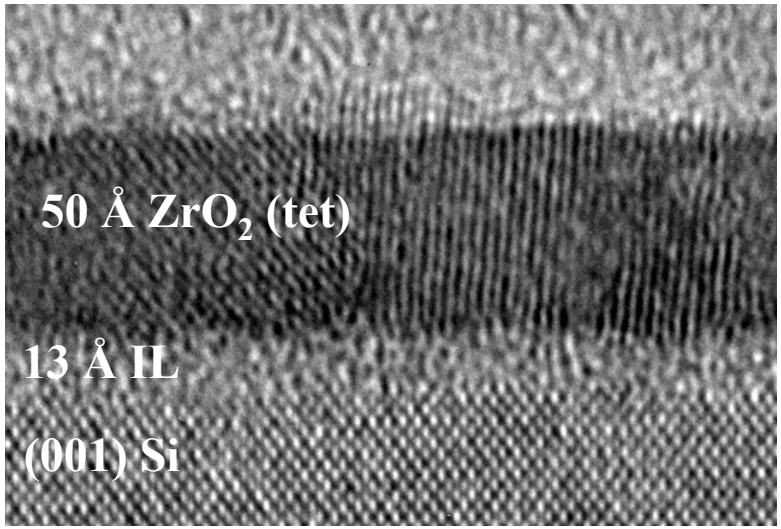
ALD ZrO_2 / Chemical Oxide Gate Stacks

Gate Leakage vs. EOT



XTEM Micrograph



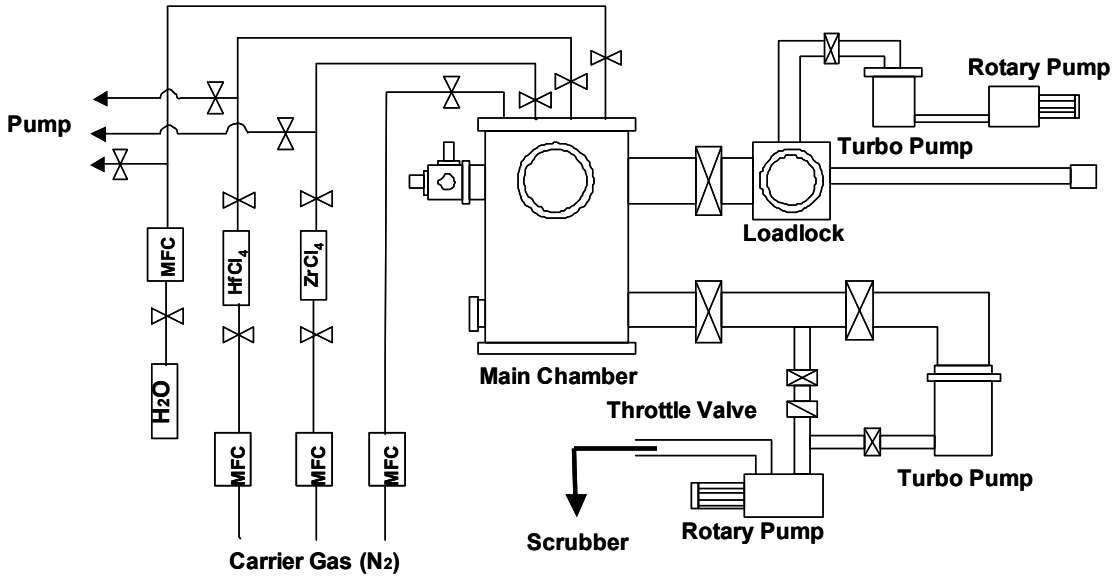
IL thickness > EOT ($\therefore \kappa_{IL} > \kappa_{SiO2}$)

- By using a chemical oxide passivation, EOT value of 1.2 nm with a leakage of ~ 10^{-6} A/cm^2 at $|V_G - V_{FB}| = 1$ V was achieved
- ZrO_2 thickness dependence of capacitance indicated $\kappa_{ZrO_2} \sim 26$, as expected
- Suggested 1.3 nm thick amorphous interface layer was not bulk-like SiO_2

C.M. Perkins et al., APL 2001

Experimental Conditions

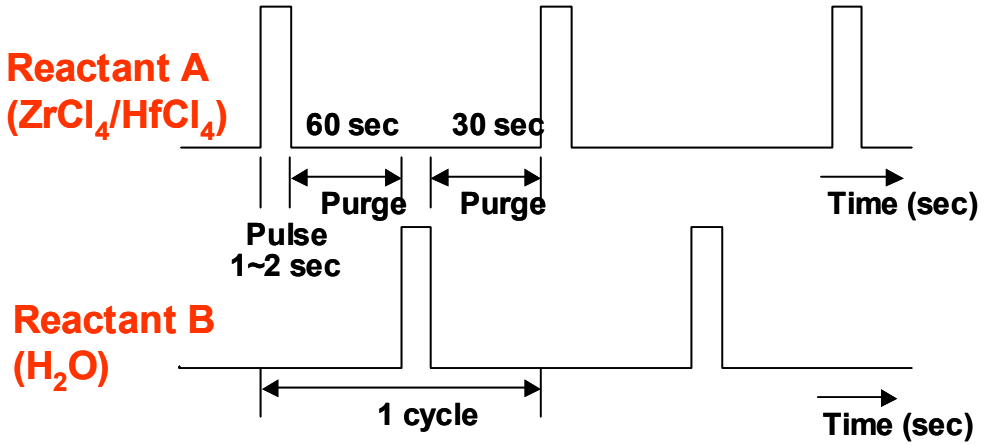
- **Deposition system**



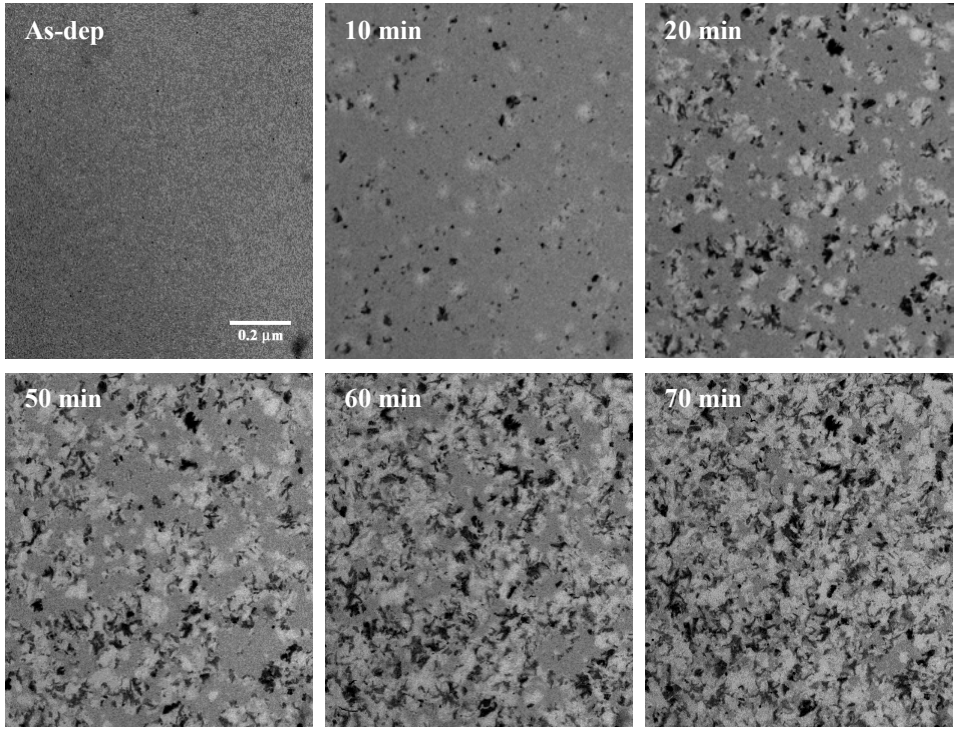
- Cold wall and resistive heating type ALD system
- Load-lock and high vacuum chamber (~10^{-8} Torr)
- Solid ($ZrCl_4$/$HfCl_4$) and liquid source (H_2O) delivery system

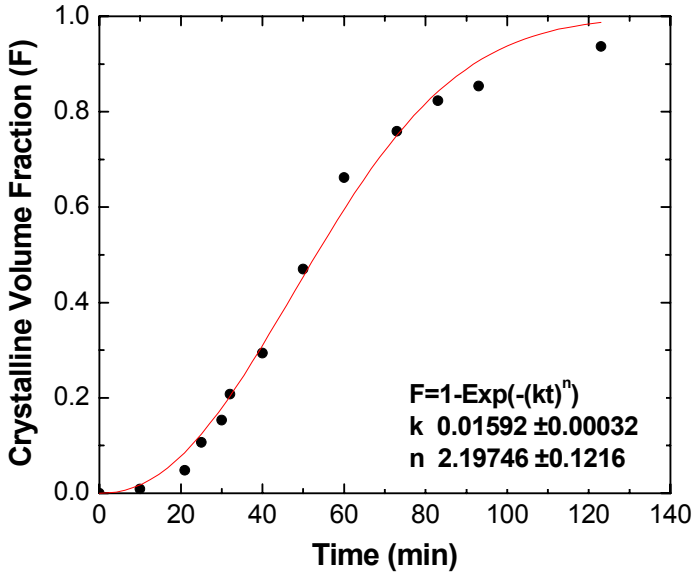
- **Deposition parameters**

- Process temperature : 300°C
- Process pressure : 0.5 Torr
- Source temperature :
  H_2O (liquid) = R.T.
  $ZrCl_4$/$HfCl_4$ (solid) = 150°C



In-Situ Crystallization Kinetics of ALD-HfO_2

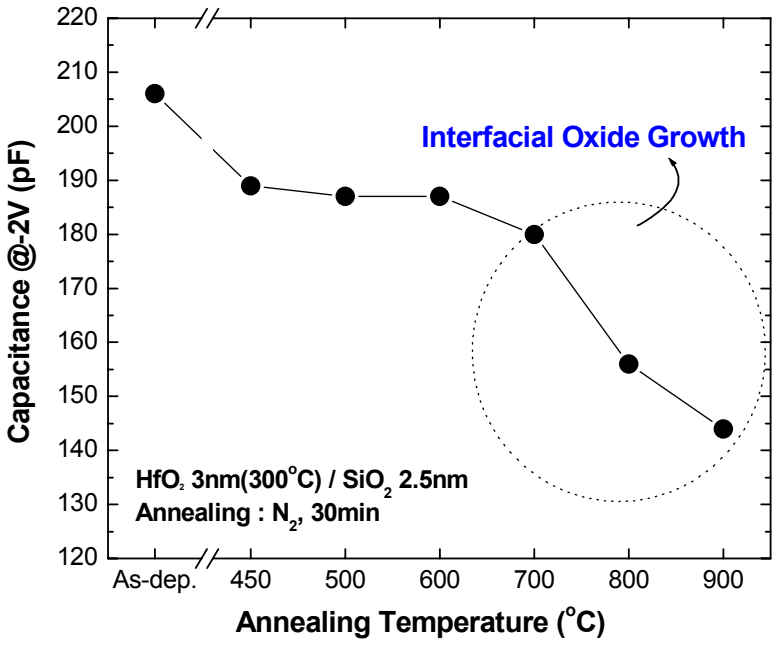


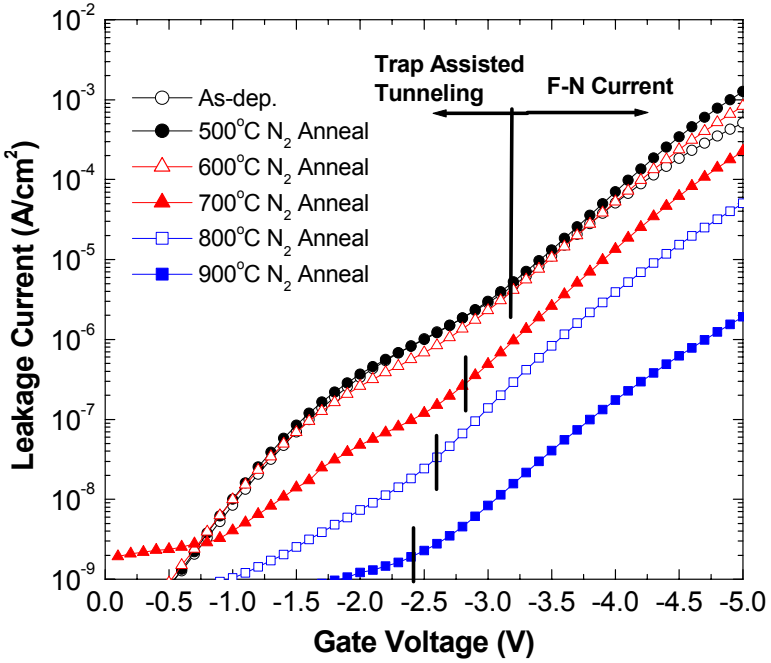


- In-situ anneal at 520°C using 30Å HfO_2 on 25Å thermal SiO_2.
- Preliminary analysis shows 2-D (radial) growth with decreasing nucleation rate.

Avrami isothermal transformation kinetics: $F=1-\exp(-(kt)^n)$ n~2.2

Effects of HfO_2 Crystallization on Electrical Properties (Thick Interfacial Oxide)





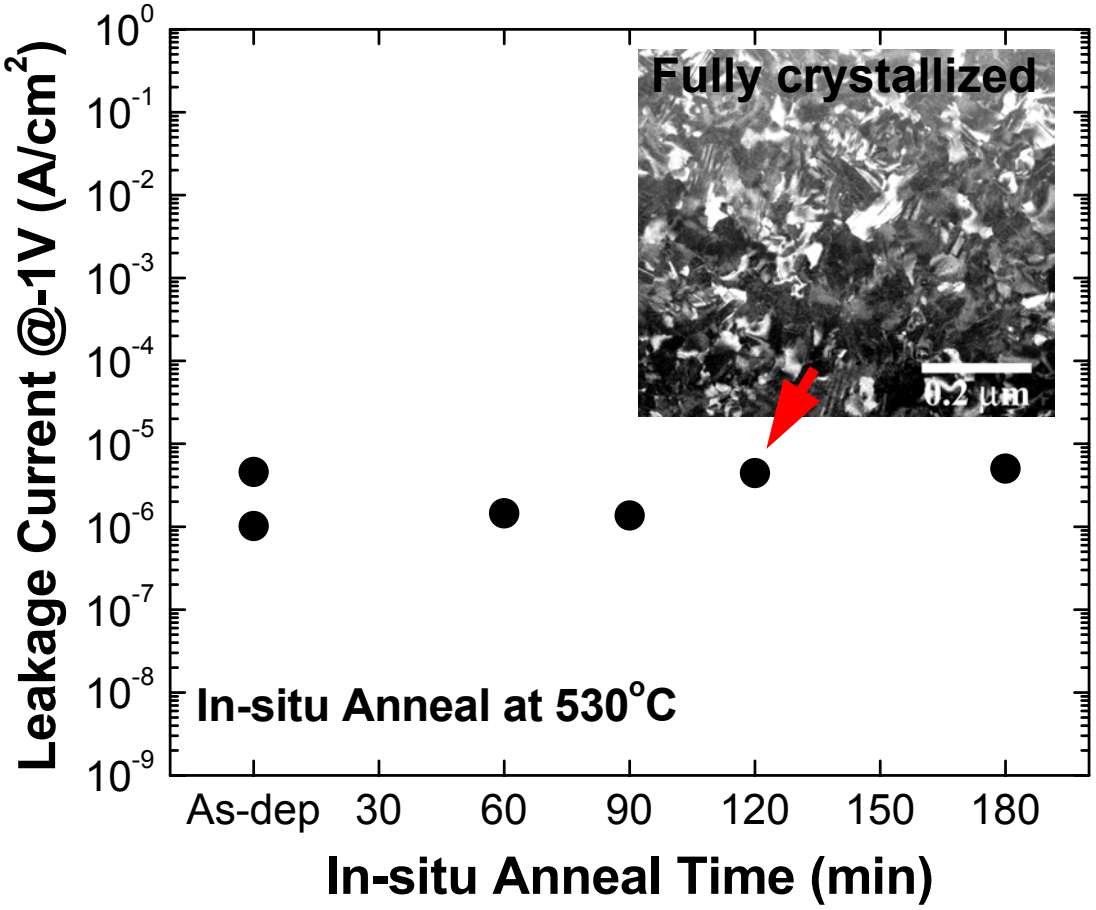
- **Sample structure : 3nm HfO_2 on 2.5nm SiO_2.**
- **After 700°C, capacitance decreases due to the interfacial oxide growth. ***
- **There was no significant increase in trap assisted tunneling leakage current resulting from crystallization.**

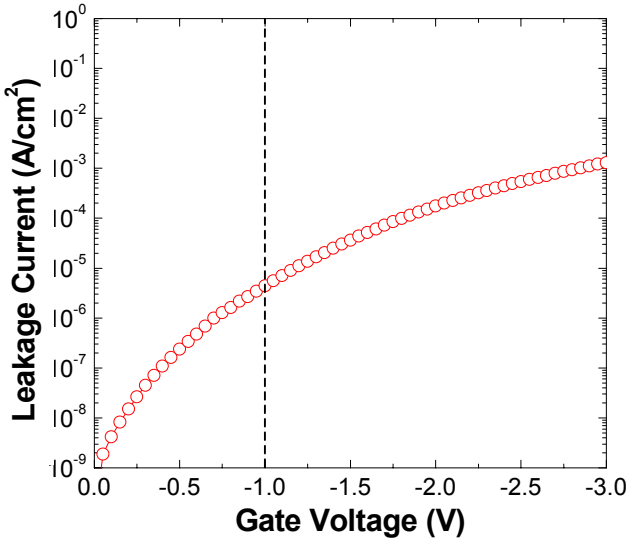
* Reagent-grade N_2 ambient contains ~ 1 ppm O_2.

H. Kim et al., APL, 2003

Effects of HfO_2 Crystallization on Electrical Properties (*In-situ* Annealing w/o interfacial oxide growth)

***In-situ* annealing after ALD-HfO_2 deposition to minimize interfacial oxide growth : 530°C, 1.3Torr with 500 sccm N_2 flow**





- **Sample structure : HfO_2 on 1.5 nm chemical SiO_2**
- **No significant leakage current change w/o interfacial oxide growth**

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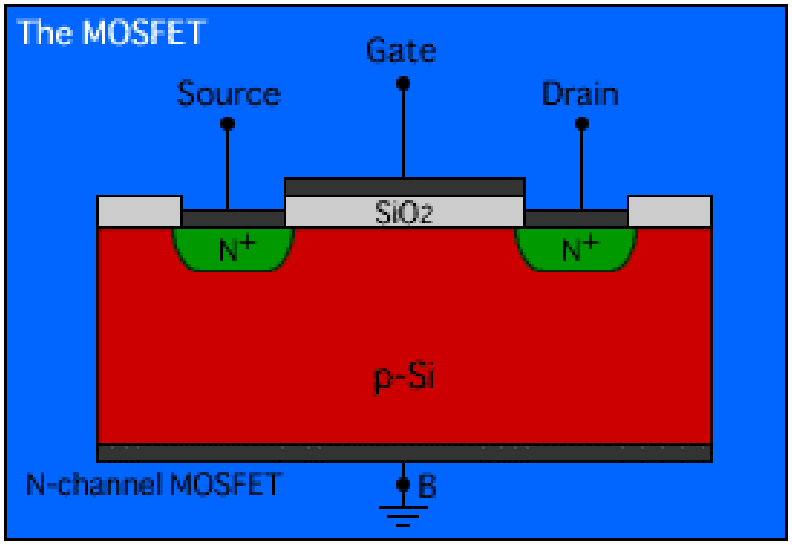
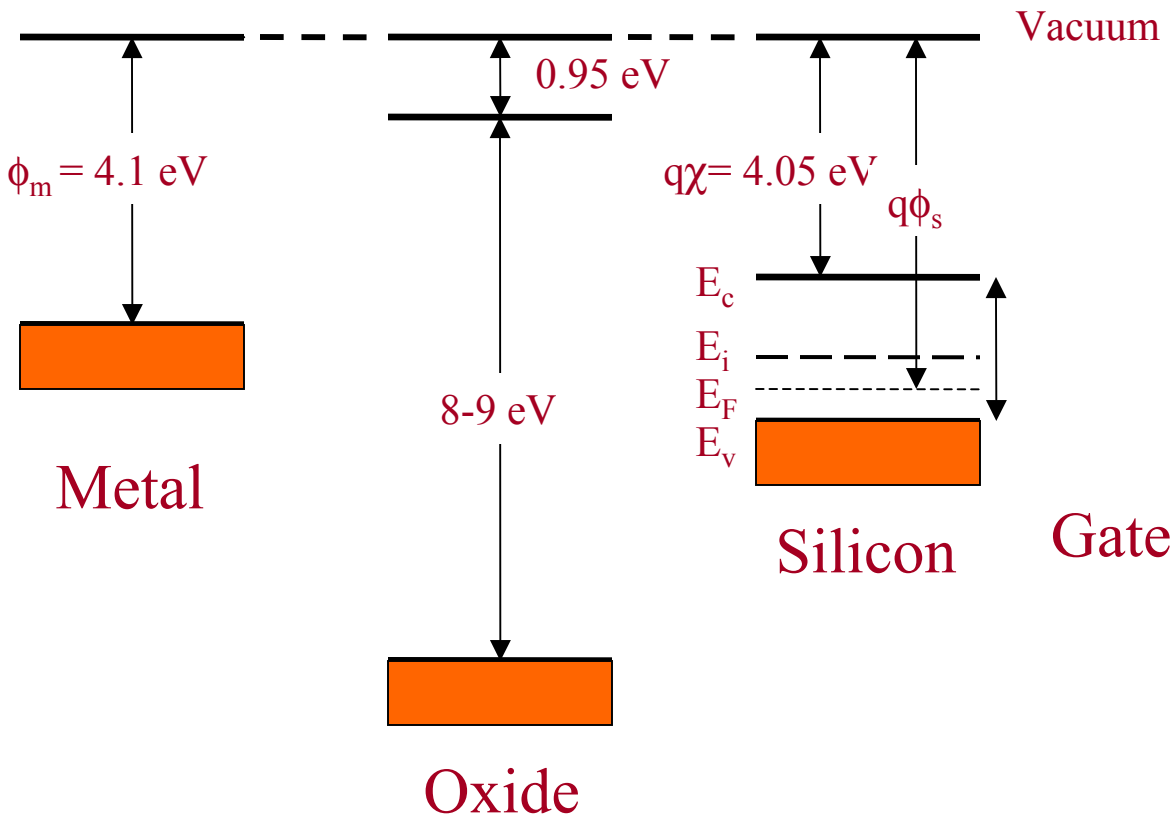
Current Technology: Poly-Si Gates



Advantages of Poly-Si:

- Self-aligned gate
- High thermal stability
- Excellent control over gate workfunction
- Single step operation
- Compatibility with gate oxide
- Ease of fabrication

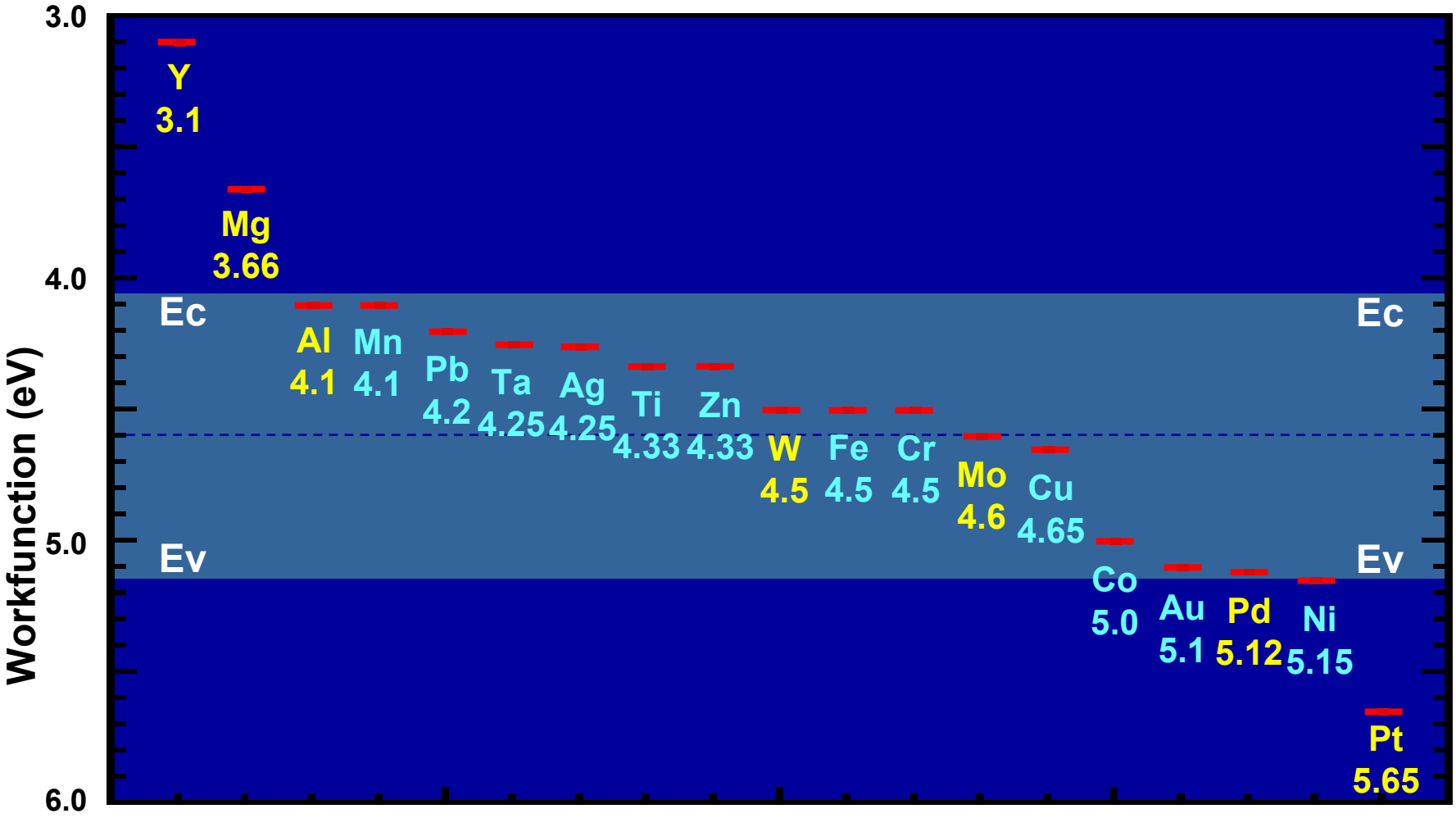
Band Diagram of an MOS Structure



Gate workfn requirements:
NMOS: ~4 eV
PMOS: ~5 eV

Schematic of the band diagram of a MOSFET

Electrical Workfunctions of Metallic Elements



Workfunction Engineering

Workfunction of Metals and Metal Nitrides:

Suitable for NMOS:

1. **Ti** (4.33)
2. **Al** (4.08)
3. **n+ poly** (4.17)
4. **Mn** (4.1)
5. **Ta** (4.25)
6. **V** (4.3)
7. **Zn** (4.33)

Suitable for PMOS:

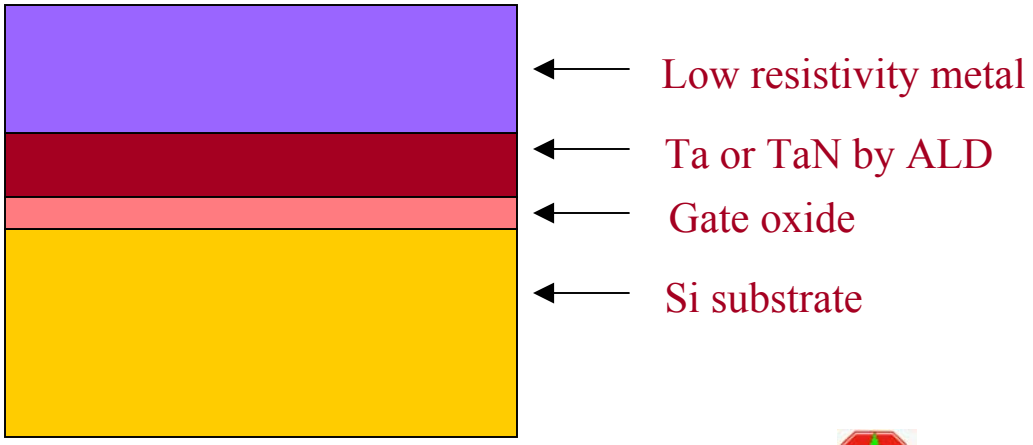
1. **Ru** (4.71)
2. **Rh** (4.98)
3. **Pt** (5.65)
4. **Co** (5.0)
5. **TaN** (5.2)
6. **p+ poly** (5.17)
7. **Mo** (4.6)

Our Focus:
Ta - NMOS
TaN - PMOS

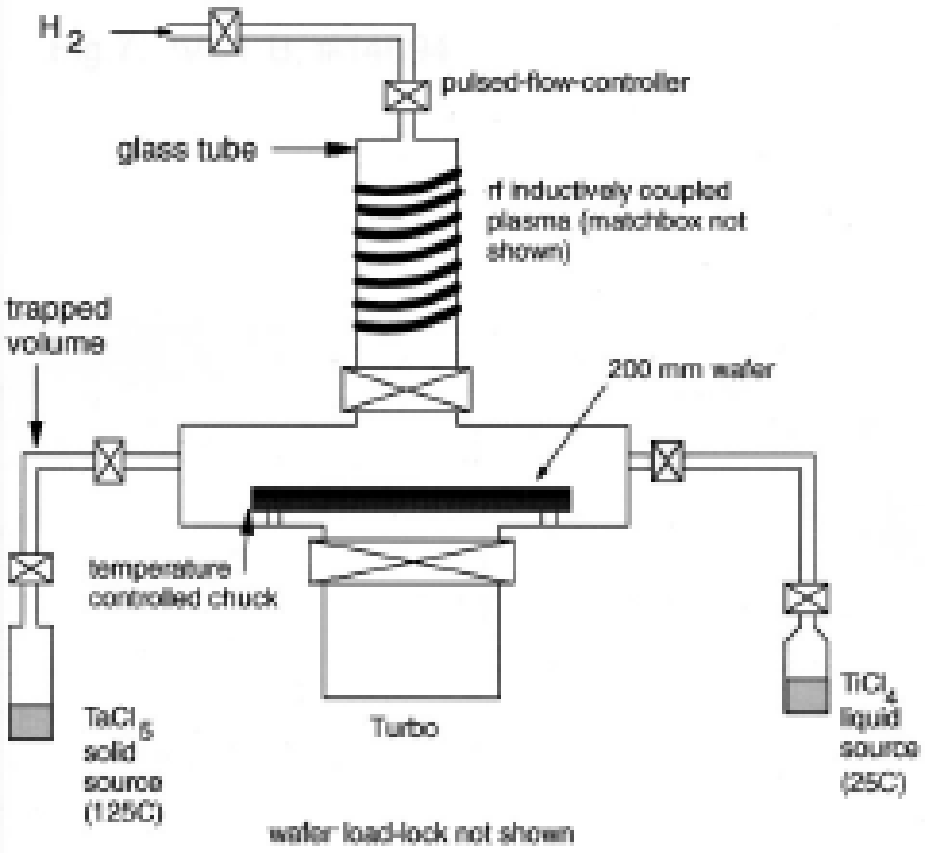
(values in brackets are workfn in eV)

Our Goal

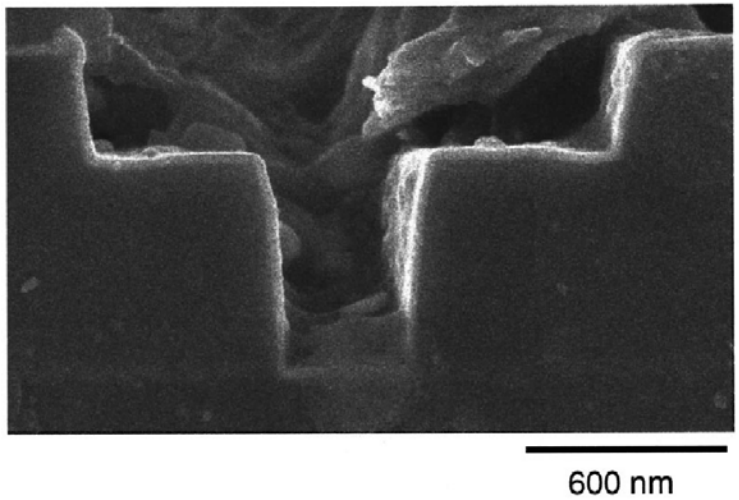
- Grow the high-k gate oxides by ALD using the Zr/Hf precursor
- In-situ gate deposition using tantalum precursor
- Deposit a thick, low resistivity metal layer to reduce the overall resistance of gate stack



ALD of Metal Thin Films – from Ta Liners to Ta - Based Gate Electrodes?



RF plasma ALD system for deposition of metal diffusion barrier liners for damascene Cu interconnect structures [*Rossnagel et al.* JVST B **18**(4) 2016 (2001)] .



- Ta and TaN have appropriate work-functions for CMOS gate electrodes
- In deeply scaled, fully-depleted channel devices, gate electrode workfunction will control device threshold voltage, rather than implanted channel dopant
- ALD may provide the needed capability to grow very thin metal layers with controlled workfunction on the gate stack

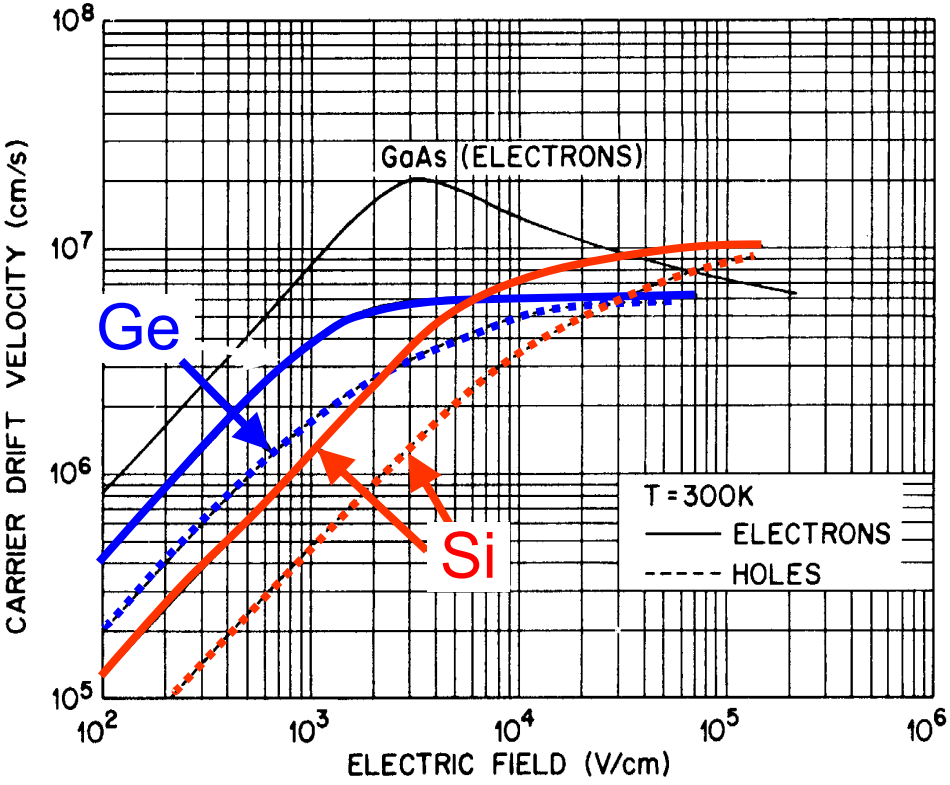
Outline

- Motivation and background
- Low thermal budget routes to high-*k* dielectric/semiconductor structures
  - ***UV-ozone oxidation (UVO) of ultra thin metal precursor layers***
  - ***Atomic layer deposition (ALD)***
- ALD as a tool for gate workfunction engineering
- UVO processing of ZrO_2 gate dielectric on Ge (100) substrates
  - ***Summary of electrical data from Pt/ZrO_2/Ge PMOSFET's***
  - ***Microstructure and interface abruptness***
- ALD of ZrO_2 and HfO_2 on Ge (100) substrates
  - ***Microstructure and dielectric/Ge interface***
- Conclusions

Benefits of Ge Substrates

Electronic Properties:

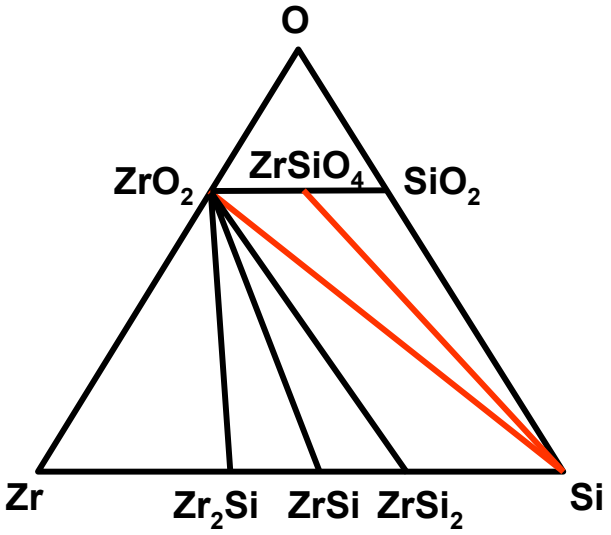
- More symmetric and higher carrier mobilities (low-field)
  - ⇒ More efficient source injection
    (due to lighter m^*)
  - ⇒ ↓ CMOS gate delay
- Smaller energy bandgap
  - ⇒ Survives V_{DD} scaling
  - ⇒ ↓ R with ↓ barrier height
- Lower temperature processing
  - ⇒ Compatible w/ 3D Integration



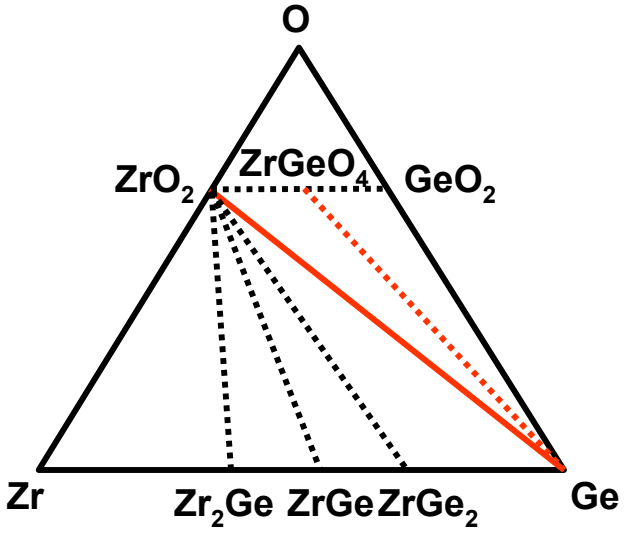
(Sze, *Phys. of Semicond. Devs. 2nd Ed.*, p.46, 1981)

Better performance may result from combining high-*k* gate dielectric and Ge substrate.

ZrO_2 on Si & Ge: Thermodynamic Considerations



700 ~ 900°C



600K

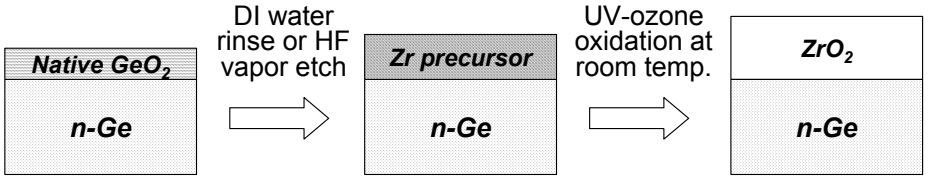
Ref.) Beyers et.al, J.Appl.Phys. ***56****, 147(1984)*

- **Although there is less available thermodynamic data for Ge compounds, phase equilibria are expected to be similar to Si case.**
- **GeO_2 is much less stable than is SiO_2 in the presence of Zr, Hf, and O_2.**

$\Delta G°_f(GeO_2)$ = -610 (kJ/mol)
$\Delta G°_f(SiO_2)$ = -921 (kJ/mol) @600K

1. $GeO_2 + Zr = Ge + ZrO_2$ (T=600K)
$\Delta G°$ = -520 kJ/mole
→ Zr-GeO_2 tie line cannot exist.
2. Formation energy of ZrO_2 is very large
[$\Delta G°(ZrO_2)$ = -1135 kJ/mole]
→ Tie lines tend to emanate from ZrO_2

Ge-Channel High-*k* Devices



(a) Native GeO_2 is unstable

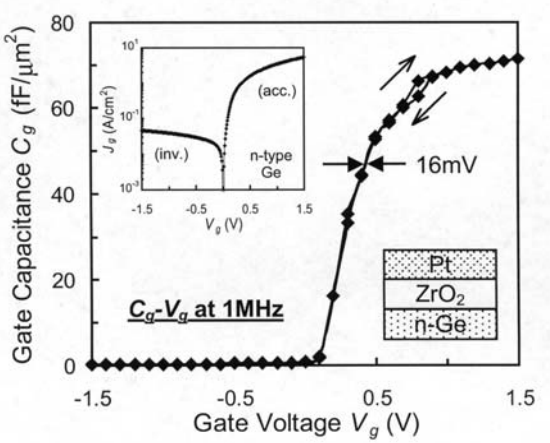
(b) Hydrophobic Ge surface

(c) Sputtering of 22-30 Å Zr

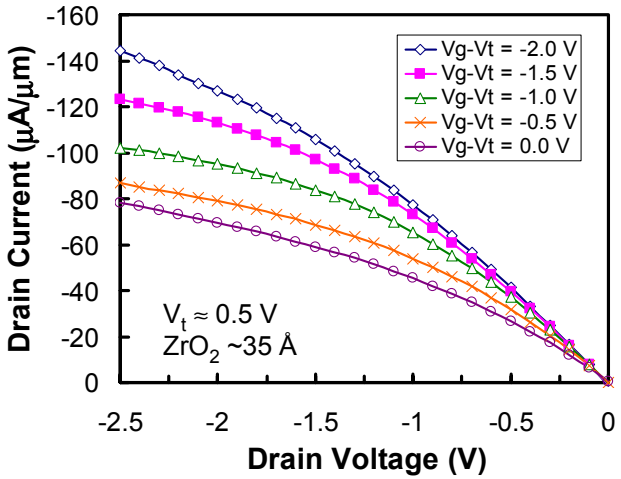
(d) Complete oxidation of Zr forming ZrO_2

(e) No interfacial oxide layer

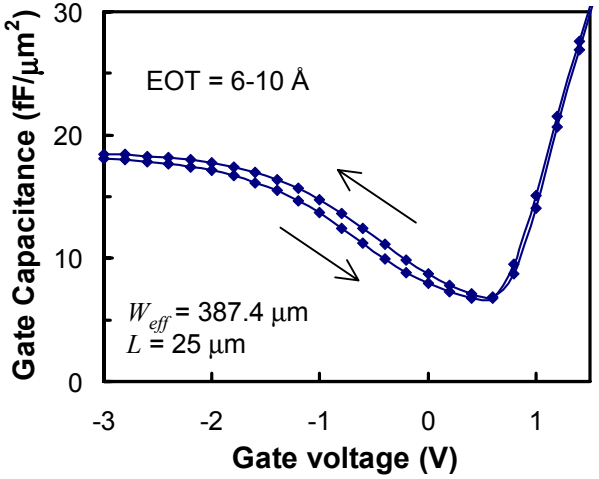
Interface layer-free room temperature ZrO_2 deposition by UVO oxidation of sputtered Zr precursor films



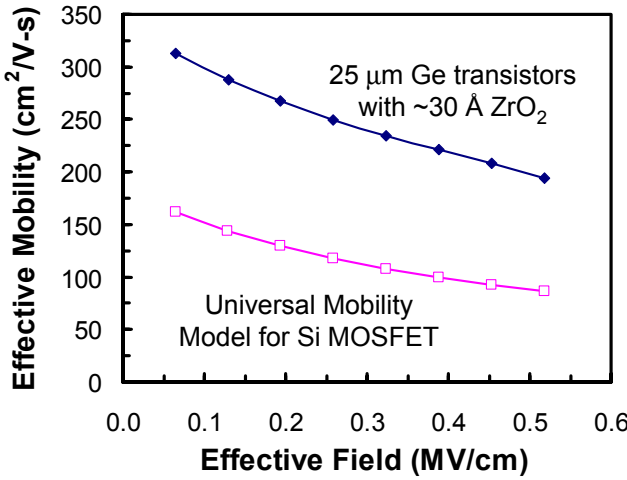
CV and JV characteristics of MOSCAP



Output characteristics of a 2 μm gate length Ge transistor (W_{eff} = 320.4 μm)



CV measurement (400 kHz) collected from a Ge transistor



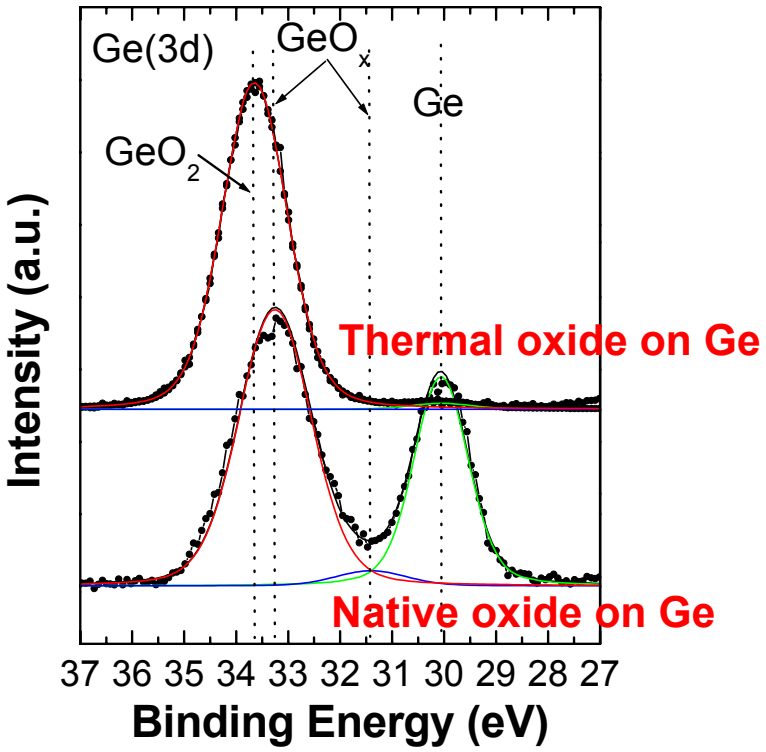
C.O. Chui et al. EDL, IEDM 2002

Krishna Saraswat (EE), McIntyre (MSE)

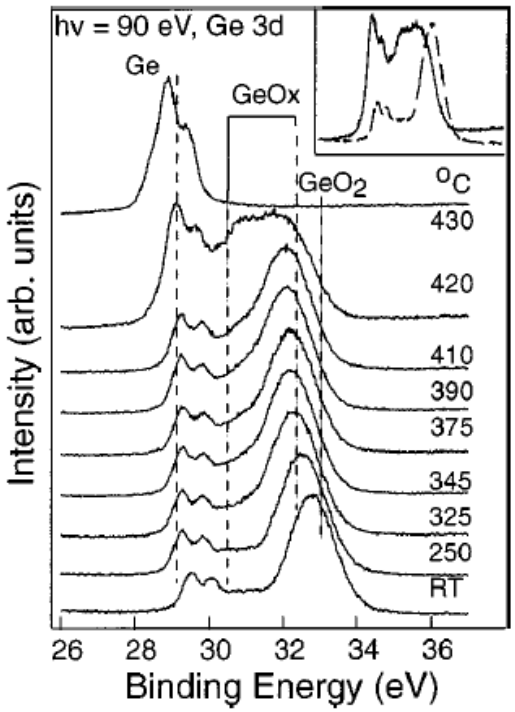
Stanford University

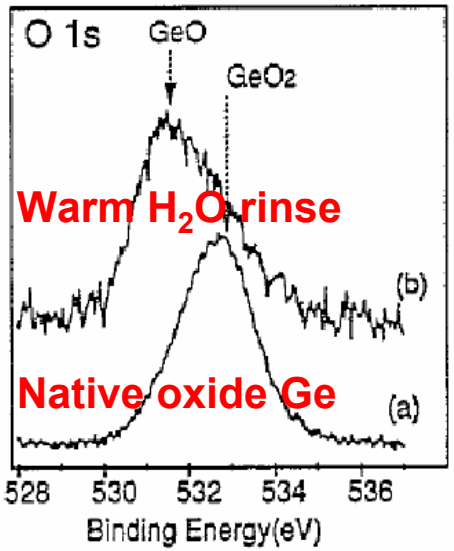
Surface Cleaning and Stability of GeO_x

Native Ge-oxide



Stability of Ge-oxide





(K. Prabhakaran, *Appl. Phys. Lett.* **76**, 2244 (2000) and *Surf. Sci.* **325**, 263 (1995)

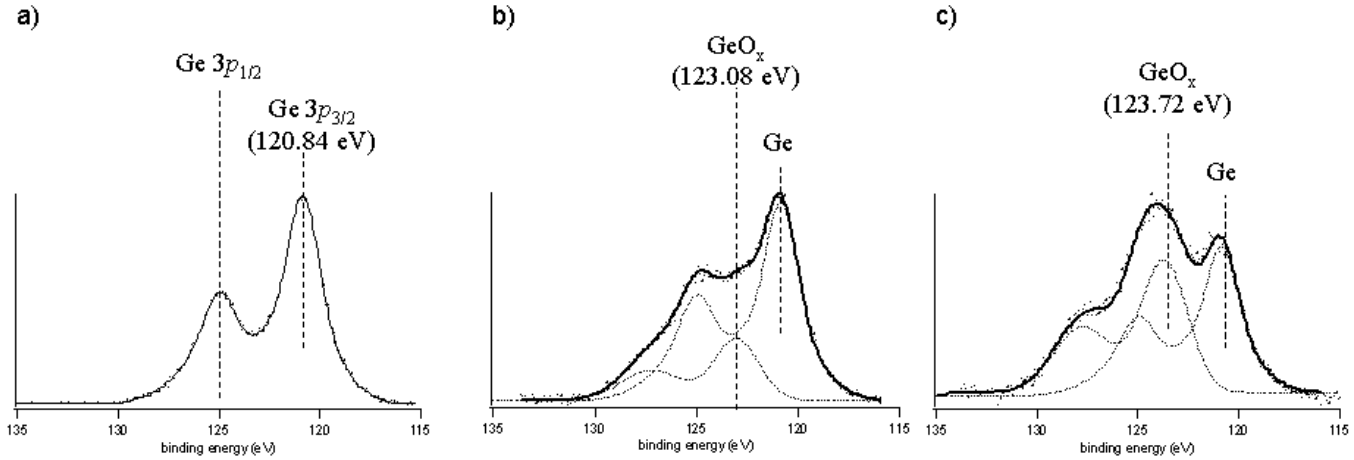
- Compared to thermally grown GeO_2, the native oxide also includes a Ge-suboxide component (GeO_x)

- Common hexagonal phase of GeO_2 is water soluble and volatile
- H_2O removes GeO_2 but not GeO
- GeO_x can be removed at T > 430 °C in vacuum

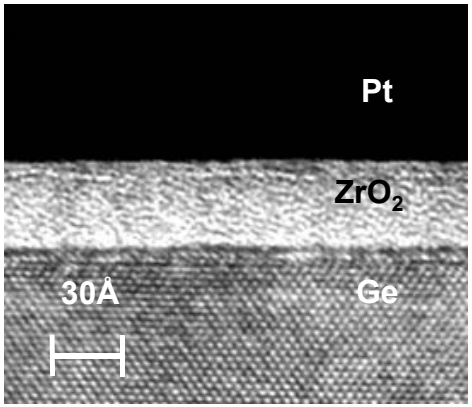
UVO ZrO_2/Ge Interface Structure

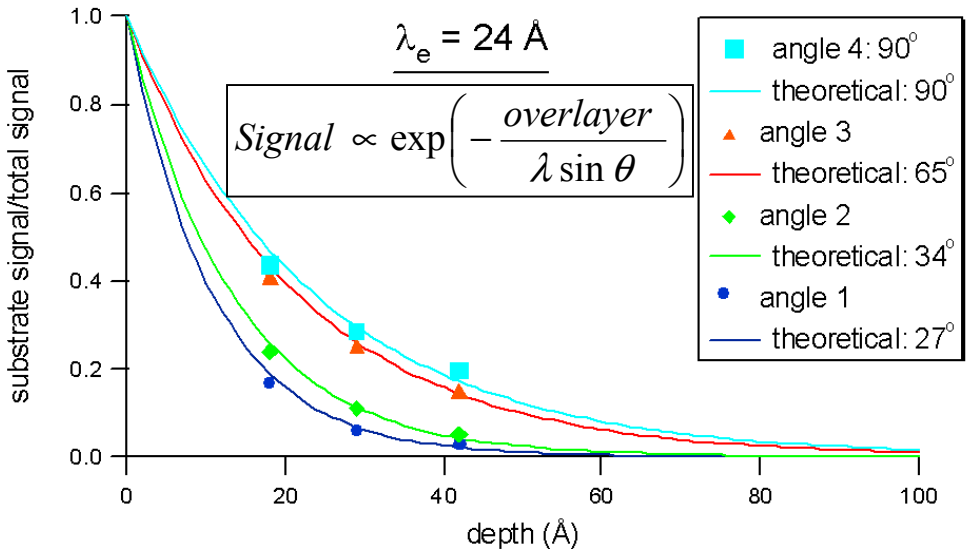
Determined standard spectra for a) sputter etched Ge, b) native Ge oxide, c) and UVO Ge oxide

- compared to 3p spectra obtained from ZrO_2/Ge samples



XTEM of functioning high-*k* MOSFET

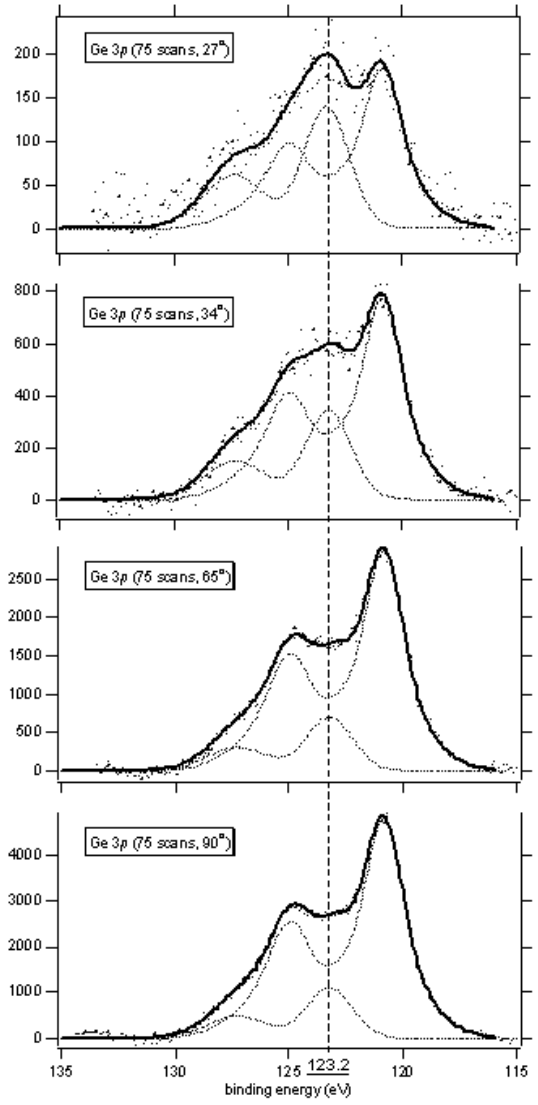




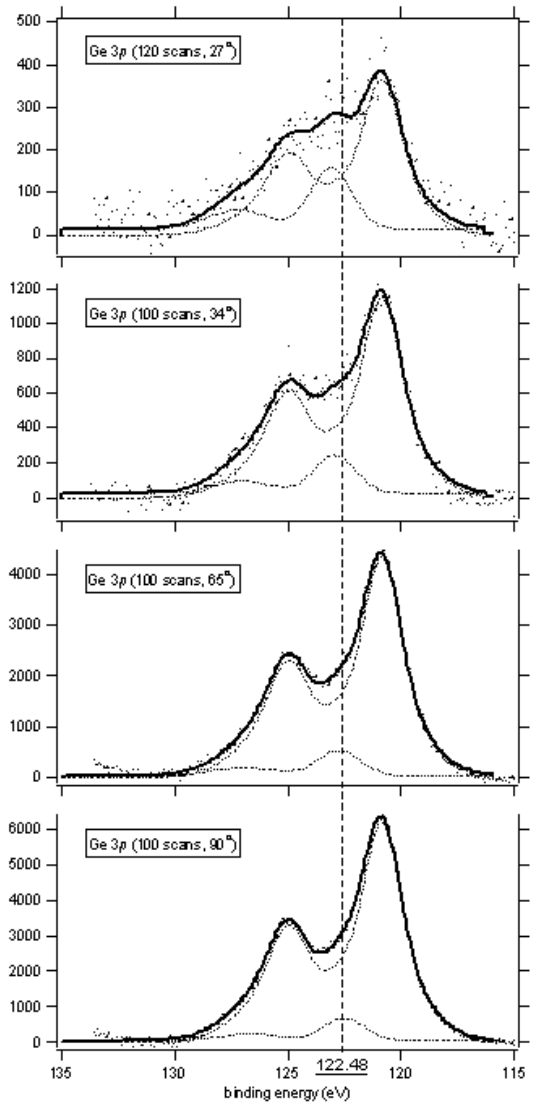
Calibrated take-off angles by measuring attenuation of Ge substrate peak for known overlayer thickness

Ge 3p Spectra for Different Angles

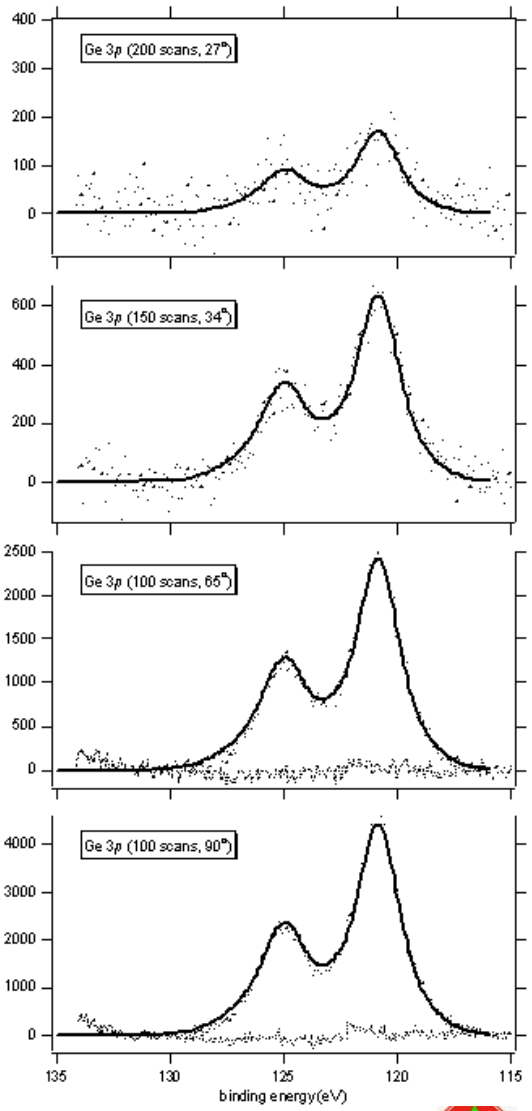
10 Å Zr, UVO



20 Å Zr, UVO



30 Å Zr, UVO



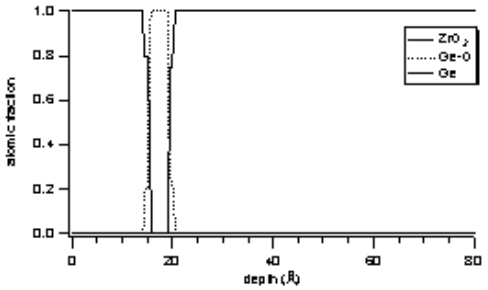
Samples capped with ~ 3 nm a-Si

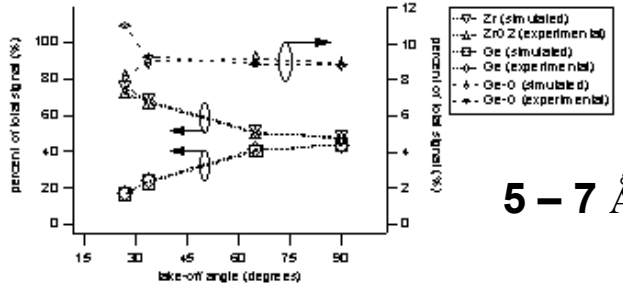
Stanford University

ARXPS Depth Profiles: ZrO_2/Ge Interface

10 Å Zr, UVO

UVO 300 K
1 hour

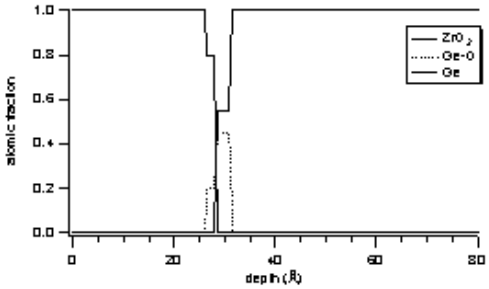


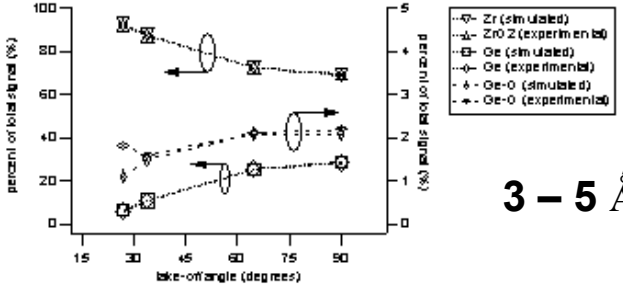


5 – 7 Å GeO_x

20 Å Zr, UVO

UVO 300 K
1 hour



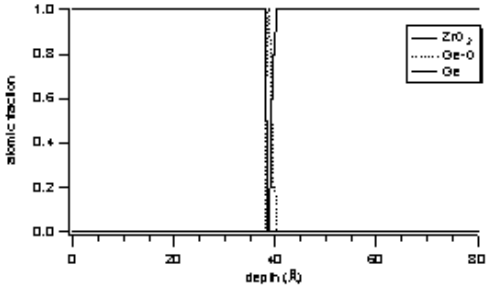


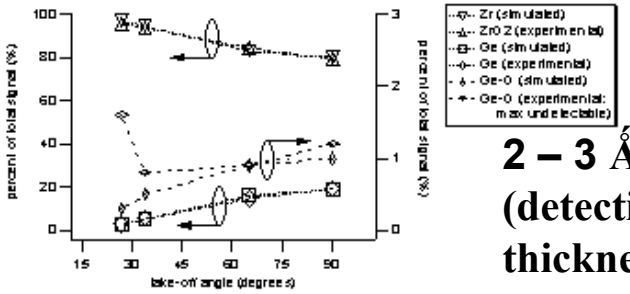
3 – 5 Å GeO_x

If precursor thickness/oxidation time is optimized, UVO gate stacks can be prepared on Ge with essentially no IL

30 Å Zr, UVO

UVO 300 K
1 hour





2 – 3 Å GeO_x
(detection limit for this ZrO_2 thickness)

Outline

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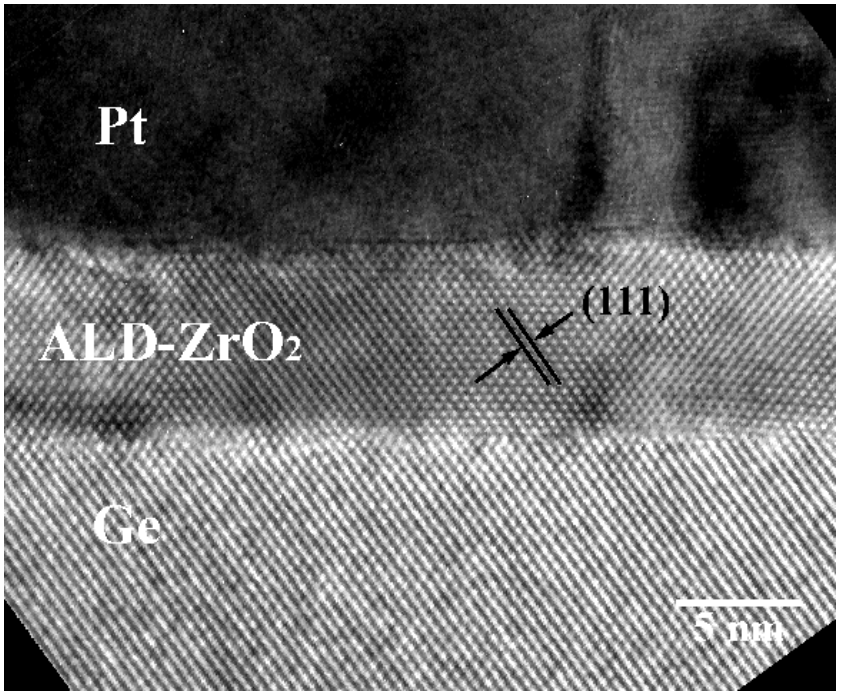
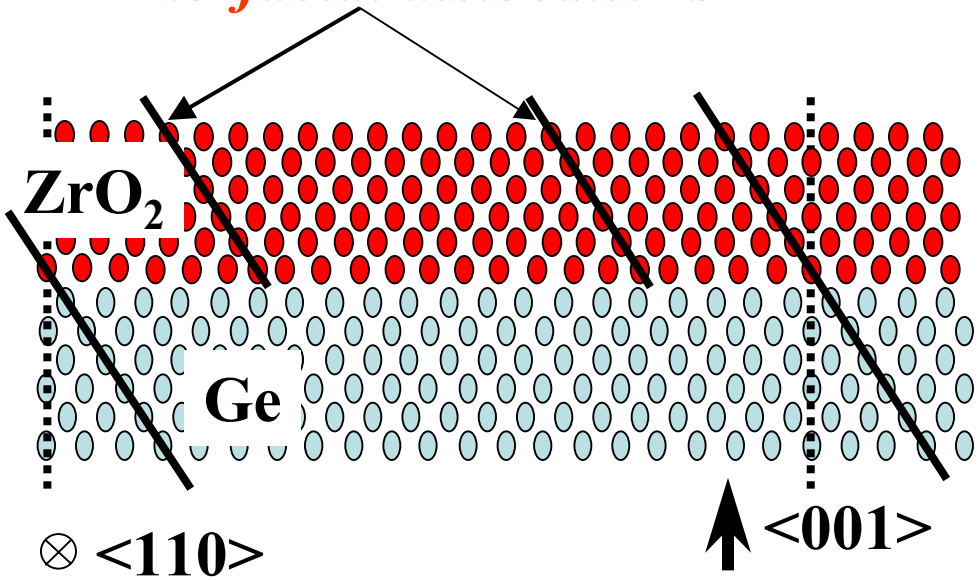
ALD-ZrO_2 on HF-last Ge Substrate



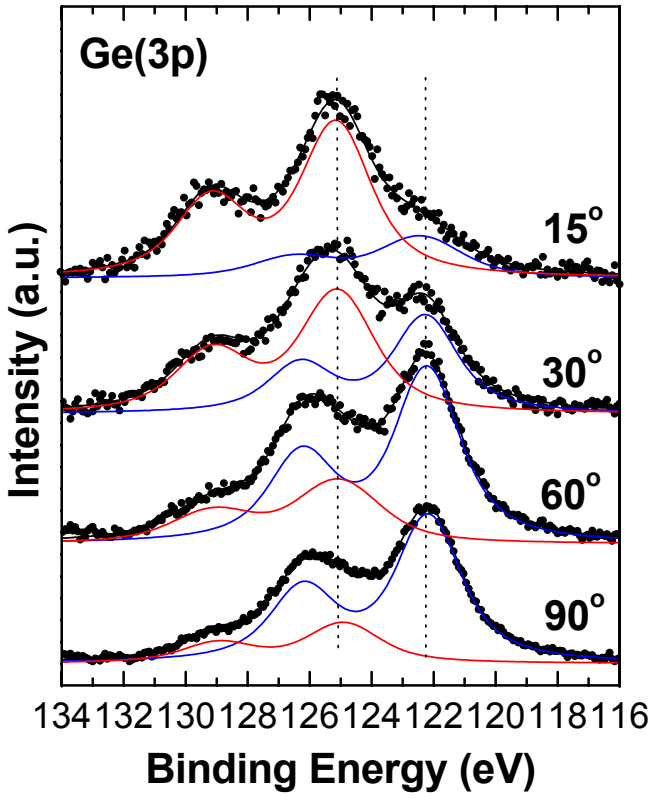


- ALD ZrO_2 (~ 55 Å thick) was grown on vapor HF cleaned Ge
- No interfacial layer detected; local epitaxial growth observed
- One interfacial dislocation per every ten (111) planes: consistent with substantial relaxation of biaxial misfit strain
  - *lattice mismatch between ZrO_2 and Ge (~10 %).*

H. Kim et al.
APL, accepted

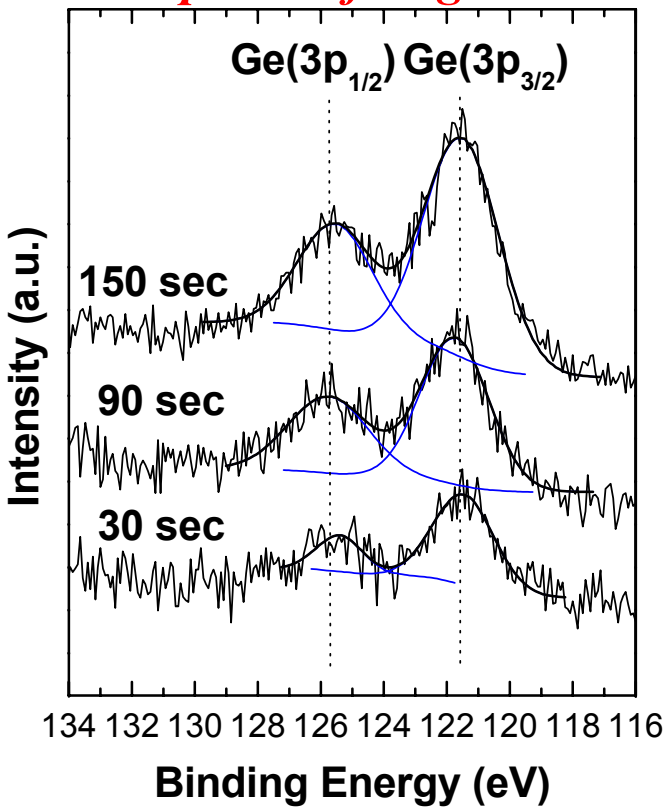
XPS Analysis of ALD ZrO_2 on Ge

Angle-Resolved XPS



ALD ZrO_2 (~15Å) on HF-last Ge

Depth Profiling XPS

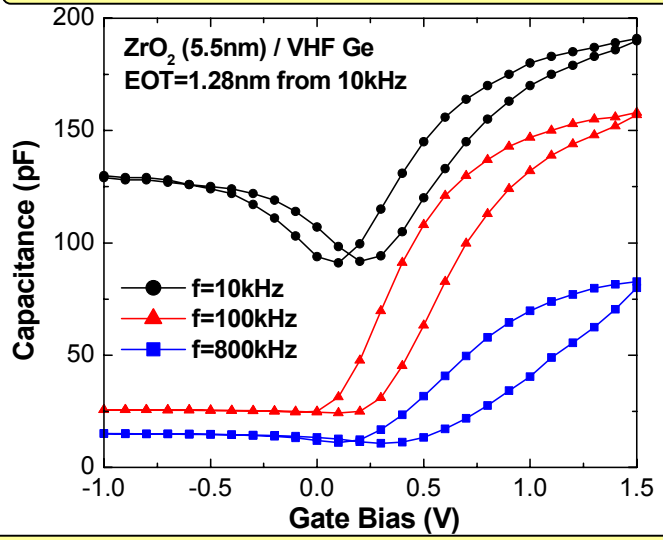


ALD ZrO_2 (~55Å) on HF-last Ge

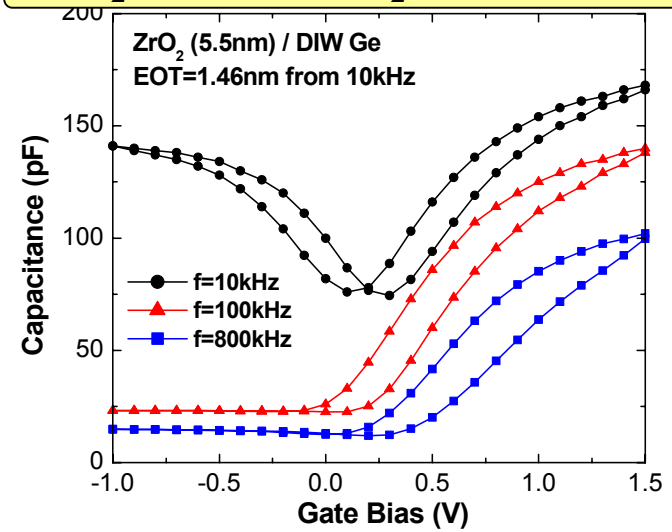
- Interfacial GeO_x is observed in thin ZrO_2 sample, appears to form by oxidation after air exposure of the uncapped ZrO_2 film
- No detectable interfacial oxide can be seen beneath thick ZrO_2

C-V Characteristics of ALD-ZrO_2 on Ge

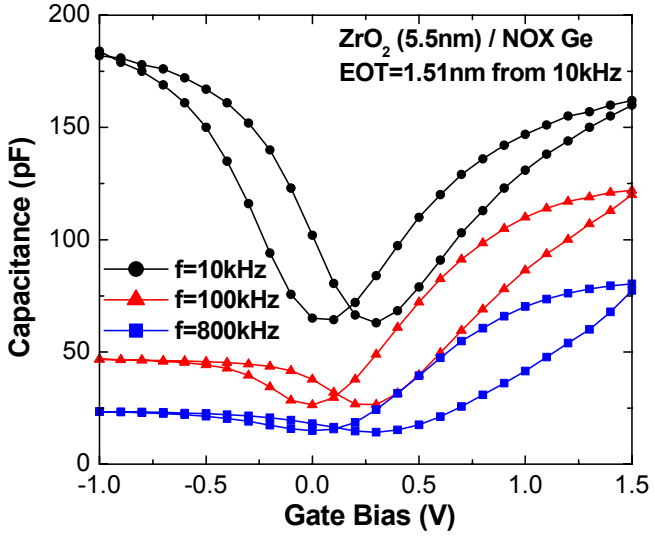
ZrO_2 (~55Å) on HF-cleaned Ge



ZrO_2 (~55Å) on H_2O-cleaned Ge

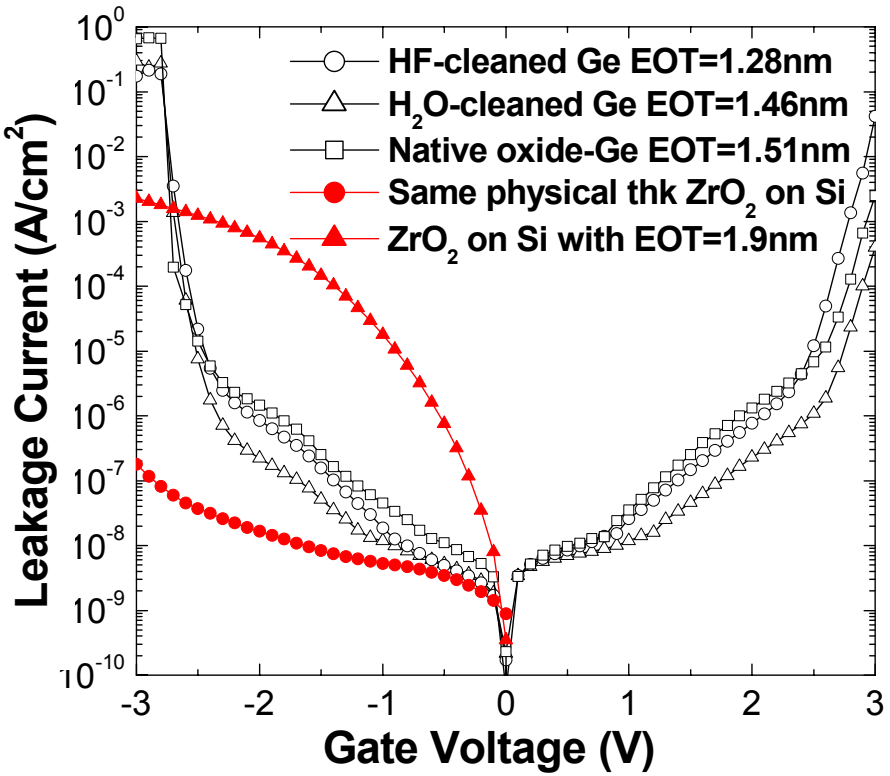


ZrO_2 (~55Å) on native oxide Ge



- EOT approximated from 10kHz CV data
- Large frequency dispersion creates uncertainty in precise EOT value
- Hysteresis and frequency dispersion may be caused by disorder at the ZrO_2/Ge interface (dislocations etc.).
- Inversion characteristics suggest increase in minority carrier generation (contamination?).

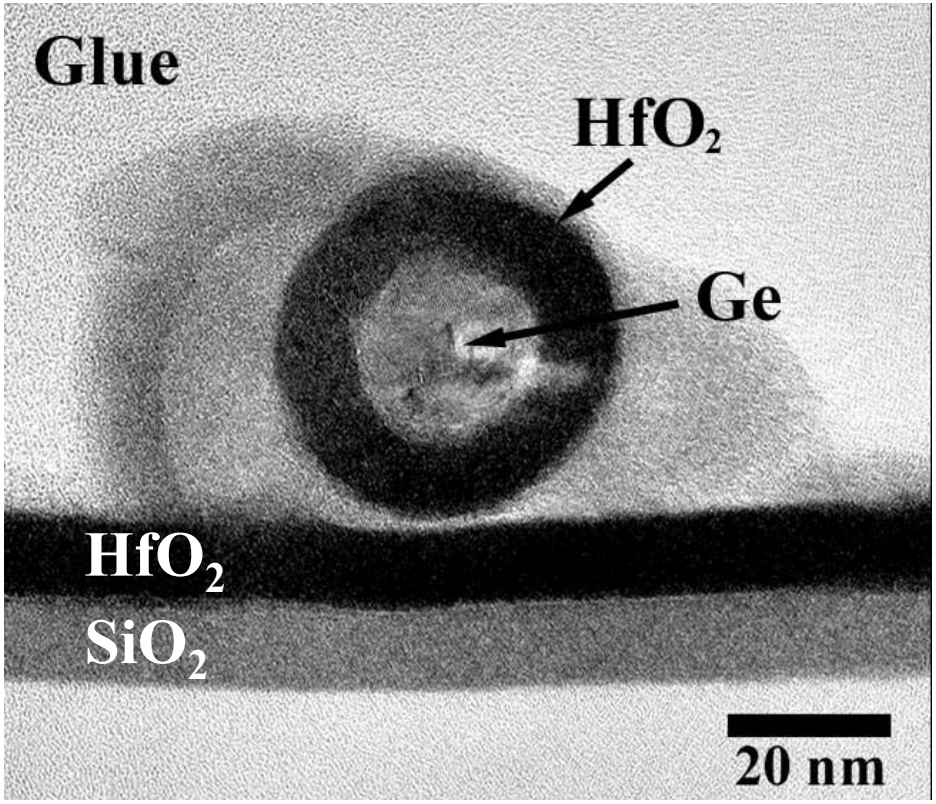
J-V Characteristics of ALD-ZrO_2 on Ge



- ZrO_2 on Ge samples show a slightly higher leakage current behavior compared to same physical thickness ZrO_2 on Si.
- Significantly lower leakage current than SiO_2 for the same EOT (absence of thick interfacial oxide layer).
- Low leakage current densities are encouraging from standpoint of device applications.

ALD of HfO_2 on Ge NW*

**CVD Ge NW growth courtesy of D. Wang and H. Dai, Stanford U.*



- **Conformal deposition – key attribute of ALD for dielectric passivation of NW surfaces for thin-body FETs**
- **Evidence that HfO_2 growth from $HfCl_4/H_2O$ precursors on Ge surface is in the true ALD regime**

Conclusions

- UVO processing of metal oxide gate dielectrics on SiO_2 from sputtered metal precursors results in a mixed metal oxide-SiO_2 layer
  - may contribute to the very low EOT of these gate stacks
- *In situ* annealing after ALD HfO_2 deposition shows HfO_2 crystallization does not contribute to an increase in leakage current density
- The surface adsorption limited film growth mechanism of ALD provides an opportunity for achieving area selectivity
  - we have demonstrated inhibition of HfO_2 ALD onto ODTS-passivated SiO_2
- UV-ozone oxidation of ultra thin Zr films has been used to prepare high-*k*/Ge PMOSFETs with hole mobilities ~ 2x that achievable in SiO_2/Si devices
- By controlling the metal precursor thickness and oxidation conditions, UVO metal oxide processing can produce essentially interface layer-free gate stacks on Ge
- ALD ZrO_2 on HF-last Ge exhibits local epitaxy (cube-on-cube relationship)
  - no interface GeO_x layer detected by XPS or TEM
- Low leakage current densities observed for ALD ZrO_2 on HF-last Ge suggest there is no intrinsic leakage problem for ZrO_2/Ge gate stacks