Novel Deposition Processes for High-k Gate Stacks on Silicon and Germanium Substrates

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Sept 18, 2003
• Motivation and background

• Low thermal budget routes to high-\(k\) dielectric/semiconductor structures
  - \textit{UV-ozone oxidation (UVO) of ultra thin metal precursor layers}
  - \textit{Atomic layer deposition (ALD)}

• ALD as a tool for gate workfunction engineering

• UVO processing of ZrO\(_2\) gate dielectric on Ge (100) substrates
  - \textit{Summary of electrical data from Pt/ZrO\(_2\)/Ge PMOSFET’s}
  - \textit{Microstructure and interface abruptness}

• ALD of ZrO\(_2\) and HfO\(_2\) on Ge (100) substrates
  - \textit{Microstructure and dielectric/Ge interface}

• Conclusions
Future Device Technology

- New structures
- New materials
- New deposition processes

![Bulk CMOS](image1)

![FD SOI CMOS](image2)

![Double-Gate CMOS](image3)

![Vertical MOS](image4)

After Peercy, P.S, IEEE1998

<table>
<thead>
<tr>
<th>Number of New Materials</th>
<th>Si</th>
<th>P</th>
<th>B</th>
<th>As</th>
<th>O</th>
<th>N</th>
<th>Al</th>
<th>WSi₂</th>
<th>TiN</th>
<th>TiSi</th>
<th>W</th>
<th>Cu</th>
<th>None</th>
<th>F</th>
<th>SiOF</th>
<th>Ta₂O₅</th>
<th>CoSi₂</th>
<th>D-Cu</th>
<th>TaSiN</th>
<th>SOI</th>
<th>BST</th>
<th>RuO₂</th>
<th>CaF₂</th>
<th>CaF₂</th>
<th>Organic</th>
<th>NiSi</th>
</tr>
</thead>
<tbody>
<tr>
<td>3+</td>
<td>2</td>
<td>1.2</td>
<td>0.8</td>
<td>0.5</td>
<td>0.35</td>
<td>0.25</td>
<td>0.18</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
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</tbody>
</table>
Physical Limits of SiO₂ Gate Dielectrics

- EELS O-K edge spectra recorded point by point across a gate stack containing a thin gate oxide.
  D. A. Muller et. al., *Nature*, 399, 758-761 (1999)

- Bulk SiO₂ properties (e.g. large bandgap) lost for films $\leq 8 \, \text{Å}$ in thickness
Gate Dielectric Technology Evolution

Transistor Drive Current

Today

1.5 nm SiO₂ \( \kappa \sim 4 \)

Si

Near future

EOT > 1 nm

Si₃N₄ \( \kappa \sim 8 \)

Long term

EOT < 1 nm

\( \kappa \sim 20 \)

Transistor Drive Current

\[ I_D \propto g_m \propto \frac{\kappa}{\text{thickness}} \]

Year of Introduction

# of Transistors per Chip


10³ 10⁴ 10⁵ 10⁶ 10⁷ 10⁸

In 1997, a gate oxide was 25 silicon atoms thick.

In 2012, a gate oxide will be five silicon atoms thick.
Desirable High-\(k\) Gate Dielectric Properties

<table>
<thead>
<tr>
<th>Material Properties</th>
<th>Electrical Properties</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\kappa &gt; 15); uniform</td>
<td>Equivalent (T_{\text{ox}} &lt; 1) nm</td>
</tr>
<tr>
<td>Thermally stable on Si (no need for barrier layer)</td>
<td>Low leakage current at the same equivalent (T_{\text{ox}})</td>
</tr>
<tr>
<td>No reaction with electrode (stop B penetration if poly-Si)</td>
<td>No mobility degradation (low interface trap density)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Material</th>
<th>(\text{SiO}_2)</th>
<th>(\text{ZrO}_2/\text{HfO}_2)</th>
<th>Silicate (Zr,Hf)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric Constant</td>
<td>3.9</td>
<td>(~25)</td>
<td>15 (~25)</td>
</tr>
<tr>
<td>Band Gap (eV)</td>
<td>8.9</td>
<td>(~5.7)</td>
<td>(~6)</td>
</tr>
</tbody>
</table>

• Motivation and background

• Low thermal budget routes to high-\( k \) dielectric/semiconductor structures
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  - Atomic layer deposition (ALD)

• ALD as a tool for gate workfunction engineering

• UVO processing of ZrO\(_2\) gate dielectric on Ge (100) substrates
  - Summary of electrical data from Pt/ZrO\(_2\)/Ge PMOSFET’s
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• Conclusions
UV light supplies atomic oxygen and ozone to the surface through the following reactions:

\[
\begin{align*}
O_2 + h\nu' & \rightarrow 2O \\
O + O_2 & \rightarrow O_3 \\
O_3 + h\nu" & \rightarrow O_2 + O
\end{align*}
\]

Benefits
- Low temperature
- No contamination
- Process simplicity

S. Ramanthan et al., APL 2001
Because a metal precursor is deposited onto the substrate before the oxidation, an opportunity exists for reaction between the precursor and the substrate.

XPS spectra of the Si 2p peak indicate a change in the chemical state of the SiO₂ present as native oxide on the substrate.

Both hafnium and zirconium have greater oxygen affinities than Si and have a tendency to reduce SiO₂ through solid state reaction.

<table>
<thead>
<tr>
<th></th>
<th>Zr</th>
<th>Hf</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>ΔH°</td>
<td>-1089 kJ/mol</td>
<td>-1222 kJ/mol</td>
<td>-910 kJ/mol</td>
</tr>
</tbody>
</table>

Change in free energy for the oxidation reaction

\[ M_x + O_2 \rightarrow M_xO_2 \]

where M is a metal.
UVO Metal Oxide Processing on a Si (100) Surface

- Deposition on bare Si leads to silicidation reaction as evidenced by Hf 4f XPS spectra

- Silicide does not oxidize during UV-ozone processing

- Presence of metallic phase at high-k/Si interface is not desirable for device applications
High-$k$ / SiO$_2$ Gate Stack Grown \textit{in-situ} by UV-Ozone Oxidation at 300 K

- Electrical properties are measured using MOS capacitors

- Metal electrodes are deposited \textit{in situ} on the oxide preventing oxidation in atmosphere and incorporation of contaminants

- Capacitor structures are made through lithographic patterning and ion etching
  Capacitor diameters($\mu$m): 200, 150, 100, 66, 50
Dielectric Behavior: Oxygen Stoichiometry Effects

Polycrystalline ZrO$_2$ film on thermal SiO$_2$/Si

QM corrected EOT ~ 1 nm (Ramanathan, McIntyre, Guha and Gusev, DRC 2002)

S. Ramanathan et al., JAP 2002

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Quantitative EELS Analysis: Partial Oxidation

- Quantitative analysis of EELS O-K fine structure detects additional sub-stoichiometric ZrO phase

ALD (Atomic Layer Deposition)

- **Surface saturation controlled process**
- **Layer-by layer deposition process**
  ; Linear sub-monolayer growth rate

- **Excellent film quality and step coverage**

ZrCl$_4$ or HfCl$_4$

\[
\text{ZrCl}_4(ad.) + 2\text{H}_2\text{O}(g) \rightarrow \text{ZrO}_2(s) + 4\text{HCl}(g)
\]

\[
\text{HfCl}_4(ad.) + 2\text{H}_2\text{O}(g) \rightarrow \text{HfO}_2(s) + 4\text{HCl}(g)
\]

RMS roughness < 0.15nm for 3nm ZrO$_2$ & HfO$_2$
By using a chemical oxide passivation, EOT value of 1.2 nm with a leakage of \(~10^{-6} \text{ A/cm}^2\) at \(|V_G-V_{FB}| = 1 \text{ V}\) was achieved.

- \(ZrO_2\) thickness dependence of capacitance indicated \(\kappa_{ZrO_2} \sim 26\), as expected.
- Suggested 1.3 nm thick amorphous interface layer was not bulk-like \(SiO_2\).

IL thickness > EOT (\(\therefore \kappa_{IL} > \kappa_{SiO_2}\))

ALD \(ZrO_2\) / Chemical Oxide Gate Stacks

C.M. Perkins et al., APL 2001

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Experimental Conditions

• **Deposition system**
  - Cold wall and resistive heating type ALD system
  - Load-lock and high vacuum chamber (~10^{-8} Torr)
  - Solid (ZrCl₄/HfCl₄) and liquid source (H₂O) delivery system

• **Deposition parameters**
  - Process temperature : 300°C
  - Process pressure : 0.5 Torr
  - Source temperature :
    - H₂O (liquid) = R.T.
    - ZrCl₄/HfCl₄ (solid) = 150°C
In-situ Crystallization Kinetics of ALD-HfO$_2$

- In-situ anneal at 520°C using 30Å HfO$_2$ on 25Å thermal SiO$_2$.
- Preliminary analysis shows 2-D (radial) growth with decreasing nucleation rate.
  Avrami isothermal transformation kinetics: $F=1-\exp(-(kt)^n)$  \(n\sim2.2\)
Sample structure: 3nm HfO₂ on 2.5nm SiO₂.

After 700°C, capacitance decreases due to the interfacial oxide growth. *

There was no significant increase in trap assisted tunneling leakage current resulting from crystallization.

* Reagent-grade N₂ ambient contains ~ 1 ppm O₂.

H. Kim et al., APL, 2003
**Effects of HfO₂ Crystallization on Electrical Properties**

*(In-situ Annealing w/o interfacial oxide growth)*

In-situ annealing after ALD-HfO₂ deposition to minimize interfacial oxide growth: 530°C, 1.3Torr with 500 sccm N₂ flow

- Sample structure: HfO₂ on 1.5 nm chemical SiO₂
- No significant leakage current change w/o interfacial oxide growth

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Current Technology: Poly-Si Gates

Advantages of Poly-Si:

• Self-aligned gate
• High thermal stability
• Excellent control over gate workfunction
• Single step operation
• Compatibility with gate oxide
• Ease of fabrication
Band Diagram of an MOS Structure

Schematic of the band diagram of a MOSFET

Gate workfn requirements:
NMOS: ~4 eV
PMOS: ~5 eV
Electrical Workfunctions of Metallic Elements
Workfunction Engineering

Workfunction of Metals and Metal Nitrides:

<table>
<thead>
<tr>
<th>Suitable for NMOS:</th>
<th>Suitable for PMOS:</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. <strong>Ti</strong> (4.33)</td>
<td>1. <strong>Ru</strong> (4.71)</td>
</tr>
<tr>
<td>2. <strong>Al</strong> (4.08)</td>
<td>2. <strong>Rh</strong> (4.98)</td>
</tr>
<tr>
<td>3. <strong>n⁺ poly</strong> (4.17)</td>
<td>3. <strong>Pt</strong> (5.65)</td>
</tr>
<tr>
<td>4. <strong>Mn</strong> (4.1)</td>
<td>4. <strong>Co</strong> (5.0)</td>
</tr>
<tr>
<td>5. <strong>Ta</strong> (4.25)</td>
<td>5. <strong>TaN</strong> (5.2)</td>
</tr>
<tr>
<td>6. <strong>V</strong> (4.3)</td>
<td>6. <strong>p⁺ poly</strong> (5.17)</td>
</tr>
<tr>
<td>7. <strong>Zn</strong> (4.33)</td>
<td>7. <strong>Mo</strong> (4.6)</td>
</tr>
</tbody>
</table>

(values in brackets are workfn in eV)

**Our Focus:**
- Ta - NMOS
- TaN - PMOS

**Our Goal**
- Grow the high-k gate oxides by ALD using the Zr/Hf precursor
- In-situ gate deposition using tantalum precursor
- Deposit a thick, low resistivity metal layer to reduce the overall resistance of gate stack

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RF plasma ALD system for deposition of metal diffusion barrier liners for damascene Cu interconnect structures [Rossnagel et al. JVST B 18(4) 2016 (2001)].

- Ta and TaN have appropriate work-functions for CMOS gate electrodes
- In deeply scaled, fully-depleted channel devices, gate electrode workfunction will control device threshold voltage, rather than implanted channel dopant
- ALD may provide the needed capability to grow very thin metal layers with controlled workfunction on the gate stack
Outline

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**Benefits of Ge Substrates**

**Electronic Properties:**
- More symmetric and higher carrier mobilities (low-field)
  ⇒ More efficient source injection
  (due to lighter $m^*$)
  ⇒ ↓ CMOS gate delay
- Smaller energy bandgap
  ⇒ Survives $V_{DD}$ scaling
  ⇒ ↓ $R$ with ↓ barrier height
- Lower temperature processing
  ⇒ Compatible w/ 3D Integration

Better performance may result from combining high-$k$ gate dielectric and Ge substrate.


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1. $\text{GeO}_2 + \text{Zr} = \text{Ge} + \text{ZrO}_2 \ (T=600K)$
   $\Delta G^\circ = -520 \text{ kJ/mol}$
   \( \rightarrow \) Zr-GeO\textsubscript{2} tie line cannot exist.

2. Formation energy of ZrO\textsubscript{2} is very large
   \( [\Delta G^\circ(\text{ZrO}_2) = -1135 \text{ kJ/mol} ] \)
   \( \rightarrow \) Tie lines tend to emanate from ZrO\textsubscript{2}

---

Although there is less available thermodynamic data for Ge compounds, phase equilibria are expected to be similar to Si case.

GeO\textsubscript{2} is much less stable than is SiO\textsubscript{2} in the presence of Zr, Hf, and O\textsubscript{2}.

\( \Delta G^\circ_f(\text{GeO}_2) = -610 \ (\text{kJ/mol}) \)

\( \Delta G^\circ_f(\text{SiO}_2) = -921 \ (\text{kJ/mol}) \ @600K \)
Ge-Channel High-k Devices

(a) Native GeO₂ is unstable
(b) Hydrophobic Ge surface
(c) Sputtering of 22-30 Å Zr
(d) Complete oxidation of Zr forming ZrO₂
(e) No interfacial oxide layer

Interface layer-free room temperature ZrO₂ deposition by UVO oxidation of sputtered Zr precursor films

CV and JV characteristics of MOSCAP

Output characteristics of a 2 µm gate length Ge transistor ($W_{eff} = 320.4$ µm)

CV measurement (400 kHz) collected from a Ge transistor

25 µm Ge transistors with ~30 Å ZrO₂

Universal Mobility Model for Si MOSFET

C.O. Chui et al. EDL, IEDM 2002

Krishna Saraswat (EE), McIntyre (MSE)
- Compared to thermally grown GeO$_2$, the native oxide also includes a Ge-suboxide component (GeO$_x$)

- Common hexagonal phase of GeO$_2$ is water soluble and volatile
- H$_2$O removes GeO$_2$ but not GeO
- GeO$_x$ can be removed at T > 430 °C in vacuum

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Determined standard spectra for a) sputter etched Ge, b) native Ge oxide, c) and UVO Ge oxide - compared to 3p spectra obtained from ZrO$_2$/Ge samples

- $\lambda_e = 24$ Å

$\text{Signal} \propto \exp\left(-\frac{\text{overlayer}}{\lambda \sin \theta}\right)$

Calibrated take-off angles by measuring attenuation of Ge substrate peak for known overlayer thickness

XTEM of functioning high-k MOSFET
Ge 3p Spectra for Different Angles

10 Å Zr, UVO

20 Å Zr, UVO

30 Å Zr, UVO

Samples capped with ~ 3 nm a-Si
ARXPS Depth Profiles: ZrO₂/Ge Interface

10 Å Zr, UVO
UVO 300 K
1 hour

5 – 7 Å GeOₓ

20 Å Zr, UVO
UVO 300 K
1 hour

3 – 5 Å GeOₓ

If precursor thickness/oxidation time is optimized, UVO gate stacks can be prepared on Ge with essentially no IL

30 Å Zr, UVO
UVO 300 K
1 hour

2 – 3 Å GeOₓ (detection limit for this ZrO₂ thickness)
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ALD ZrO₂ (~ 55 Å thick) was grown on vapor HF cleaned Ge
No interfacial layer detected; local epitaxial growth observed
One interfacial dislocation per every ten (111) planes: consistent with substantial relaxation of biaxial misfit strain
- lattice mismatch between ZrO₂ and Ge (~10 %).

H. Kim et al.
APL, accepted

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XPS Analysis of ALD ZrO$_2$ on Ge

Angle-Resolved XPS

Depth Profiling XPS

- Interfacial GeO$_x$ is observed in thin ZrO$_2$ sample, appears to form by oxidation after air exposure of the uncapped ZrO$_2$ film
- No detectable interfacial oxide can be seen beneath thick ZrO$_2$

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EOT approximated from 10kHz CV data
Large frequency dispersion creates uncertainty in precise EOT value
Hysteresis and frequency dispersion may be caused by disorder at the ZrO$_2$/Ge interface (dislocations etc.).
Inversion characteristics suggest increase in minority carrier generation (contamination?).
- ZrO₂ on Ge samples show a slightly higher leakage current behavior compared to same physical thickness ZrO₂ on Si.
- Significantly lower leakage current than SiO₂ for the same EOT (absence of thick interfacial oxide layer).
- Low leakage current densities are encouraging from standpoint of device applications.
ALD of HfO$_2$ on Ge NW*

*CVD Ge NW growth courtesy of D. Wang and H. Dai, Stanford U.

- Conformal deposition – key attribute of ALD for dielectric passivation of NW surfaces for thin-body FETs
- Evidence that HfO$_2$ growth from HfCl$_4$/H$_2$O precursors on Ge surface is in the true ALD regime
Conclusions

- UVO processing of metal oxide gate dielectrics on SiO$_2$ from sputtered metal precursors results in a mixed metal oxide-SiO$_2$ layer - may contribute to the very low EOT of these gate stacks

- *In situ* annealing after ALD HfO$_2$ deposition shows HfO$_2$ crystallization does not contribute to an increase in leakage current density

- The surface adsorption limited film growth mechanism of ALD provides an opportunity for achieving area selectivity - we have demonstrated inhibition of HfO$_2$ ALD onto ODT-passivated SiO$_2$

- UV-ozone oxidation of ultra thin Zr films has been used to prepare high-$k$/Ge PMOSFETs with hole mobilities ~ 2x that achievable in SiO$_2$/Si devices

- By controlling the metal precursor thickness and oxidation conditions, UVO metal oxide processing can produce essentially interface layer-free gate stacks on Ge

- ALD ZrO$_2$ on HF-last Ge exhibits local epitaxy (cube-on-cube relationship) - no interface GeO$_x$ layer detected by XPS or TEM

- Low leakage current densities observed for ALD ZrO$_2$ on HF-last Ge suggest there is no intrinsic leakage problem for ZrO$_2$/Ge gate stacks