Novel Germanium Technology and Devices for High Performance MOSFETs

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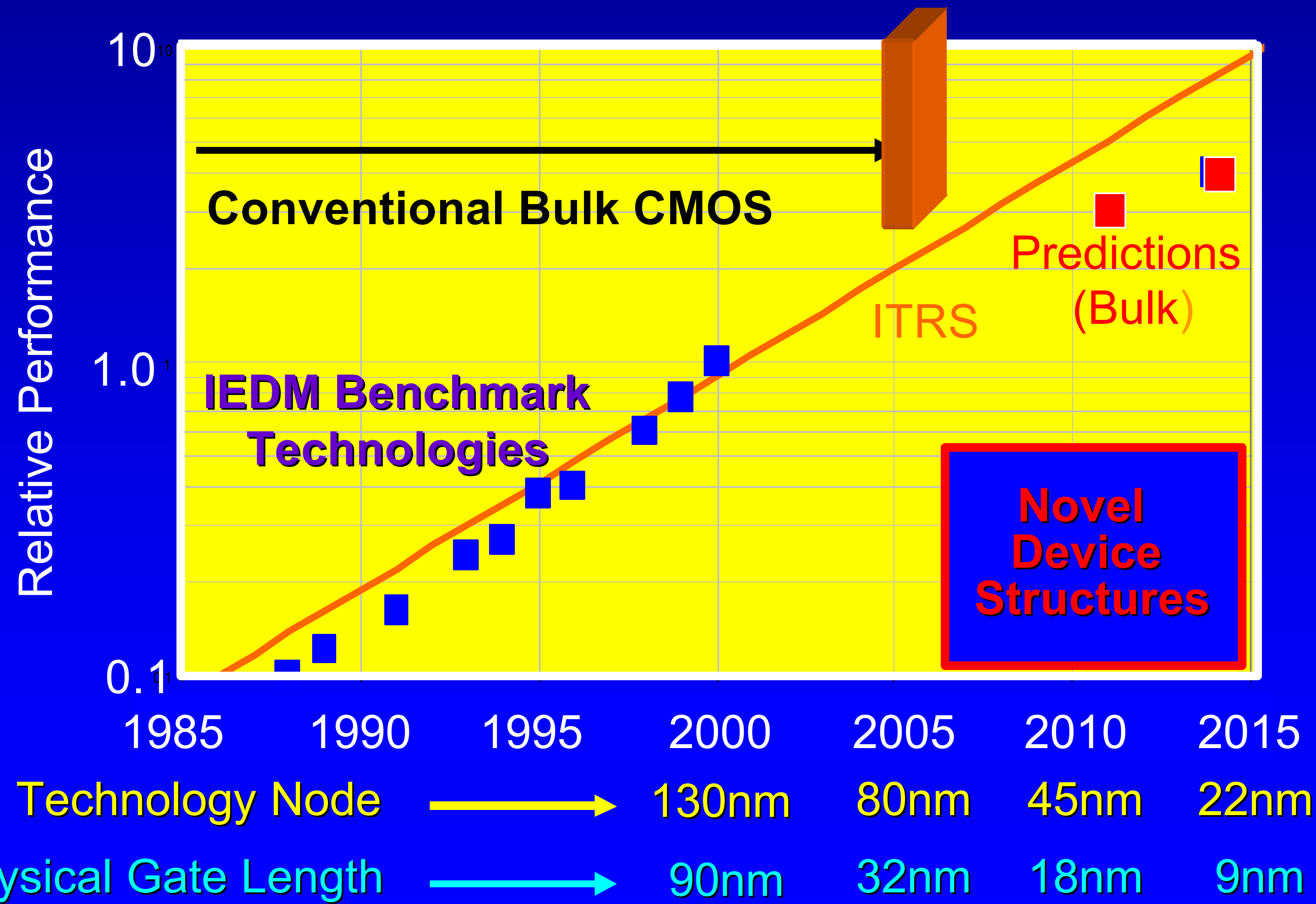
Collaborators: Profs. Paul C. McIntyre and Yoshio Nishi

Outline

- Ge CMOS Motivations
- Ge MOS Gate Dielectric Technology
  ⇒ UVO Oxidation of Metal
  ⇒ ALD of Metal Oxides
- Ge Dopant Incorporation Technology
- Ge MOSFETs with High-κ and Metal Gate
- Conclusions

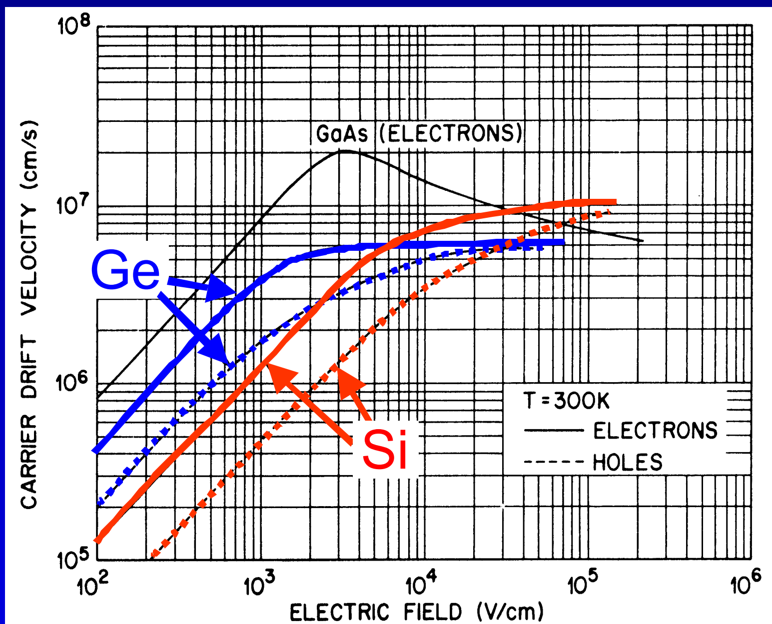
Bulk-Si Performance Trends

- Maintaining historical CMOS performance trend requires new semiconductor material and structures by 2008-2010…
- Earlier if current bulk-Si data do not improve significantly



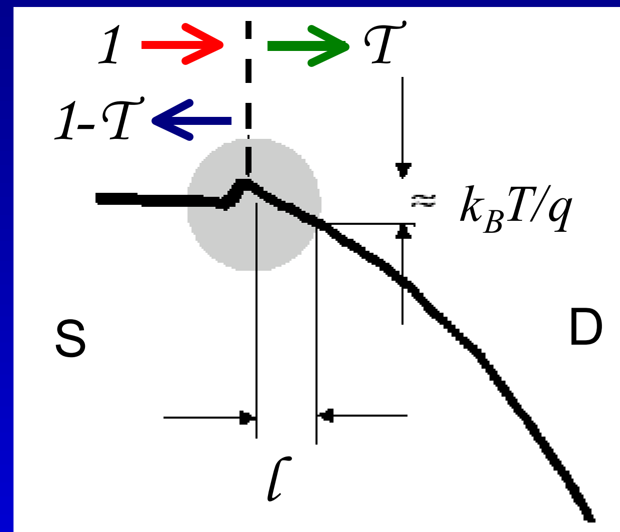
A Fundamental Scaling Limit - I_{Dsat}

I_{Dsat} no longer set by v_{sat}



(Sze, 1981)

For very short channel MOSFETs



(Lundstrom, 2001, Purdue)

$$\mathcal{T} = \frac{l_0}{l + l_0}$$

$$l_0 \propto t_0 \propto m_{low-field} \propto v_{inj}$$

Drive Current & Gate Delay

$$I_{DS} = W \times Q_{inv} \times v_{inj}$$

$$\frac{C_{LOAD} V_{DD}}{I_{DS}} = \frac{L_{gate} \times V_{DD}}{(V_{DD} - V_T) \times v_{inj}}$$

Ballisticity Comparisons

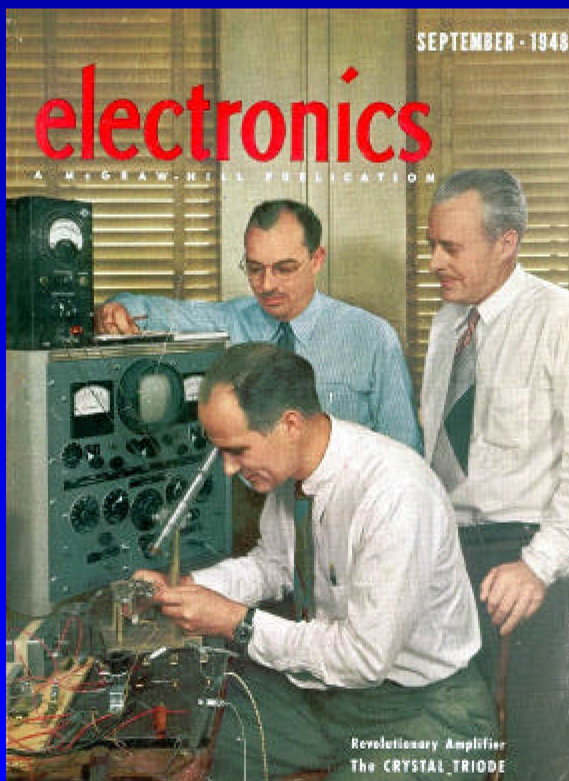
	Si <100>	Ge <100>	Ge <111>
n-MOS	0.68	0.78	0.76
p-MOS	0.48	0.70	0.56

(Chui *et al.*, *IEEE IEDM*, 2003)

Germanium – A Material with History

1st Transistor is in Ge

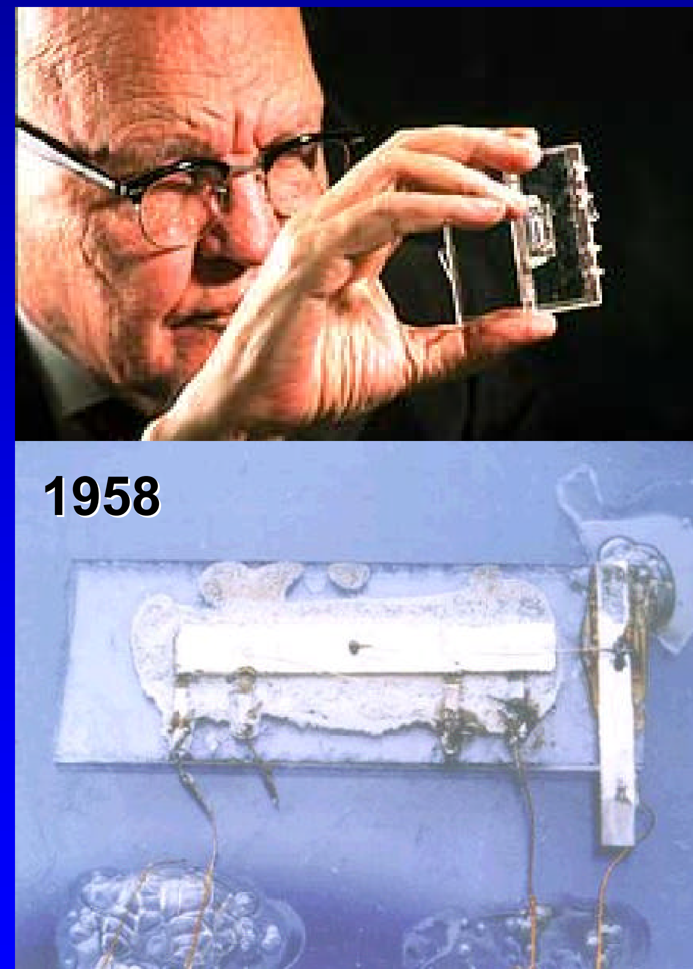
By Bardeen, Brattain, and Shockley,
Nobel Laureates in Physics 1956



(http://www.bellsystemmemorial.com/belllabs_transistor.html)

1st Integrated Circuit is in Ge

By Kilby,
Nobel Laureates in Physics 2000



(Courtesy of TI and Huff, SEMATECH)

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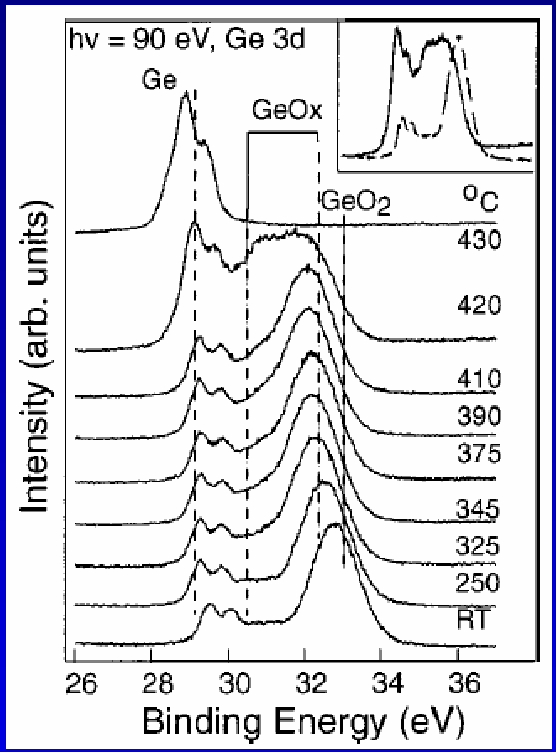
Problem #1: Ge Surface Passivation

The Problems:

- The native oxide passivation on Ge surface is not stable enough either during fabrication or in the end-product
  - ⇒ GeO_2: water soluble/hygroscopic
  - ⇒ GeO : volatile at low temperature
- Very high quality gate dielectric/Ge substrate interface is required



(Prabhakaran, *APL*, 2000)

Prior Attempts in the Last 40 Years:

- Pyrolytic, LPCVD, RPECVD **SiO_2**
- Thermal, UVO **GeO_x** (followed by nitridation, **GeO_xN_y**)
- LPCVD **Ge_3N_4** and Pyrolytic **Al_2O_3**

None of them would likely offer an EOT ≤ 10 Å to advance beyond the sub-20 nm regime

High-k Dielectrics on Germanium

The Surface Passivation Solution:

- **High-k** (metal oxide) dielectrics are being researched to replace SiO_2 for scaled Si MOSFETs
- These dielectrics are deposited on Si, but not thermally grown, why not on Ge?
- Volatility/Instability of native oxides or sub-oxides makes surface cleaning easier for **high-k** on Ge
- Gate dielectric stack free of the performance limiting, lower-κ, interfacial GeO_x layer could be possible
- Allows integration of metallic gate electrode to eliminate the carrier depletion problem in poly-Si gates

(Chui *et al., U.S. Patent Pending (Serial No.: 10/404,876*))

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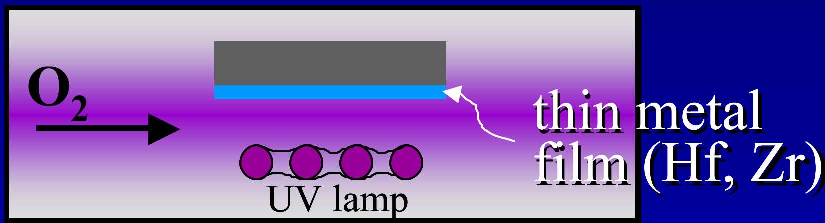
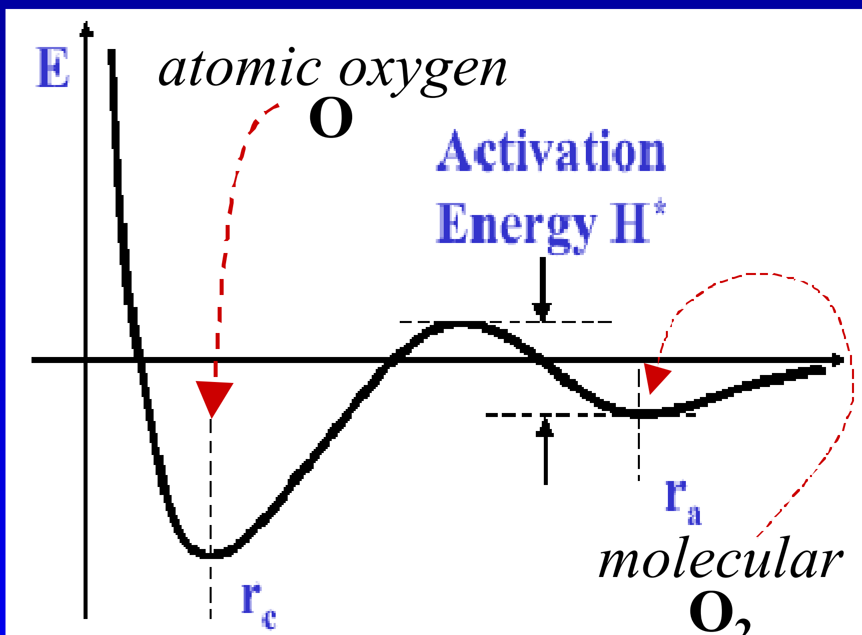
Novel Dielectrics by UV-O_3 Oxidation

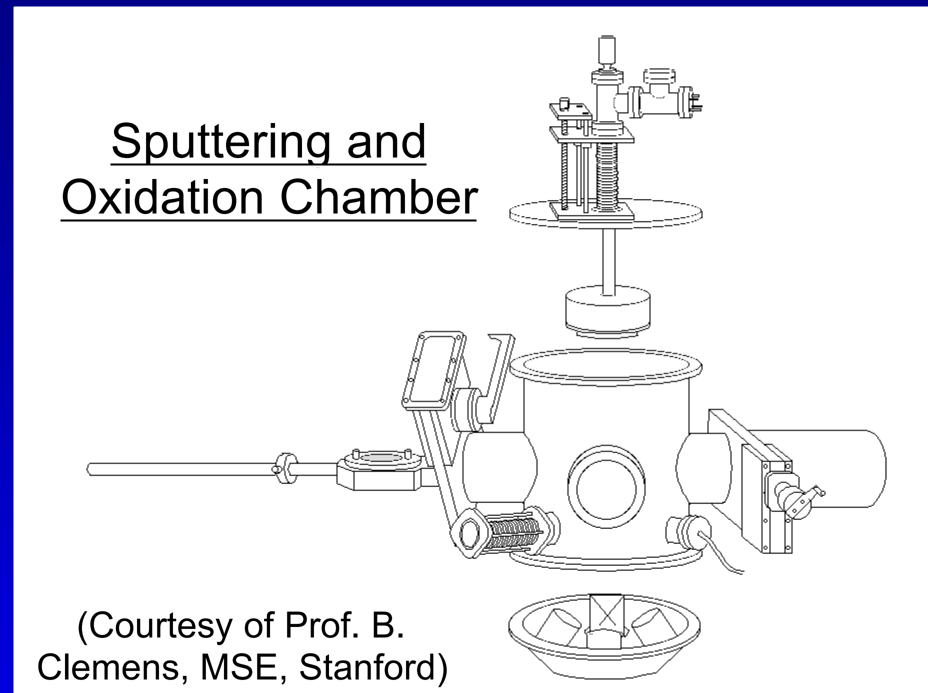




$O_2 + hn' \text{ —— } 2O$

$O + O_2 \text{ —— } O_3$

$O_3 + hn'' \text{ —— } O_2 + O$



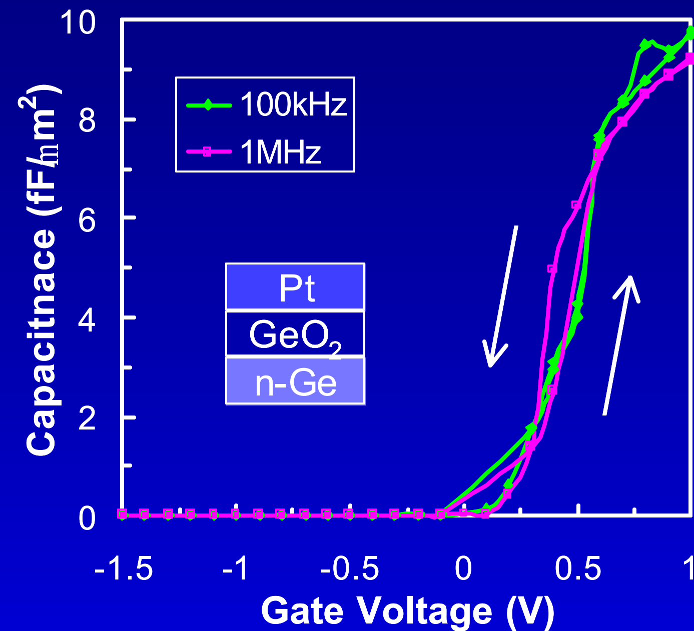
- Advantages
  - ⇒ Low temperature
  - ⇒ Low contamination
  - ⇒ Process simplicity
  - ⇒ *In-situ* electrode capping

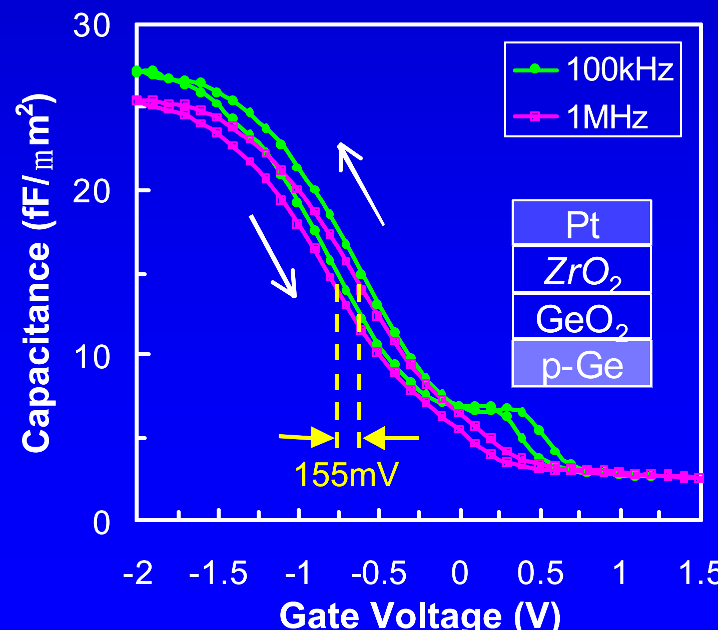
(Courtesy of Prof. Paul McIntyre, MSE, Stanford)

UV-O_3 Oxidation of Zr on Ge

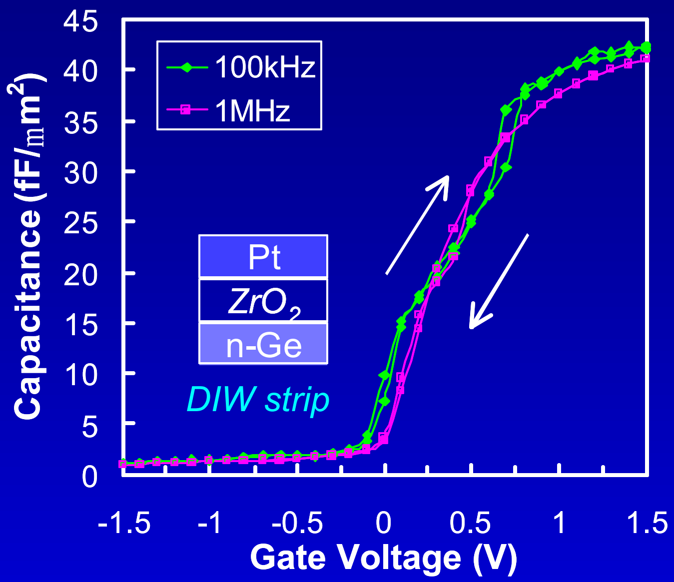
Sample	Doping	Native Oxide	Thermal Oxidation	ZrO_2 Deposition
#1	N	Kept	500°C 2 mins	-
#2	P	Kept	-	~35 Å
#3	N	Stripped in DI Water	-	~35 Å
#4	N	Stripped in HF Vapor	-	~35 Å

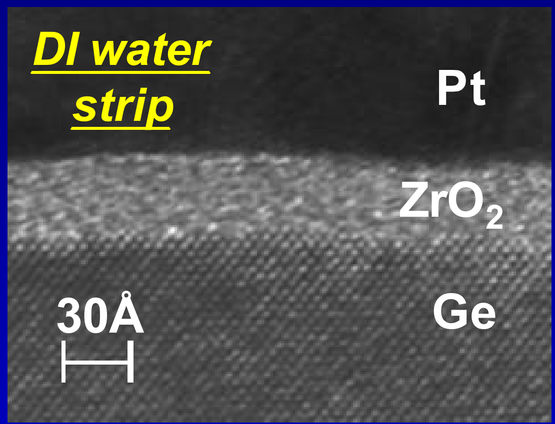
(***Best Student Paper Award:** Chui *et al.*, *IEEE DRC*, 2002)



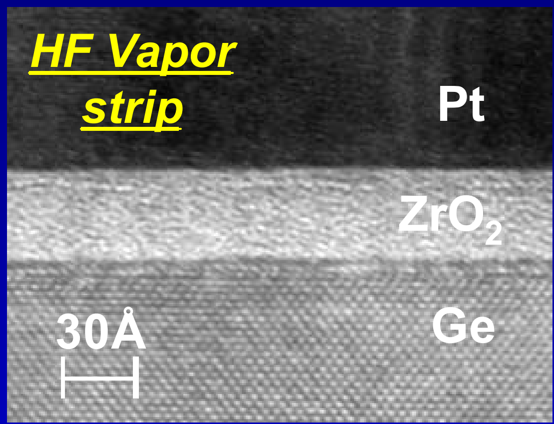


Electrical & Material Characteristics

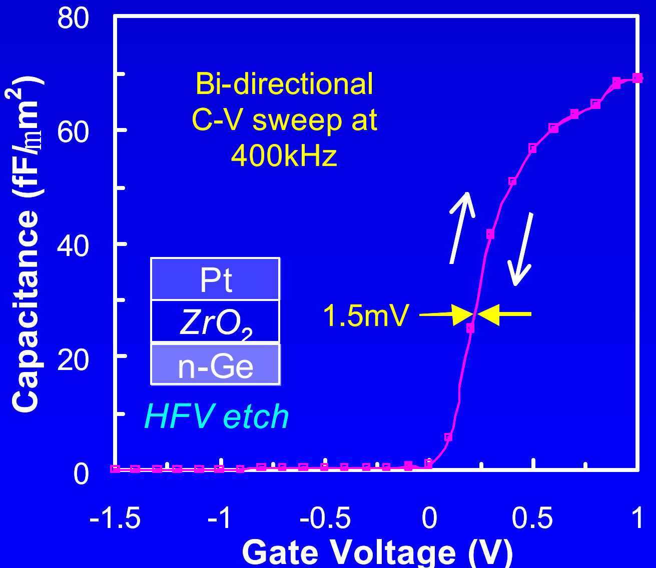




TEM + CV ⇒ EOT ~8-10 Å



TEM + CV ⇒ EOT ~5-7 Å



- The common GeO_2 phase has poor quality
- Hysteresis become negligible in its absence
- Atomically abrupt interface
- Usually, high-quality interface layer between high-κ and Si is required
- High-κ maybe more feasible for Ge MOS applications

(Chui *et al.*, *IEEE EDL*, 2002)

(***Best Student Paper Award:** Chui *et al.*, *IEEE DRC*, 2002)

SR-PES Spectra of ZrO_2 on Ge

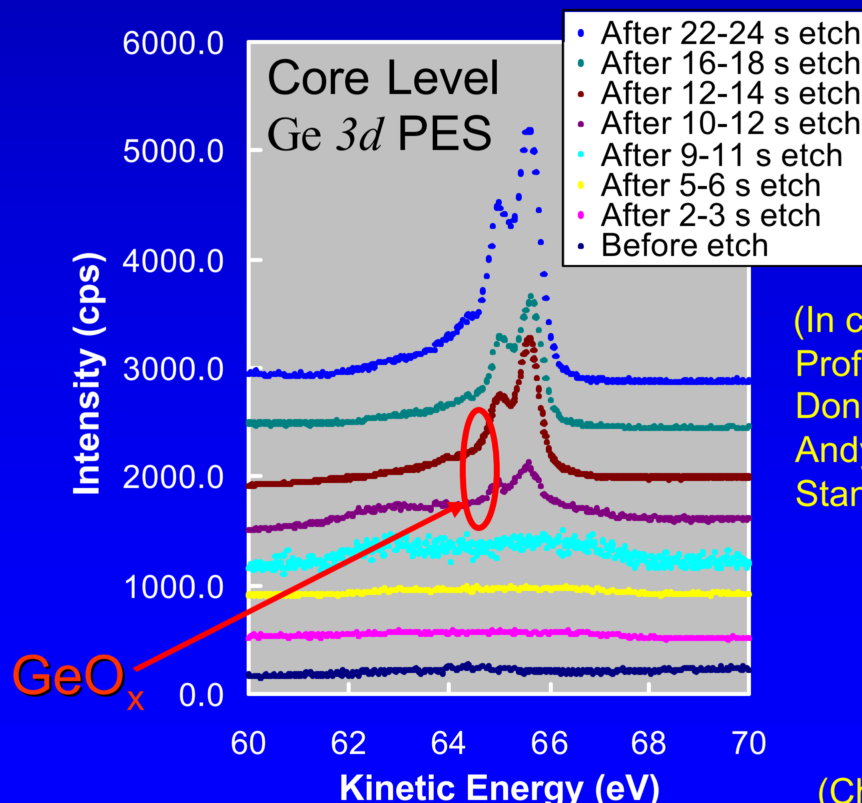
Stanford Synchrotron Radiation Lab

BL 8-1 ***hn*** **= 100 eV Bias = 0 V DKE = 0.05 eV**

⇒ To identify the existence of interfacial GeO_x

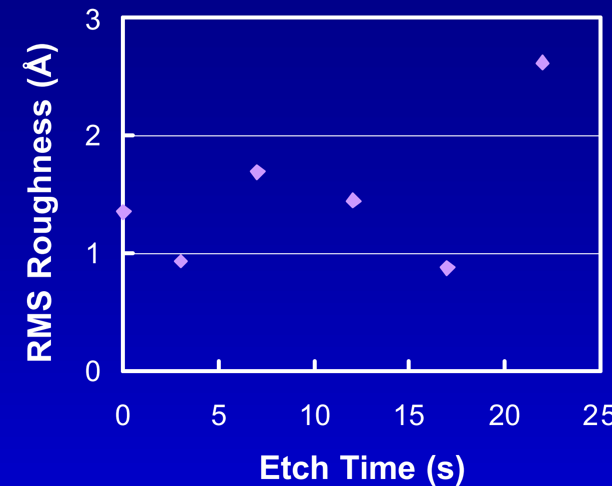
⇒ Upon layer-by-layer wet etching of ZrO_2, composition variation is monitored with PES

⇒ Little shoulder observed in lower KE side of Ge *3d* doublet peak, i.e. interfacial GeO_x

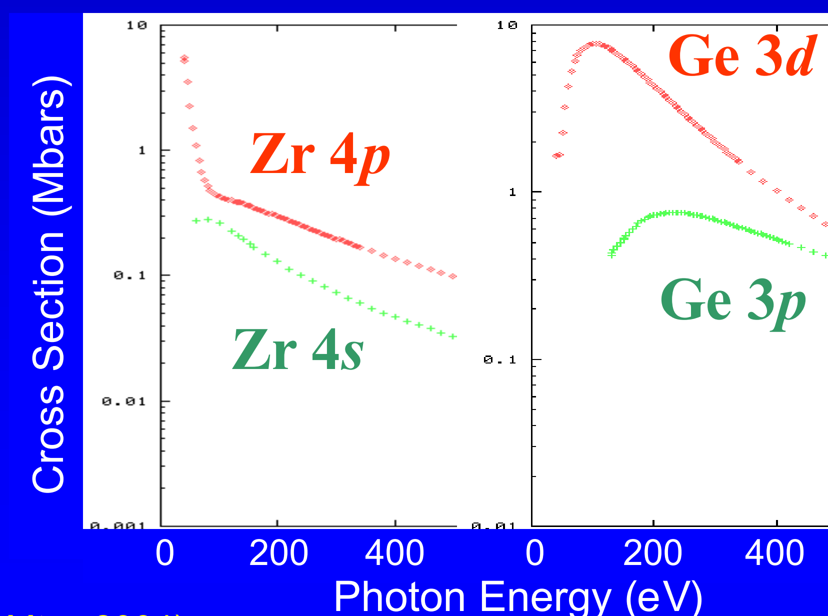


(In collaboration with Prof. Piero Pianetta, Dong-Ick Lee, and Andy Singh, SSRL, Stanford)

AFM ZrO_2 Surface Roughness



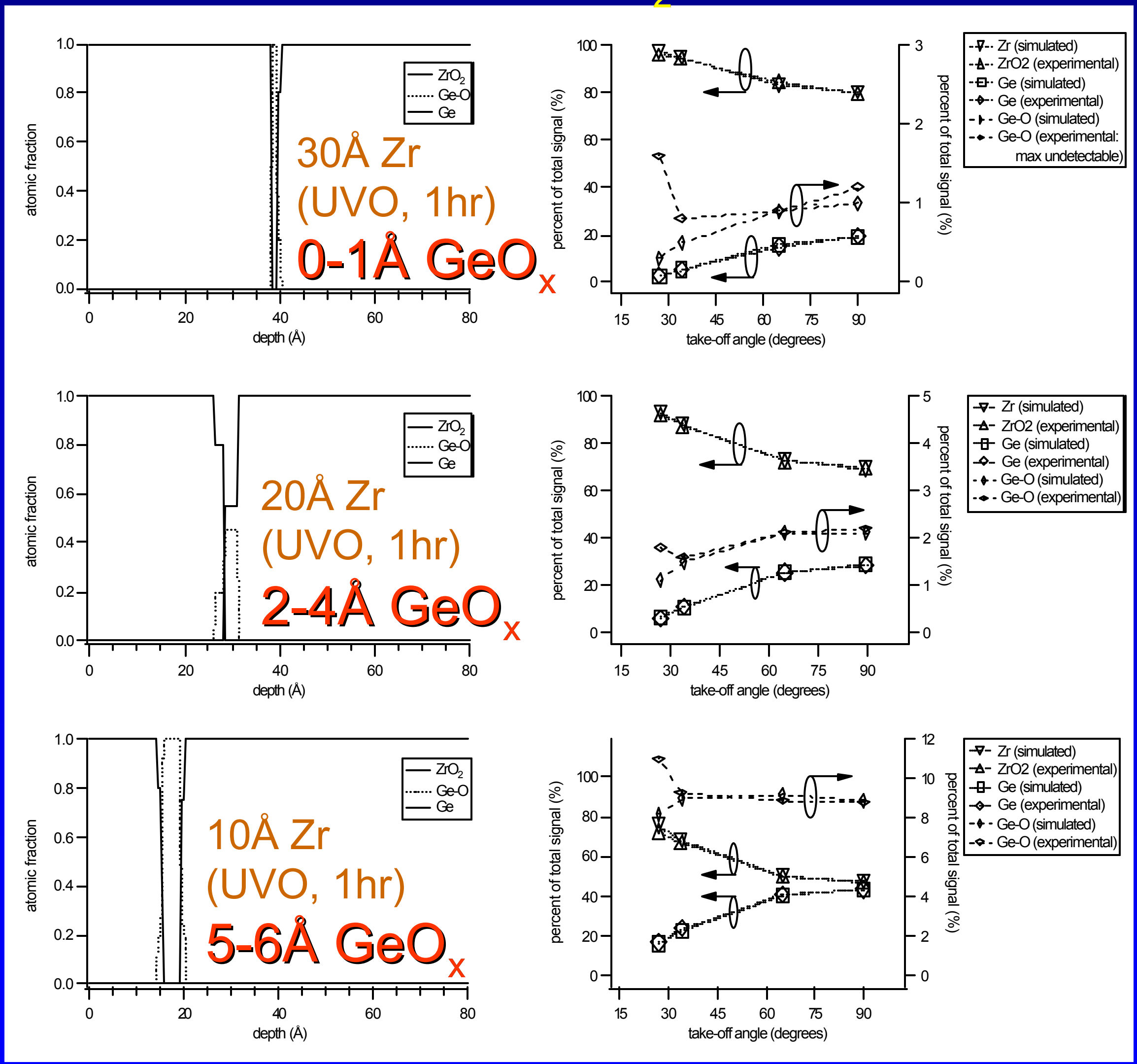
Subshell PE-XS of Zr and Ge



(Chui *et al.*, *MRS Spr. Mtg.*, 2004)

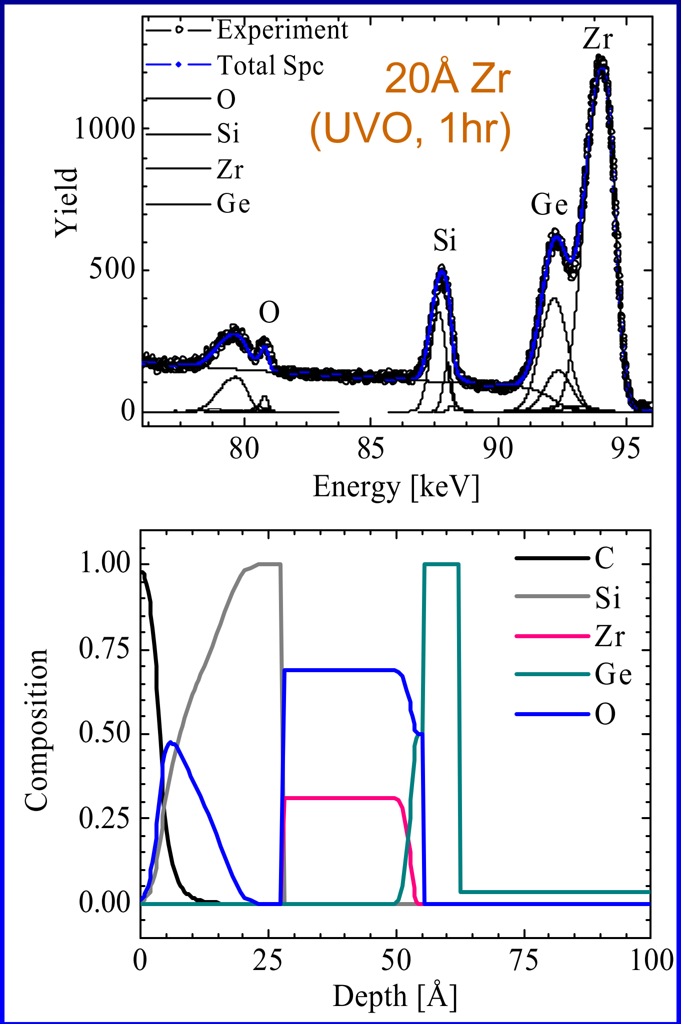
ARXPS and MEIS of ZrO_2 on Ge

Depth Profile Simulations on Experimental ARXPS for Different ZrO_2 Thickness on Ge



(Chi, Chui, Saraswat, Triplett, and McIntyre, *submitted to JAP*)

MEIS Spectrum and Depth Profile Simulation



24.5Å ZrO_2/3Å GeO/Ge(001)

(with Prof. Eric Garfunkel, Chemistry, Rutgers)

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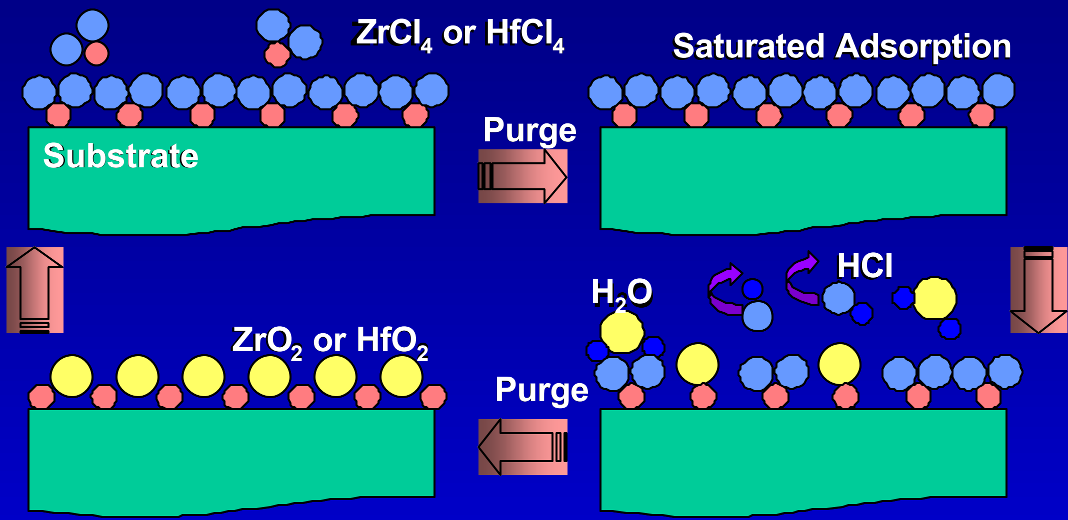
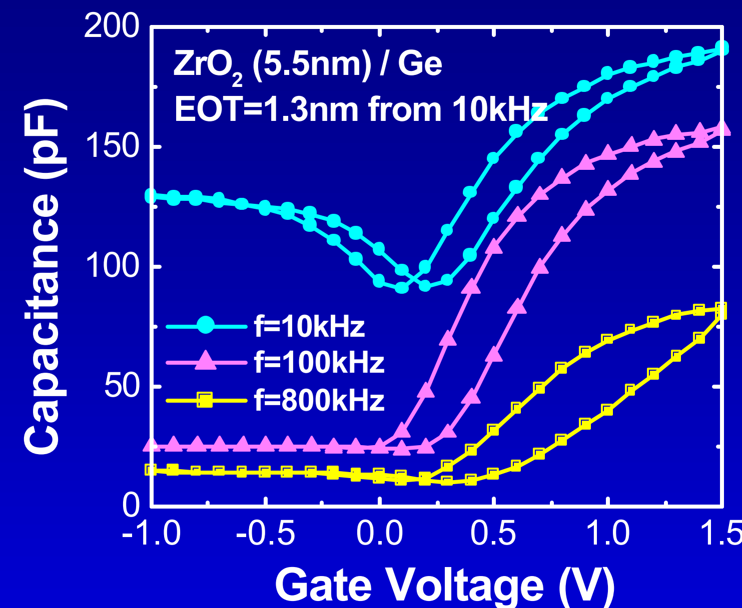
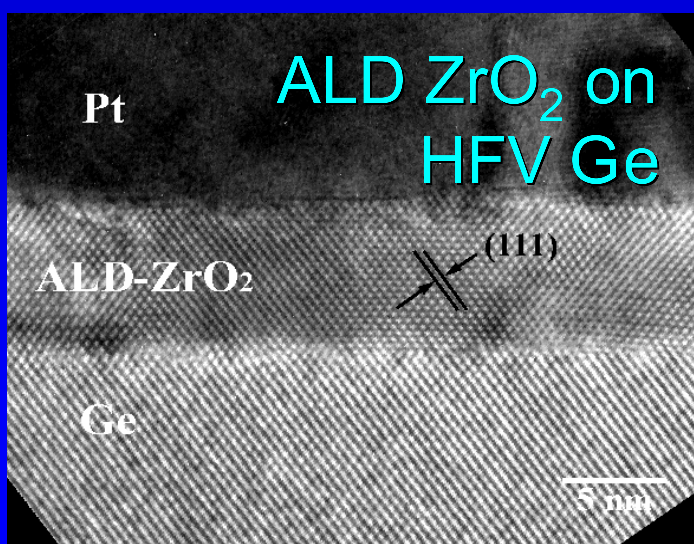
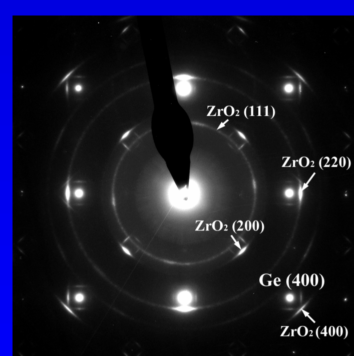
Atomic Layer CVD of High-k Dielectrics

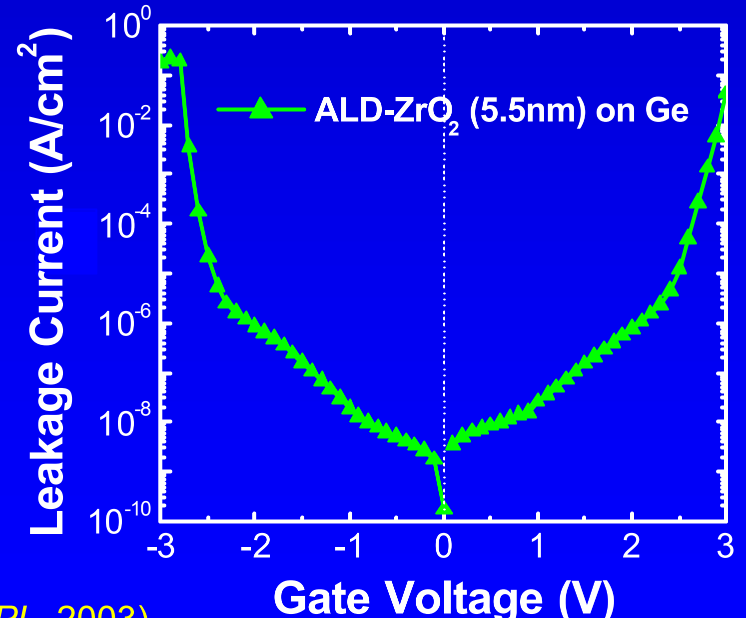


$ZrCl_4$(ad.) + $2H_2O$(g) -> ZrO_2(s) + 4HCl(g)
$HfCl_4$(ad.) + $2H_2O$(g) -> HfO_2(s) + 4HCl(g)



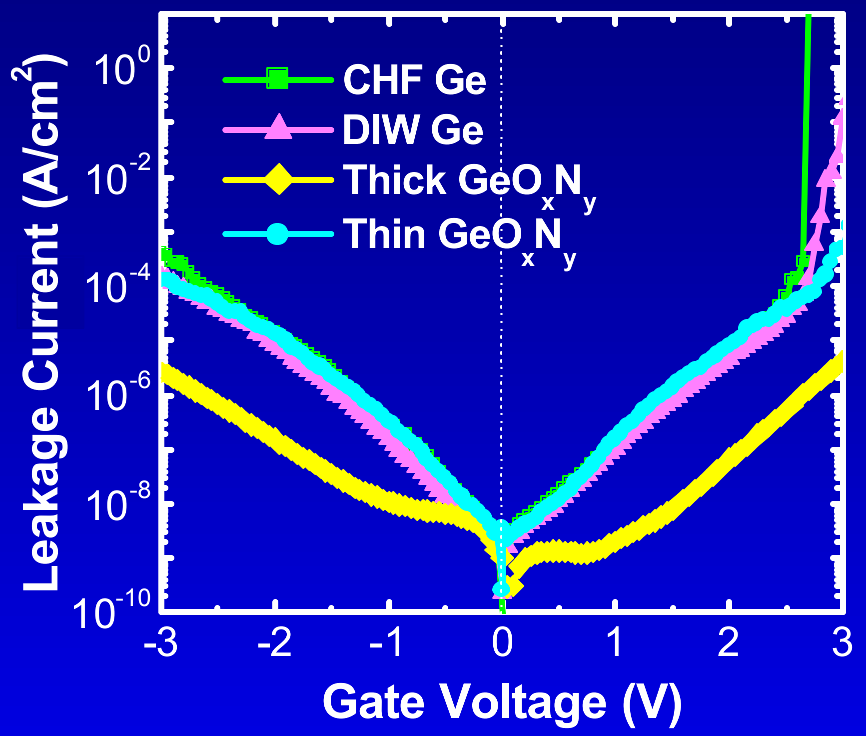


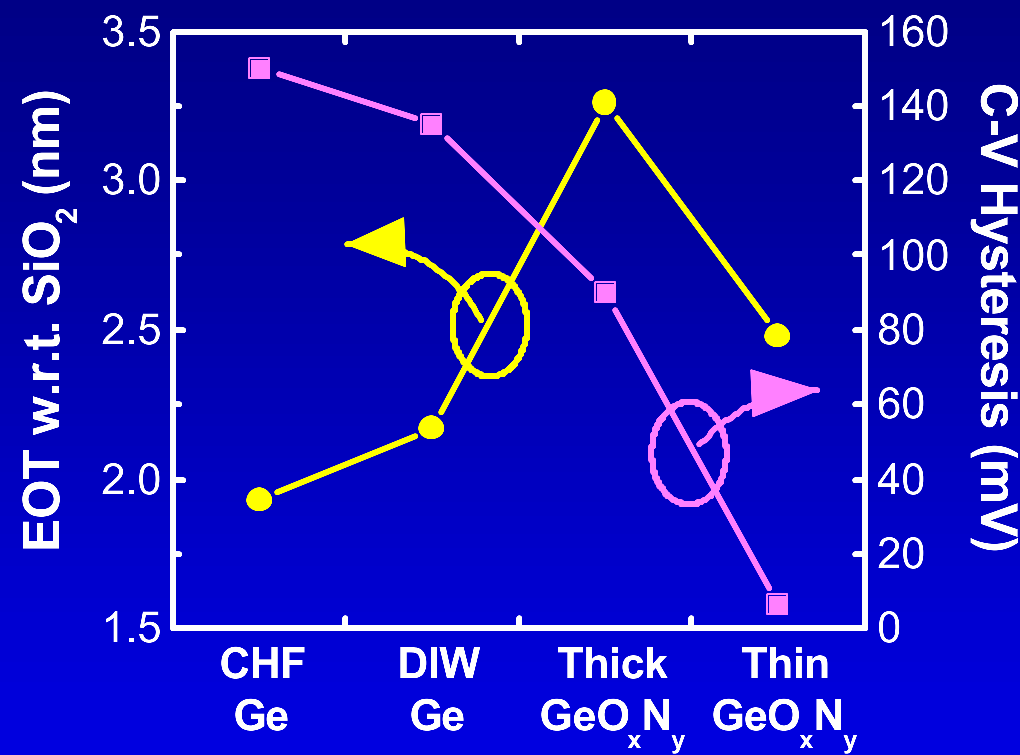




(Kim and Chui *et al.*, *APL*, 2003)

Effects of Surface Preparation





- **CHF Ge:**

  Cyclic rinsing between 50:1 HF and H_2O

- **DIW Ge:**

  Rinsing in DI water

- **Thick GeO_xN_y:**

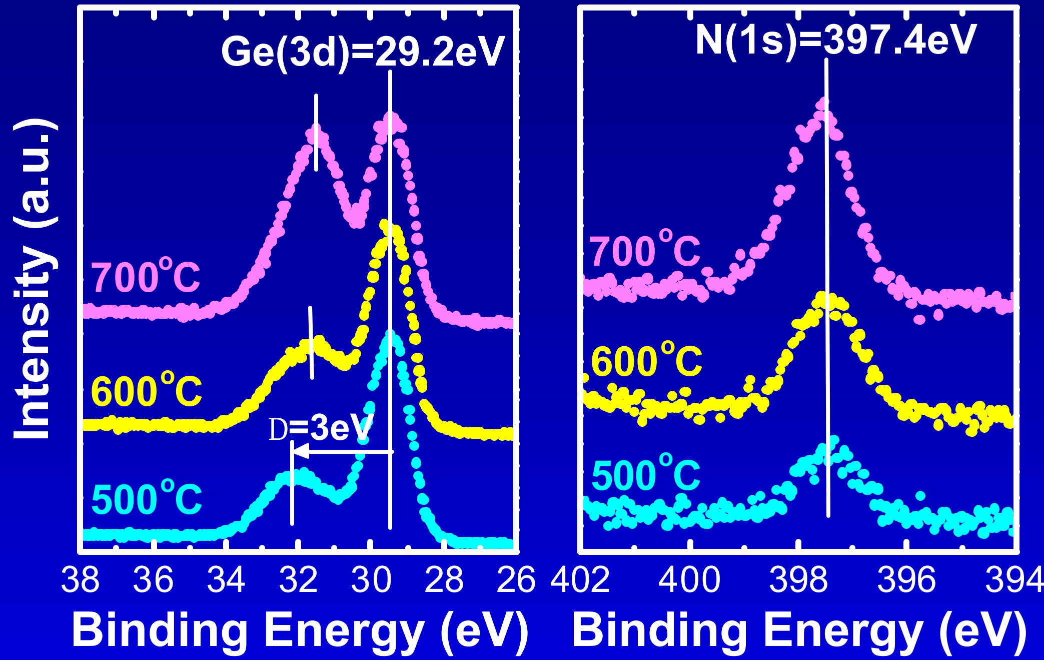
  Rapid Thermal Nitridation (RTN) of thermally grown GeO_2

- **Thin GeO_xN_y:**

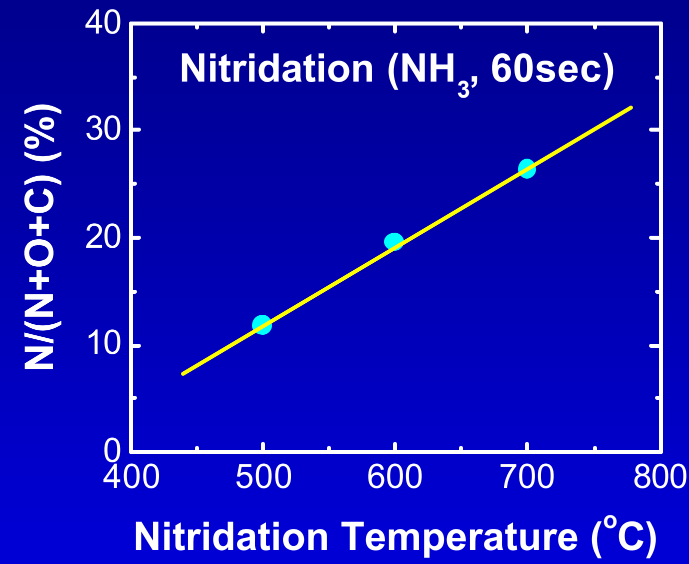
  RTN of CHF Ge

(Chui *et al., submitted to IEEE EDL*)

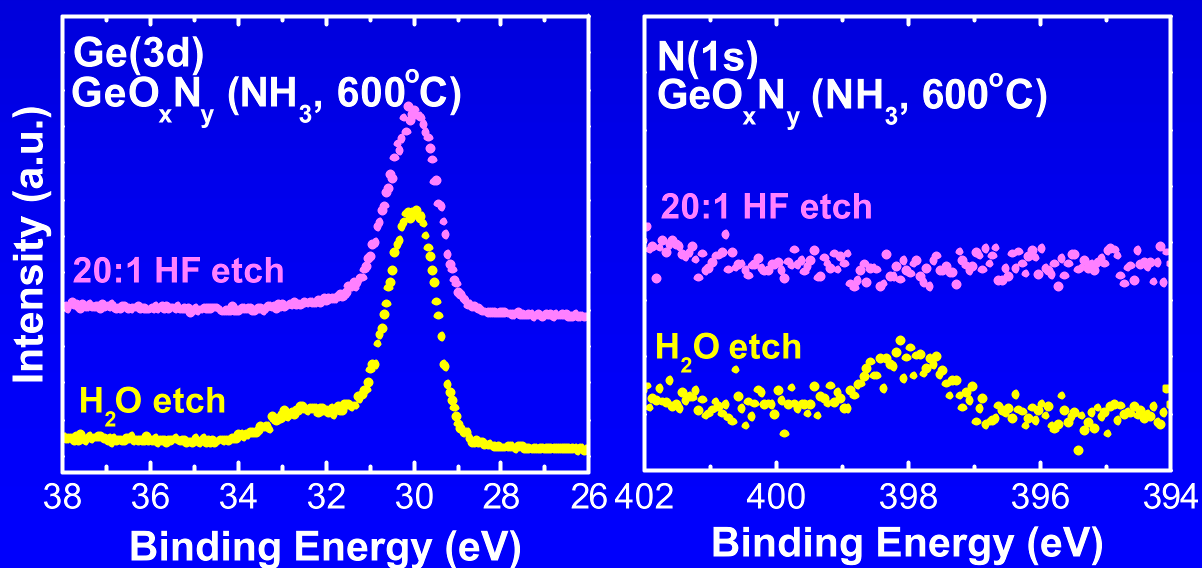
GeO_xN_y Optimization and Stability



N content vs. temperature

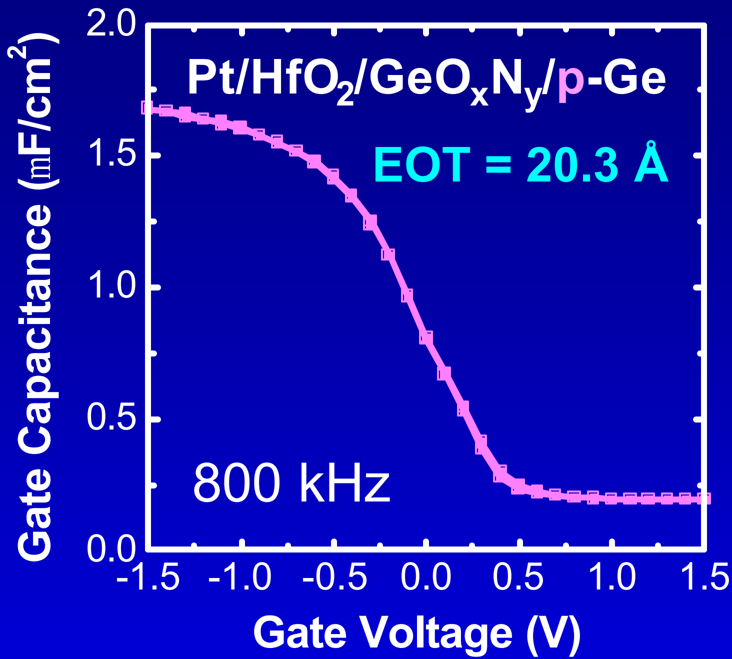


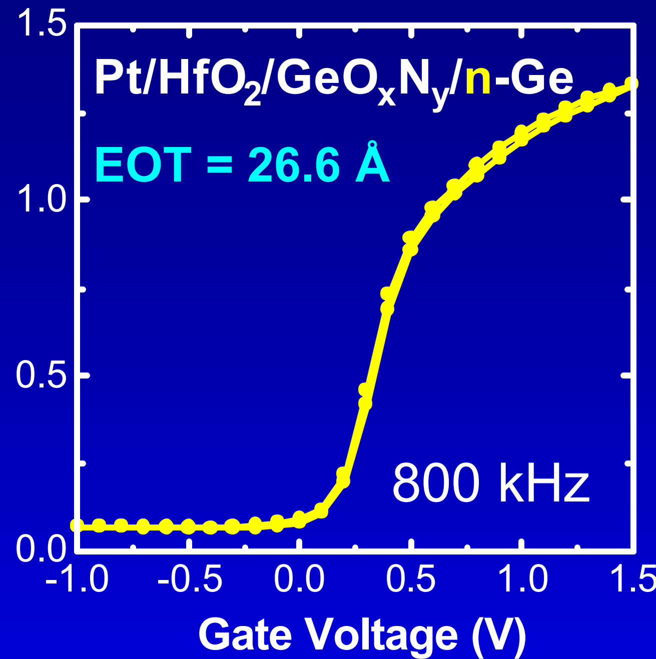
Wet etching stability of the optimum GeO_xN_y



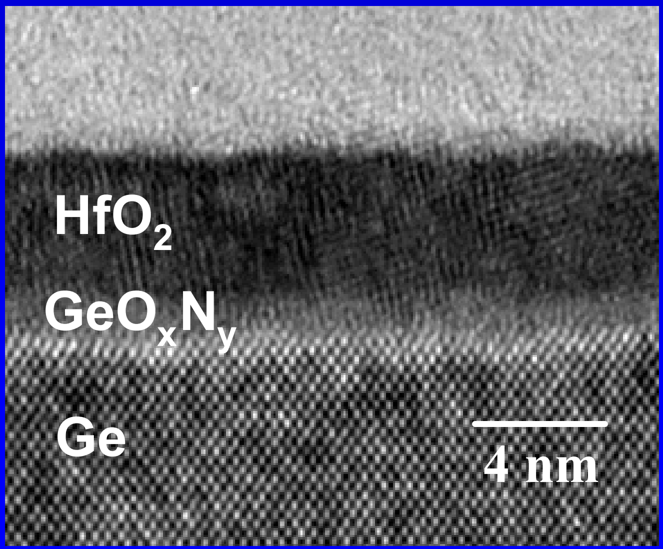
(Chui and Kim *et al.*, *in preparation*)

Dielectric Stack for MOSFET





(Chui *et al., submitted to IEEE EDL*)



The dielectric recipe:

1) Ge cyclic rinsing between 50:1 HF and H_2O
2) RTN in NH_3 at 600°C for 1 min
3) ALD of high-κ films at 300°C using MCl_4 precursors

Where Do These New Materials Help?

$I_{channel}$ μ *charge × source injection velocity*

μ *(gate oxide cap × gate overdrive) ×* v_{inj}

μ $C_{ox}(V_{GS} - V_T) \times E_{source} \times m_{inj}$

High-κ Gate Dielectrics

- ⇒ ↑ gate coupling
- ⇒ ↓ leakage & ↑ reliability (?)
- ⇒ ↓ dopant penetration

Metal Gate Electrode

- ⇒ ↓ gate poly depletion
- ⇒ ↓ remote charge scattering

High Quality Ge Channel

- ⇒ ↑ mobility
- ⇒ ↓ supply V_{DD} (V_{DD} scaling)
- ⇒ ↓ processing temperature

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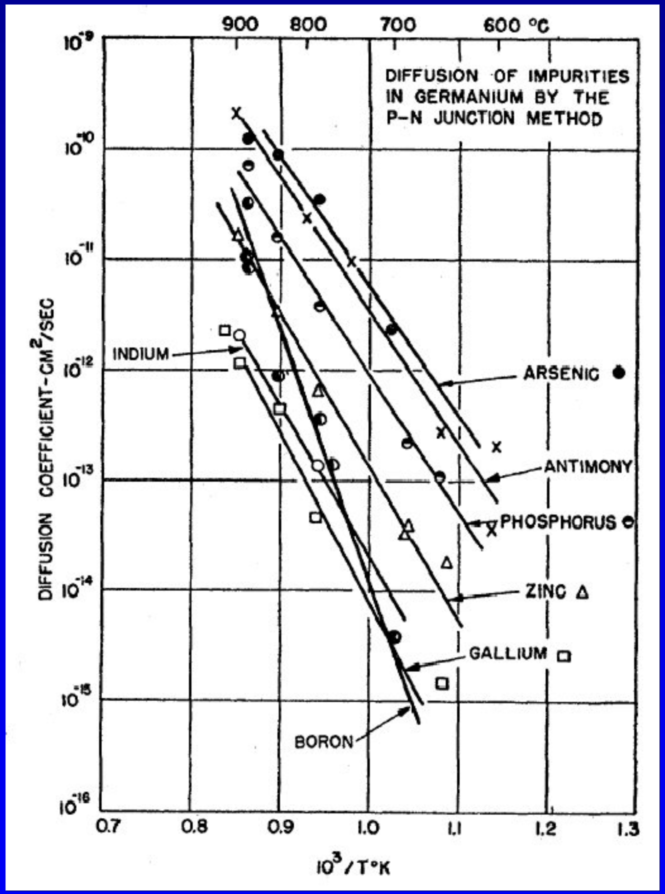
Problem # 2: Dopant Incorporation in Ge

The Problems:

- Larger *n*-type impurity diffusivities than Si
  - ⇒ Shallow junction in Ge NMOS difficult
  - ⇒ Unknown diffusion mechanisms
- Relatively lower Solid Solubility Limits (SSL)
  - ⇒ I_{ON} limited by source/drain resistance

Prior Attempts in the Last 30 Years:

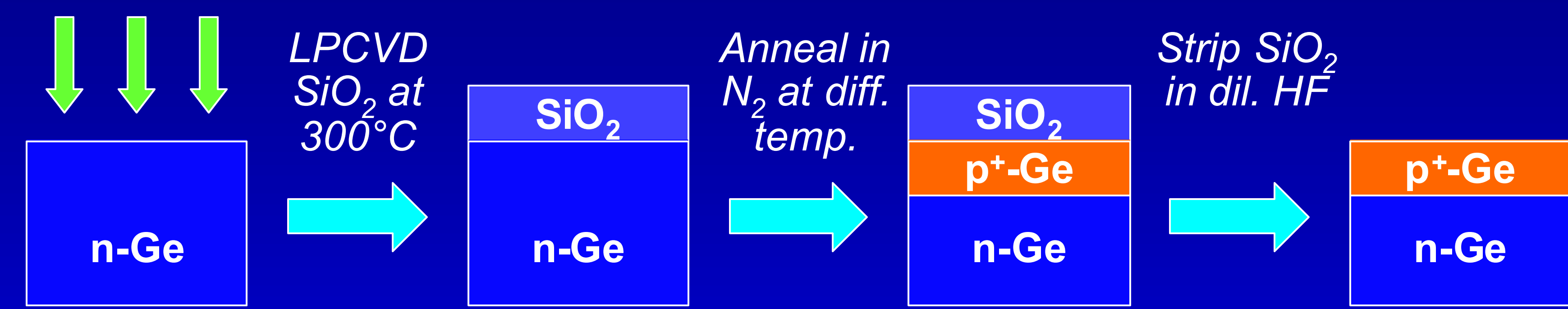
- *P*-type: Furnace anneal of ion-implanted B
  - ⇒ Not suitable for shallow junction
- *N*-type: RTA and FA of implanted ions
  - ⇒ Mostly low dose and high energy implants achieving low level of activation

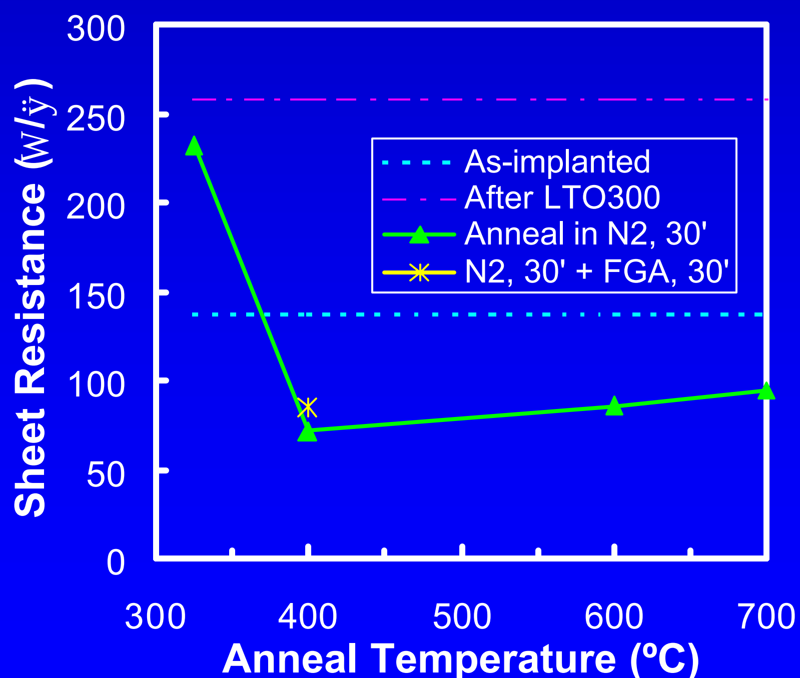


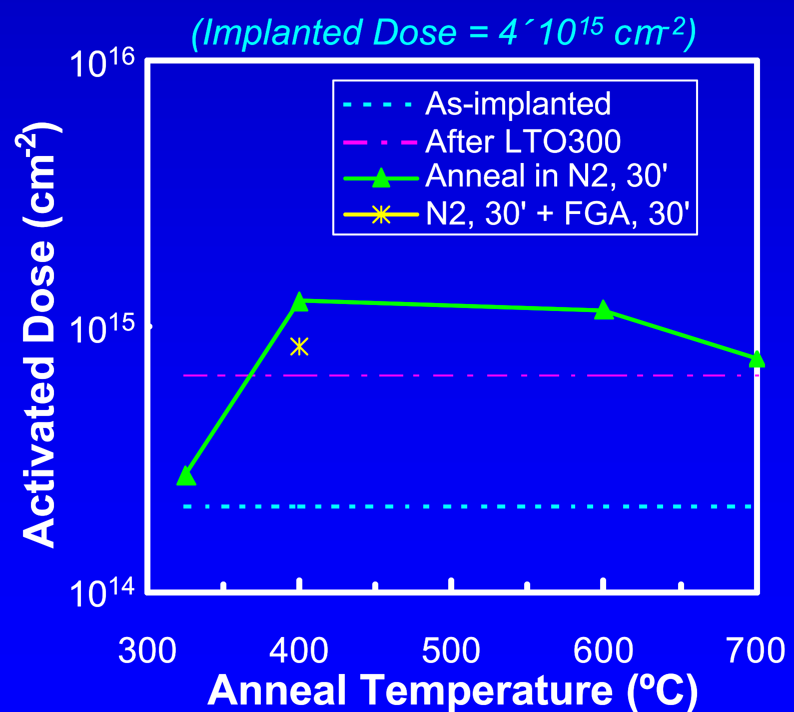
(Dunlap, *Phys. Rev.*, 1954)

P-Type Dopant Incorporation

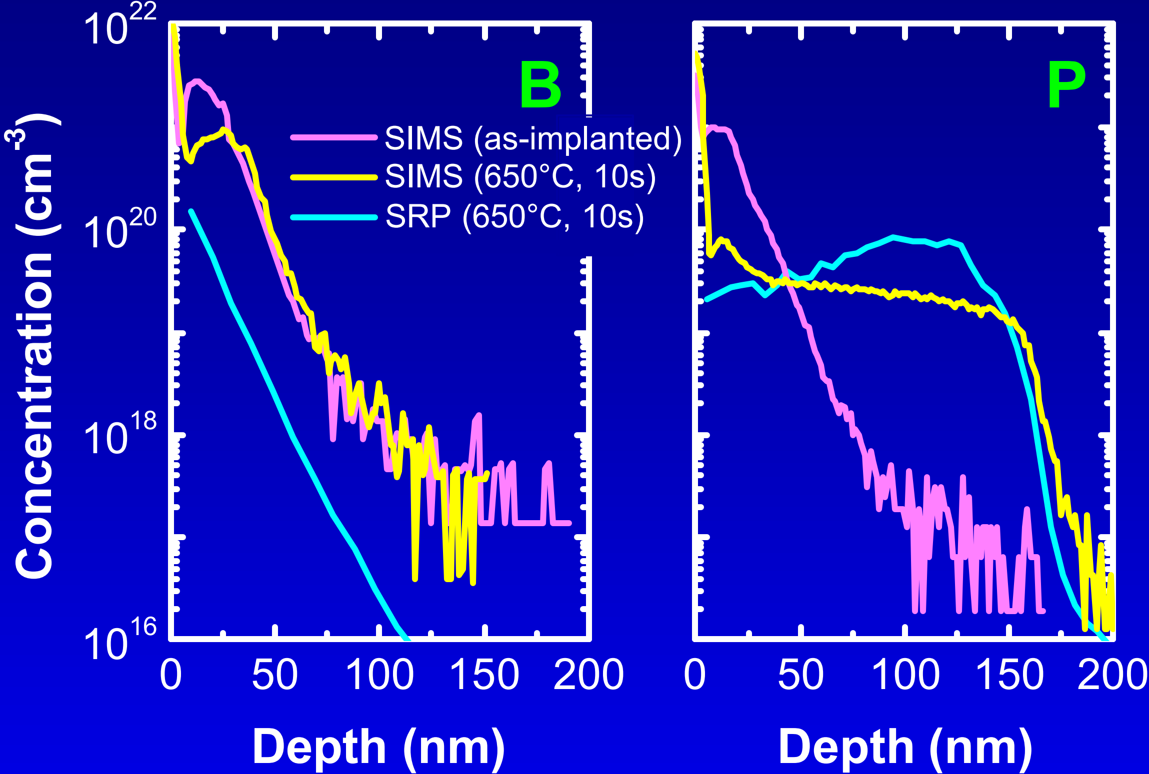
(Chui *et al.*, *IEEE IEDM*, 2002)

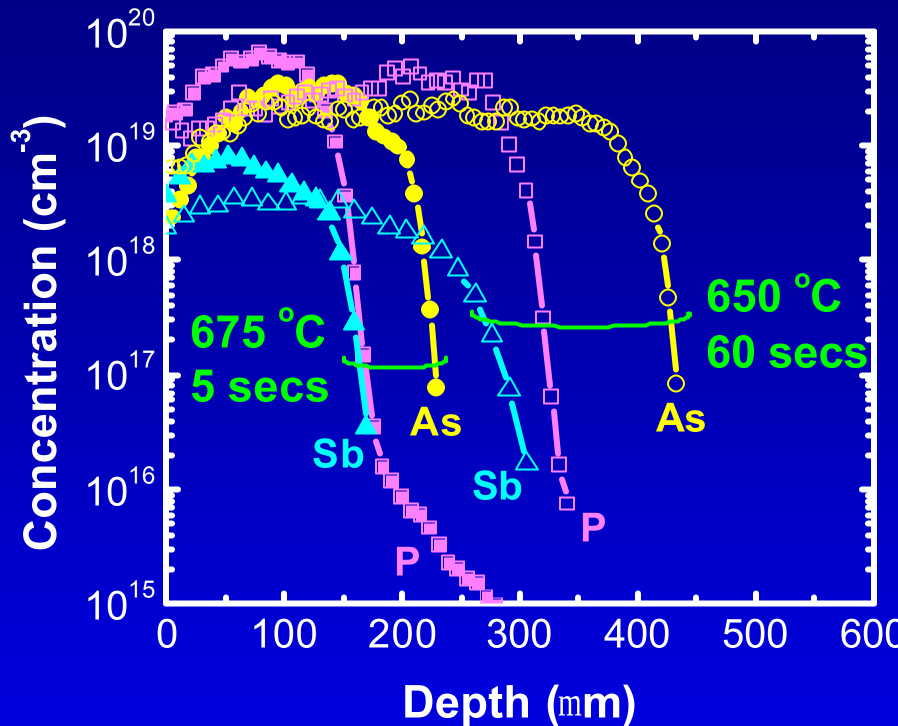






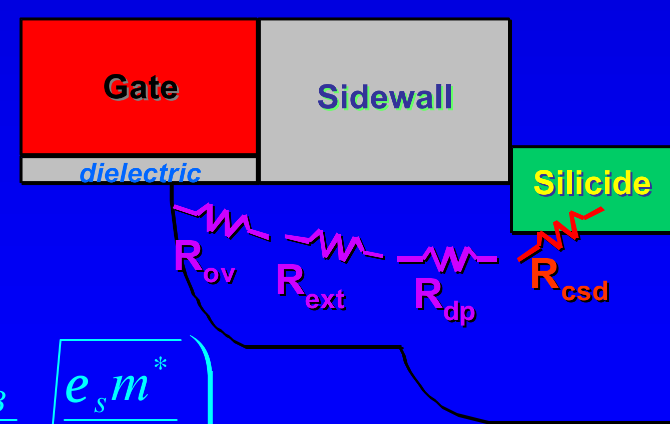
Conventional Ion Implantation Doping





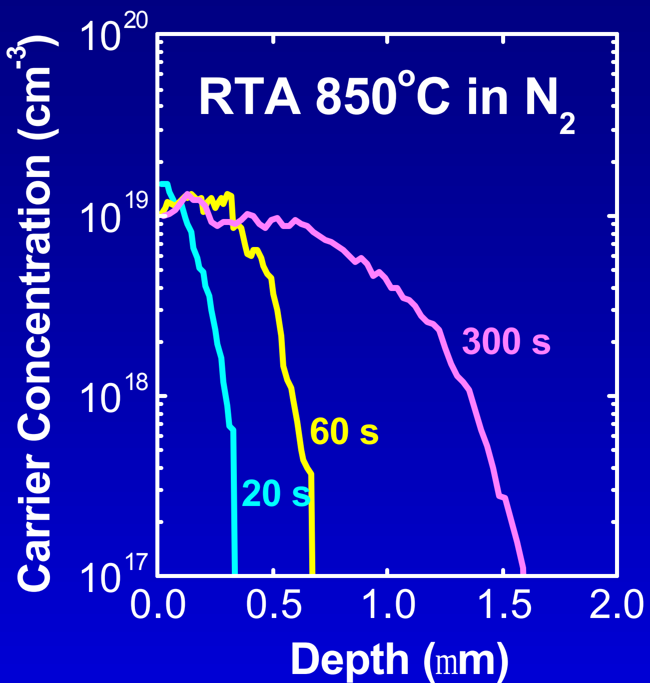
Dopants	Model	E_A (eV)	D^0 (cm^2/s)
P	$(n/n_i)^2$	2.07	4.38×10^{-2}
As	$(n/n_i)^2$	3.32	1.45×10^{6}
Sb	n/n_i	2.28	1.189×10^{1}

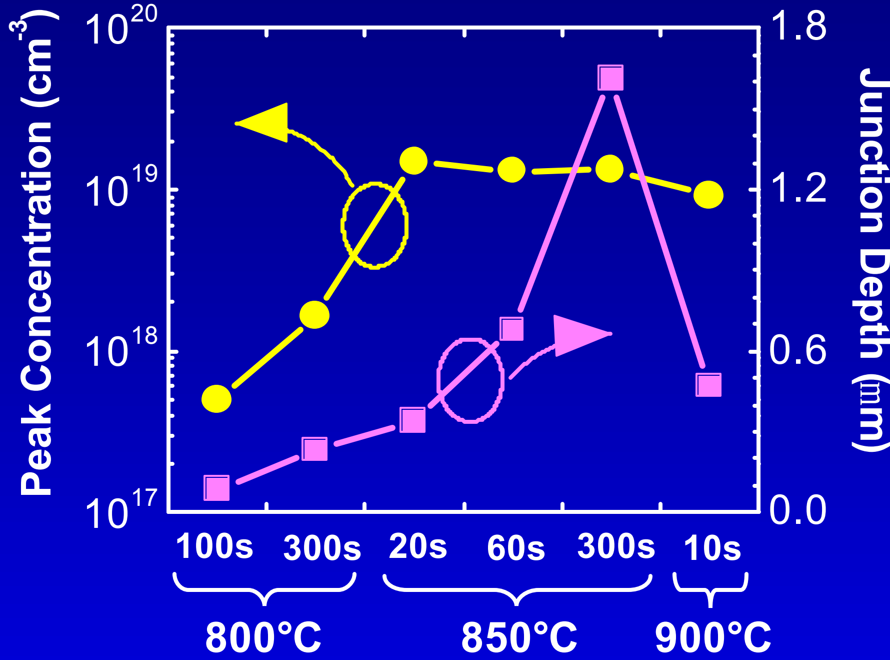
(Chui *et al.*, *APL*, 2003)



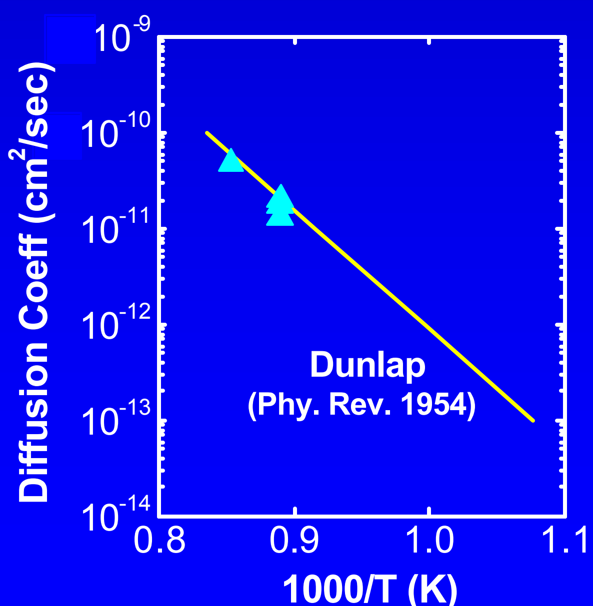
$$r_c = r_{c0} \exp\left(\frac{2 f_B}{\hbar}\sqrt{\frac{\varepsilon_s m^*}{N_{sub}}}\right)$$

Solid Source Diffusion from PSG





(Chui *et al.*, *IEEE IEDM*, 2003)



Some advantages:

1) Avoid non-equilibrium effects like transient enhanced diffusion (TED) from defects

2) Require standard materials, e.g. phosphosilicate glass (PSG), as dopant source

3) Allow shallow junction with peak concentration at surface with RTA

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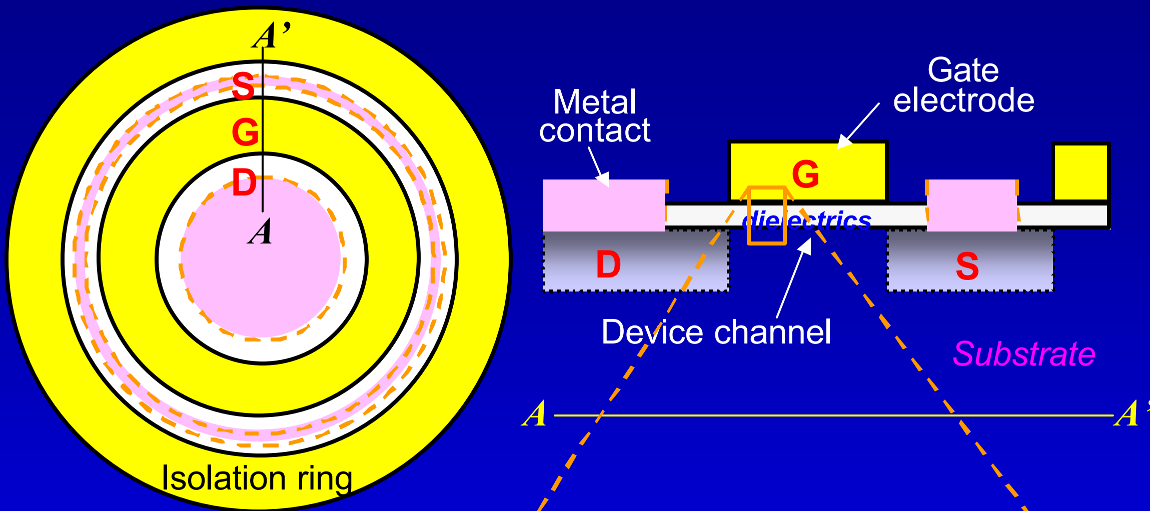
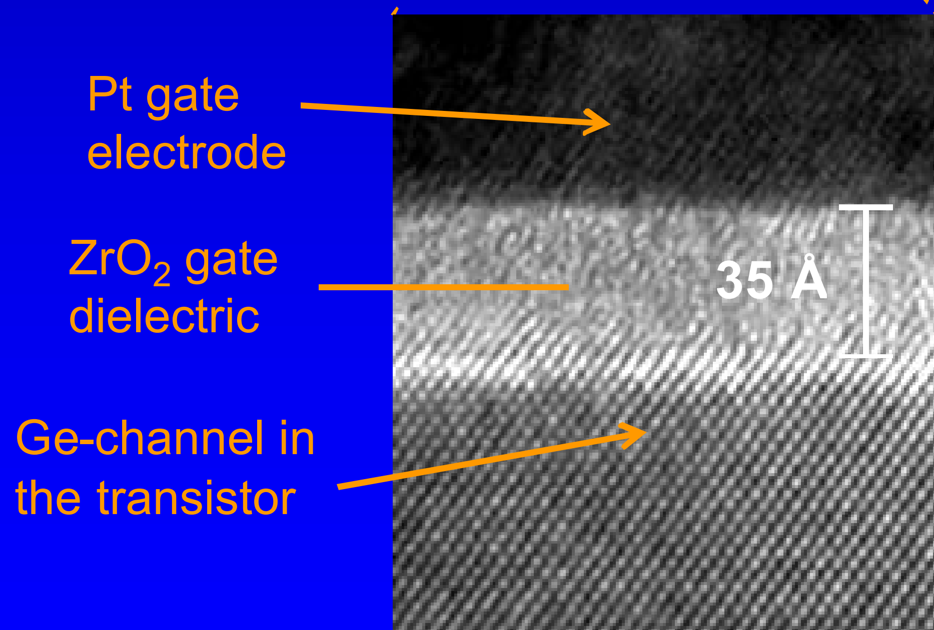
The Stanford Sub-400°C Germanium *P*-MOSFET Process

1) (100), ~10^{16} cm^{-3} n-Ge
2) Surface Preparations
3) ZrO_2 deposition at room temp*
4) Litho for metal gate liftoff
5) Pt evaporation and liftoff
6) Self-aligned S/D implant
7) Dopant activation at 400ºC
8) Litho for contact etch and metallization
9) ZrO_2 contact etch**
10) Ti-Al evaporation and liftoff
11) FGA at 300ºC

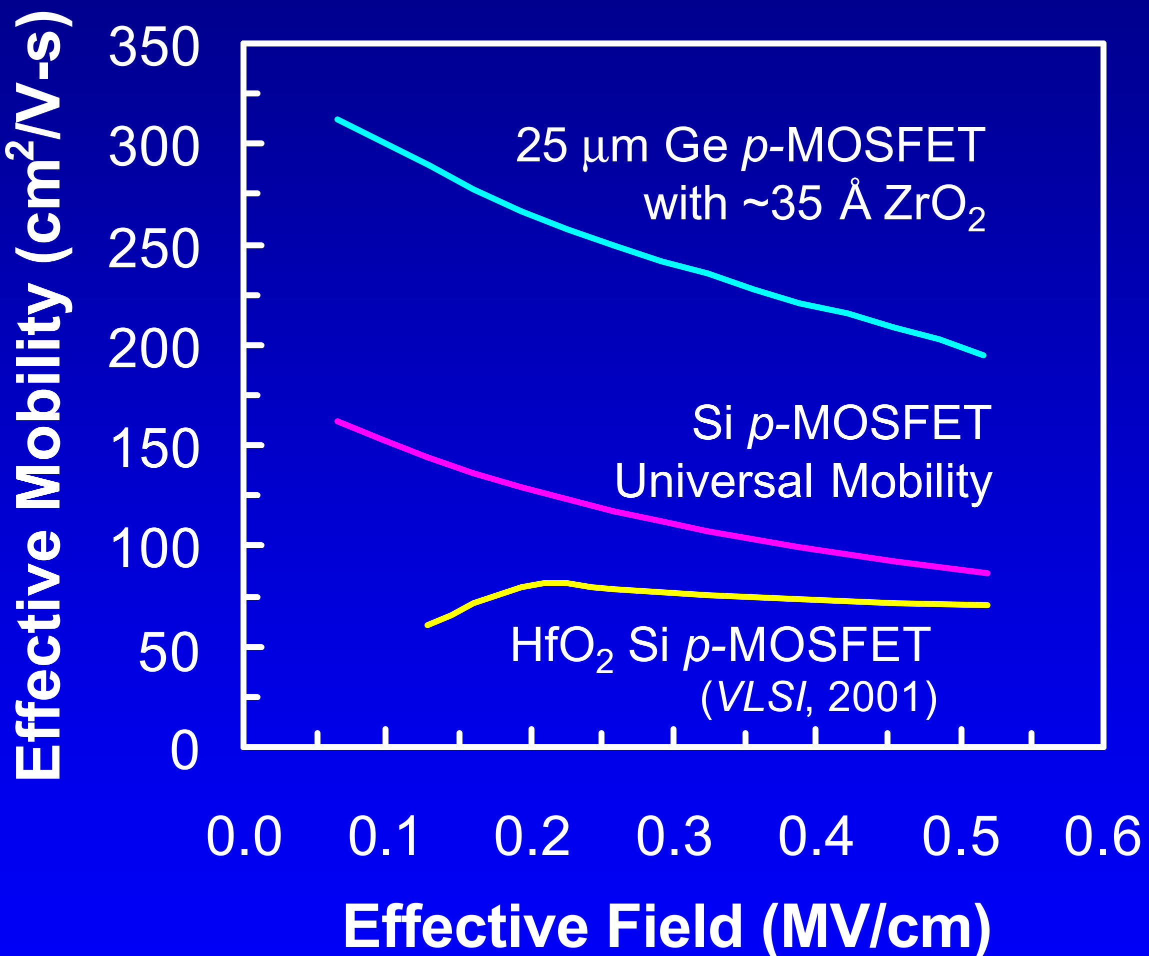




* *Collaborations with D. Chi, B. B. Triplett, & P. C. McIntyre from MSE, Stanford*
** *with M. Liao from MSE, Stanford*

(Chui *et al.*, *IEEE IEDM*, 2002)

Hole Mobility Enhancement with Ge



(Chui *et al.*, *IEEE IEDM*, 2002)

- ⇒ 1st demonstration of metal gate on high-κ on Ge MOSFETs
- ⇒ 2× mobility vs. Si universal mobility
- ⇒ 3× mobility vs. Si high-κ *p*-MOSFETs
- ⇒ 400°C maximum temperature process
- ⇒ All the processing were done at Stanford (EE and MSE)

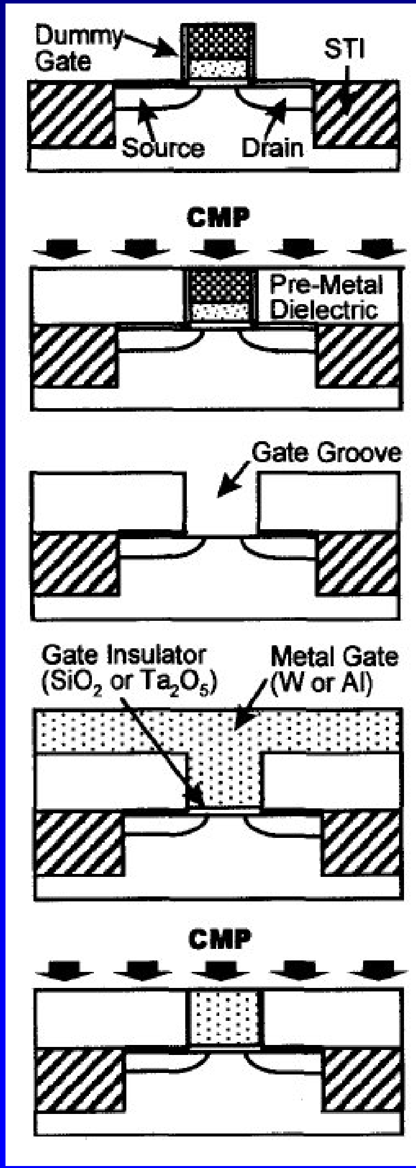
Requirements and Solutions of Metal Gate High-κ MOSFET Integration

Integration Requirements:

- Thermal stability of the metal gate high-κ gate stack during conventional self-aligned dopant activation
- Resemblance to the conventional VLSI device structure
- Compatibility with the Si mainline equipment set
- Inclusion of standard isolation together with planar geometry

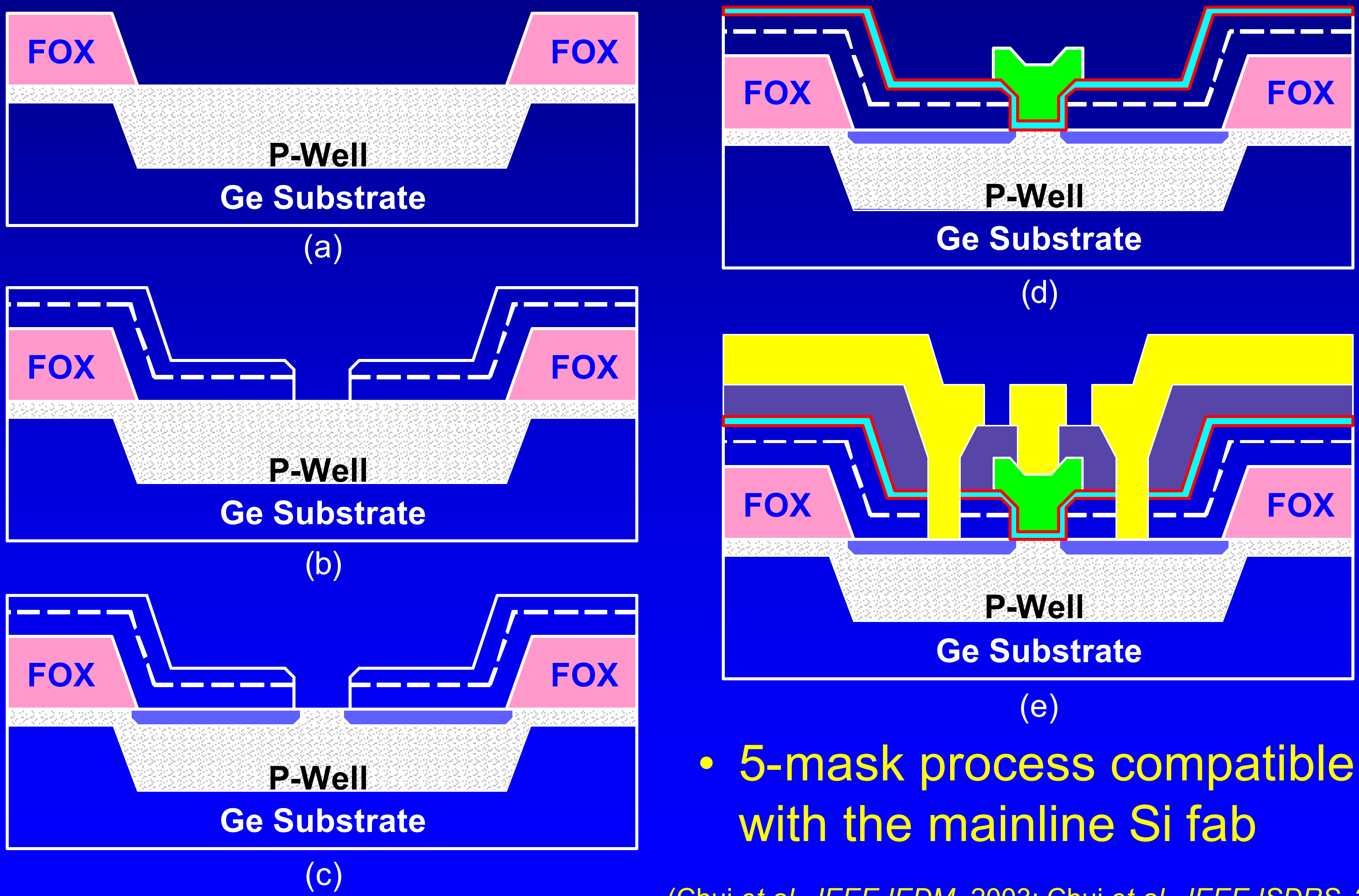
Present solutions:

- Replacement or damascene gate process



(Yagishita *et al.*, IEEE *IEDM*, 1998)

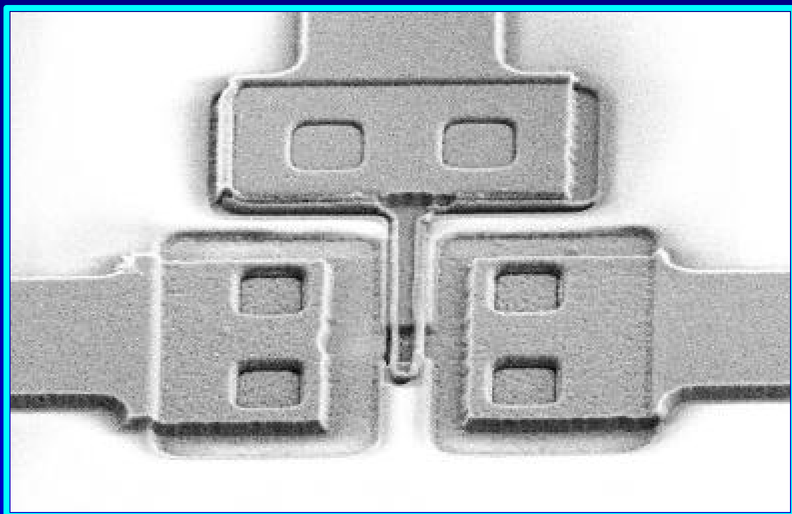
The Novel Self-Aligned Gate-Last Metal Gate High-k MOSFET Process

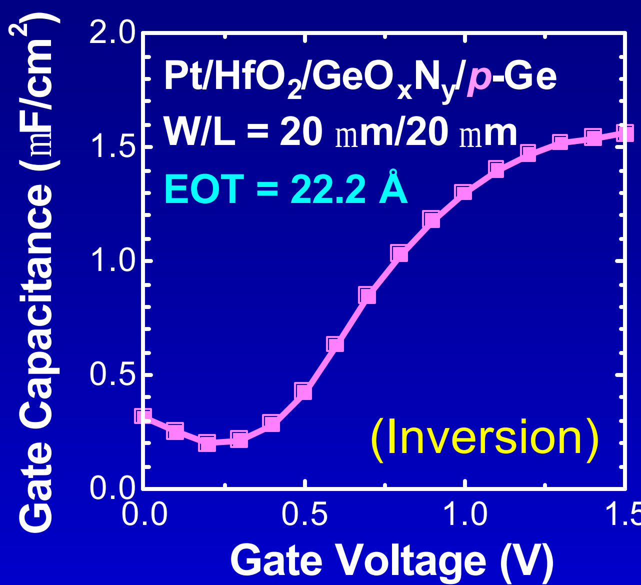


- 5-mask process compatible with the mainline Si fab

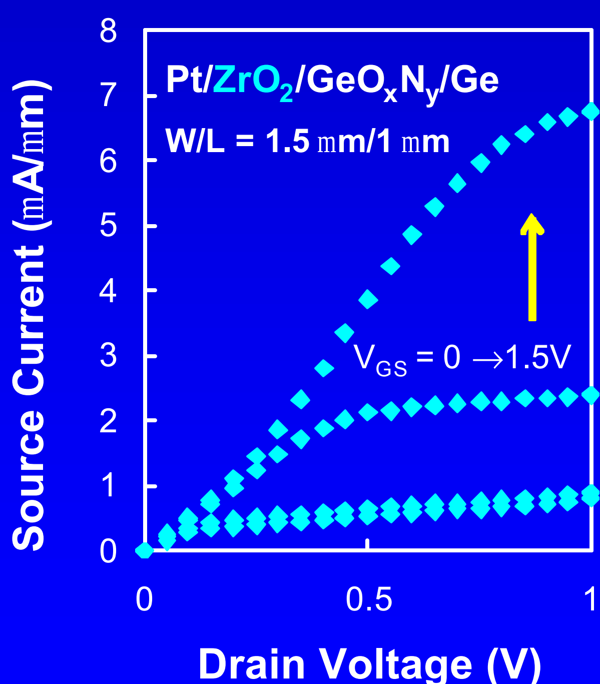
(Chui *et al.*, *IEEE IEDM*, 2003; Chui *et al.*, *IEEE ISDRS*, 2003)

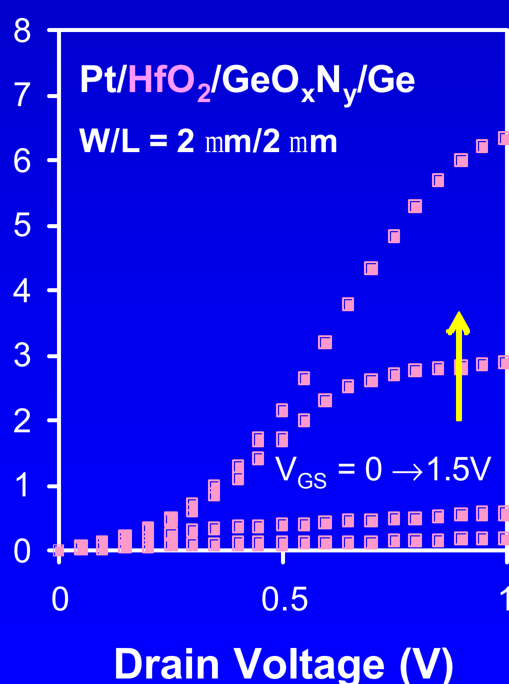
Ge *N*-MOSFET Characteristics





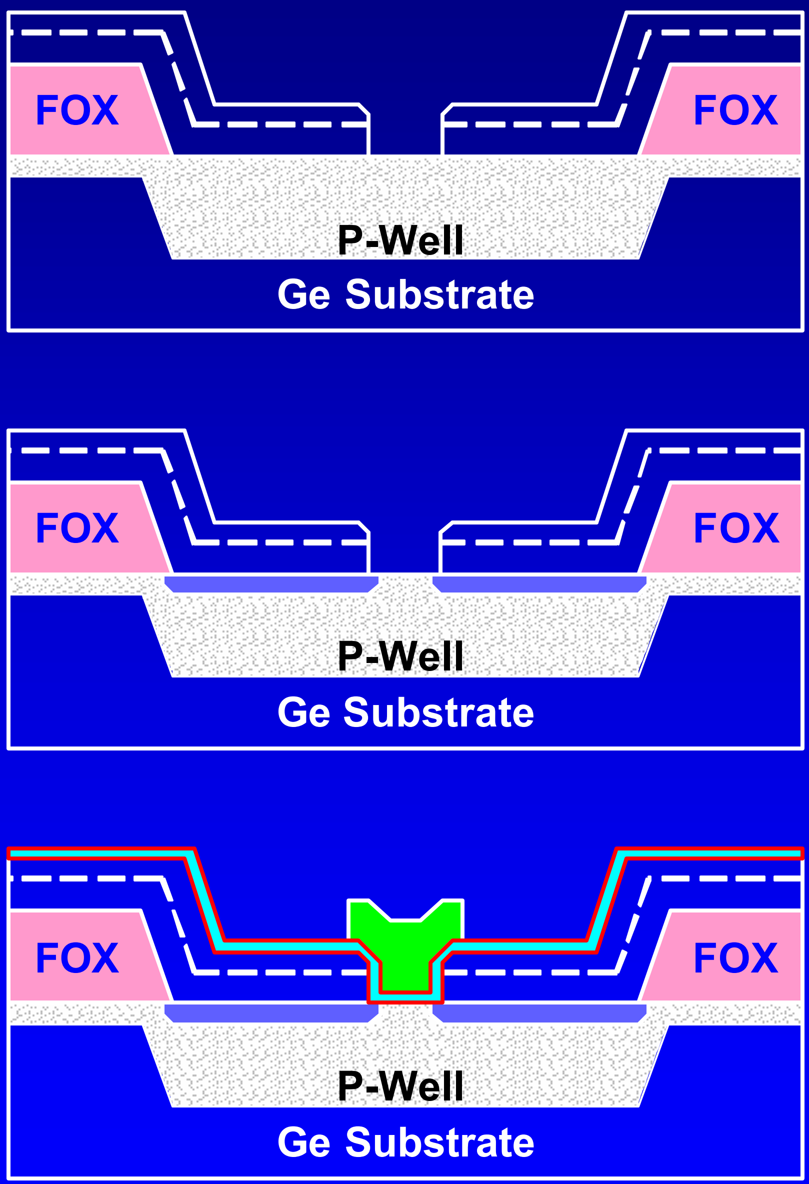
(Chui *et al.*, *IEEE IEDM*, 2003)





- 1st proof of concept Ge *n*-MOSFETs with both ZrO_2 & HfO_2 dielectrics and Pt gate electrode fabricated
- Functional *n*-MOSFETs with channel length down to 1-2 μm

Process Versatility



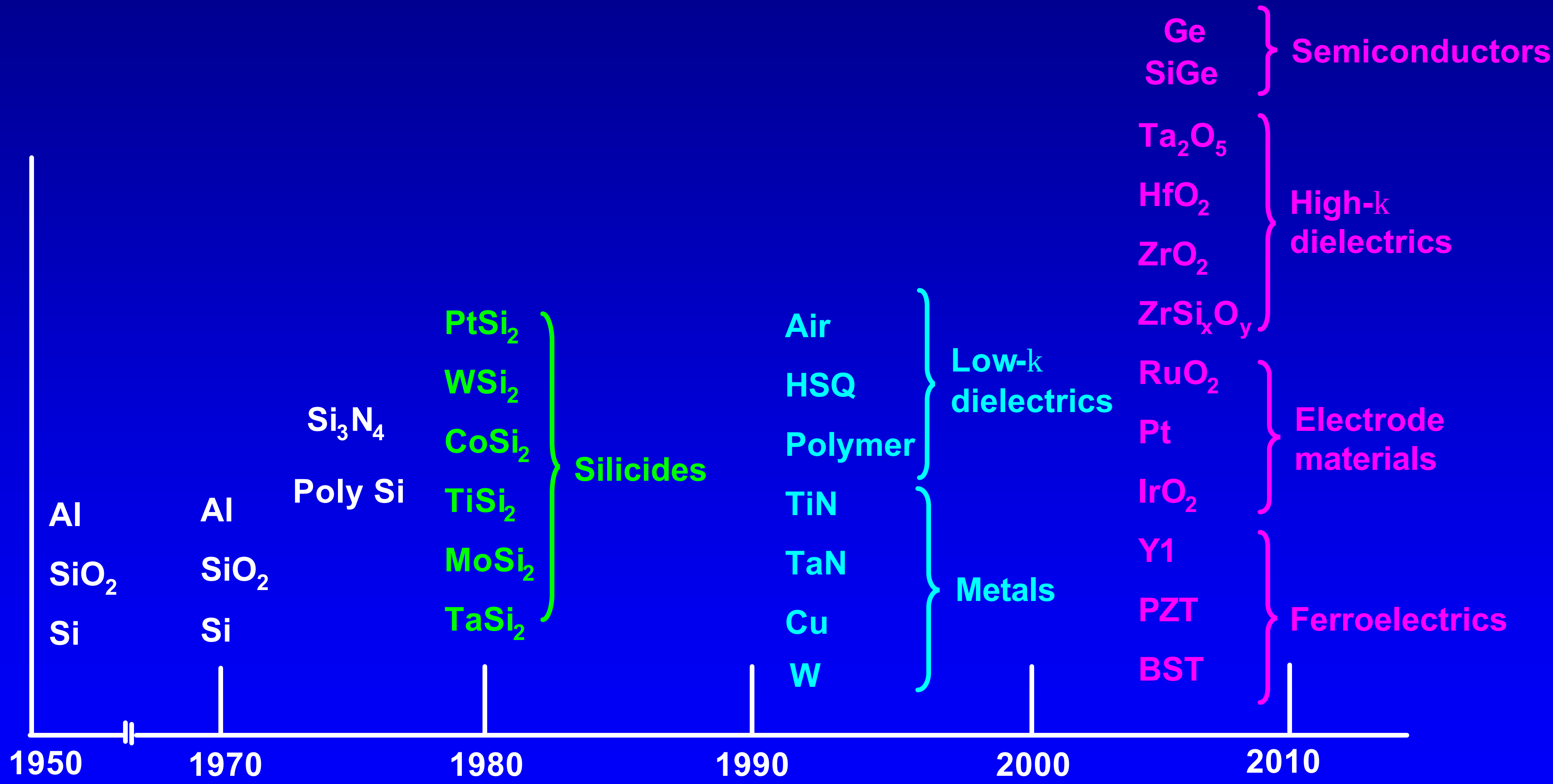
(Chui *et al.*, *IEEE IEDM*, 2003)

- Stringent thermal stability requirement relaxed without the need of the more-involved replacement or damascene process
- Highly selective etch of metal gate vs. high-κ, and high-κ vs. Ge not necessary on the thick LTO buffer
- Lightly-doped drains (LDD) possible with lower wt% PSG inward spacers
- CMOS formation by selective PSG removal followed by blanket BSG
- Elevated source/drains with doped-Ge instead of PSG

Outline

- Ge CMOS Motivations
- Ge MOS Gate Dielectric Technology
  - ⇒ UVO Oxidation of Metal
  - ⇒ ALD of Metal Oxides
- Ge Dopant Incorporation Technology
- Ge MOSFETs with High-κ and Metal Gate
- Conclusions

New Materials for CMOS



Conclusions

- 1st demonstration of Ge MOS capacitors incorporating high-κ gate dielectrics (ZrO_2 & HfO_2) deposited using either UVO or ALD
- 1st demonstration of high Ge surface *p*- and *n*-type dopings by either ion implantation or solid source diffusion
- 1st demonstration of Ge *p*- and *n*-MOSFETs with high-κ gate dielectrics and metal gate down to 1-2 μm channel length
- Future work in the areas of Ge surface cleaning, passivation, and dopant activation

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