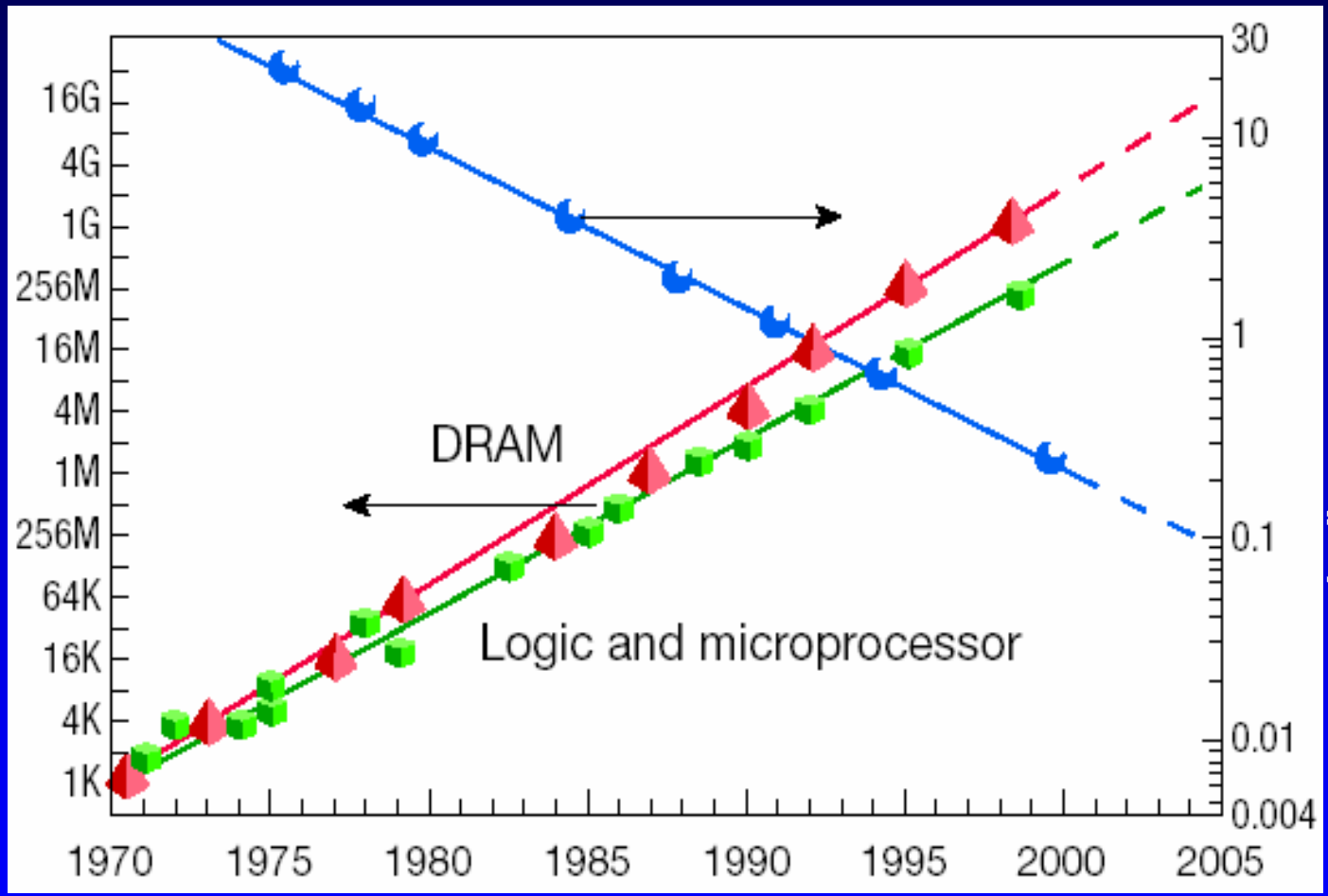
Challenges and Opportunities for Future Nanoelectronic Devices

Ken Uchida

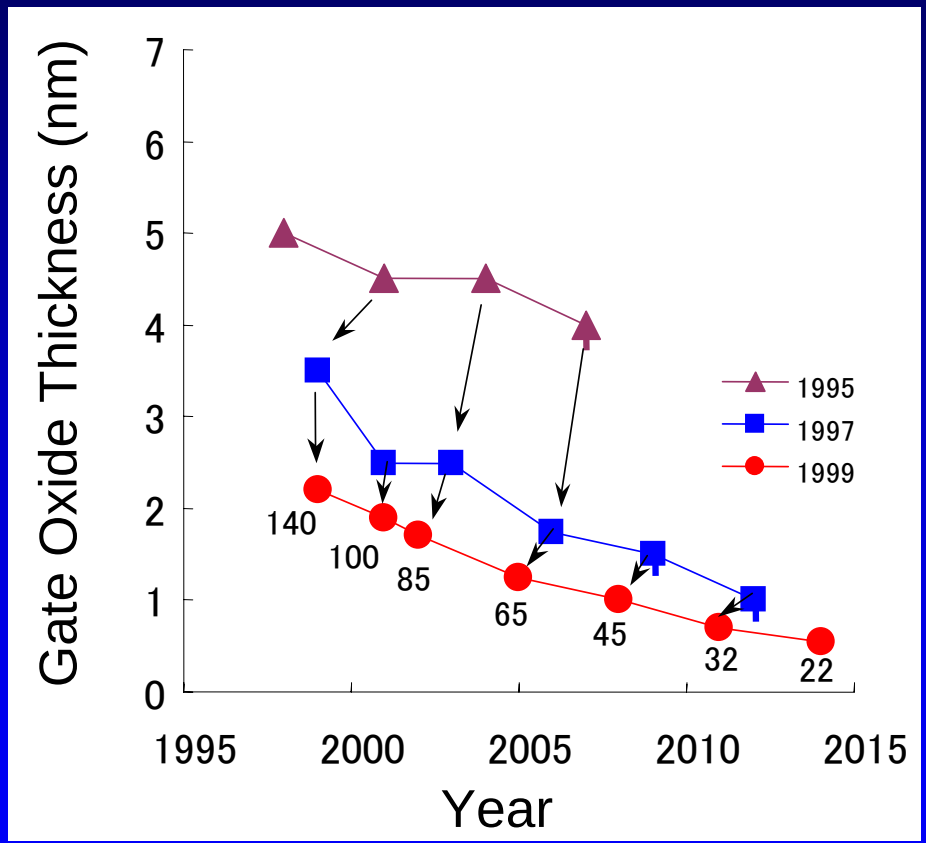
Toshiba Corporation / Stanford University

Scaling Trend of MOSFETs - General -

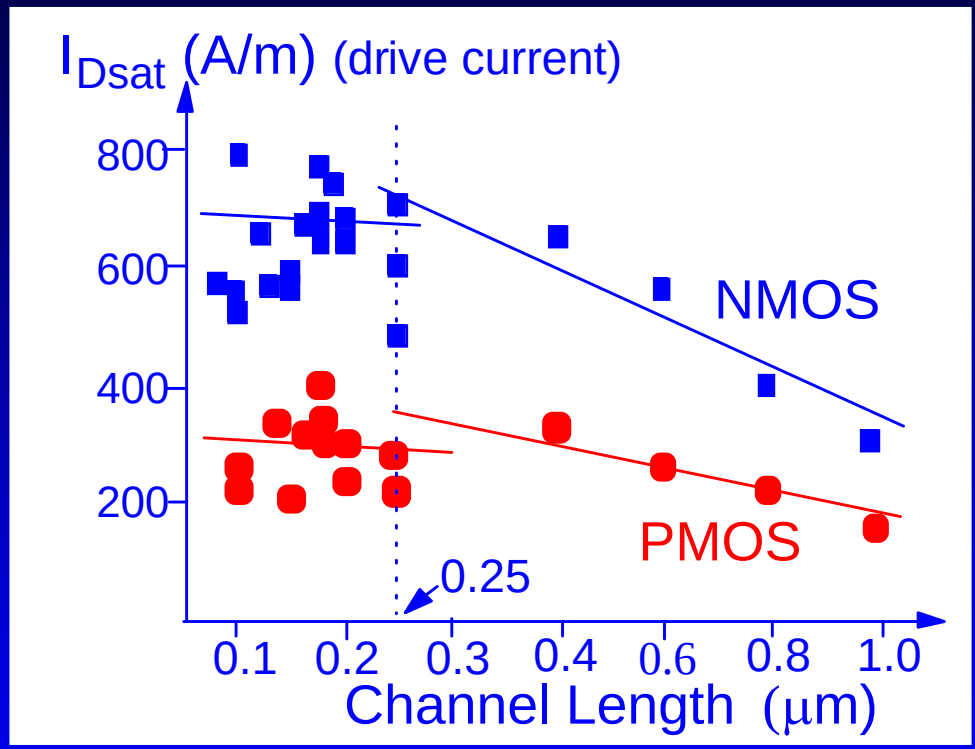


A. I. Kingon et al., Nature **406**, 1032 (2000).

Scaling Trend of MOSFETs
- Gate Oxide Thickness -

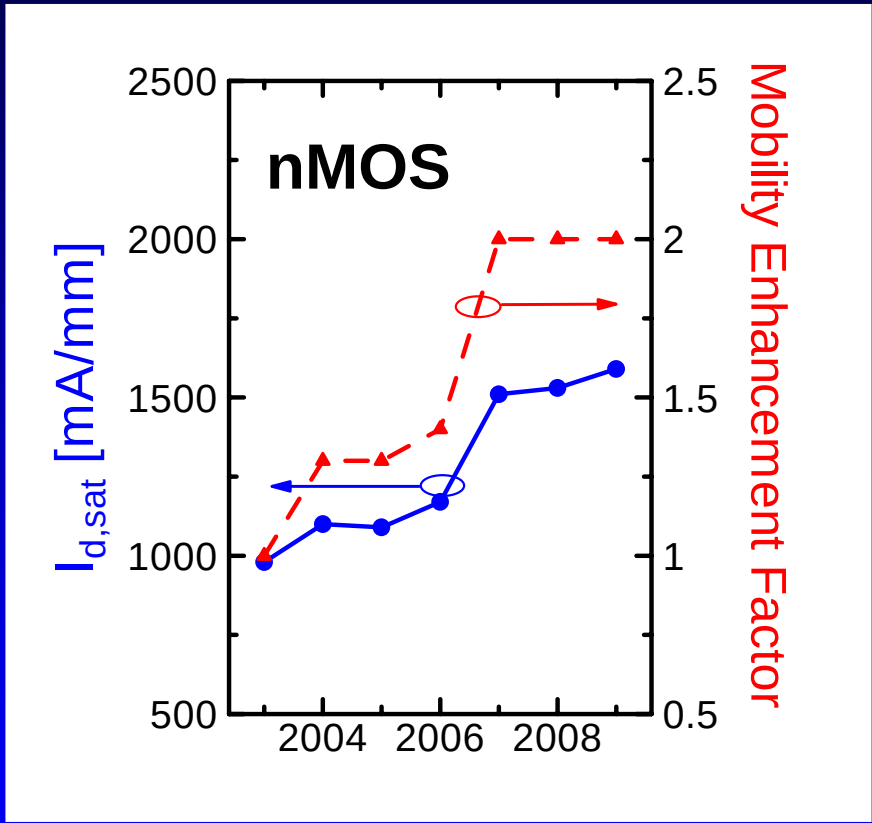


Saturation of Tr. Performance



Changhoon Choi, PhD Thesis in Dutton Group, Stanford Univ., 2002

Introduction of New Technology



Paradigm Change (I)

Scaling Technology Node

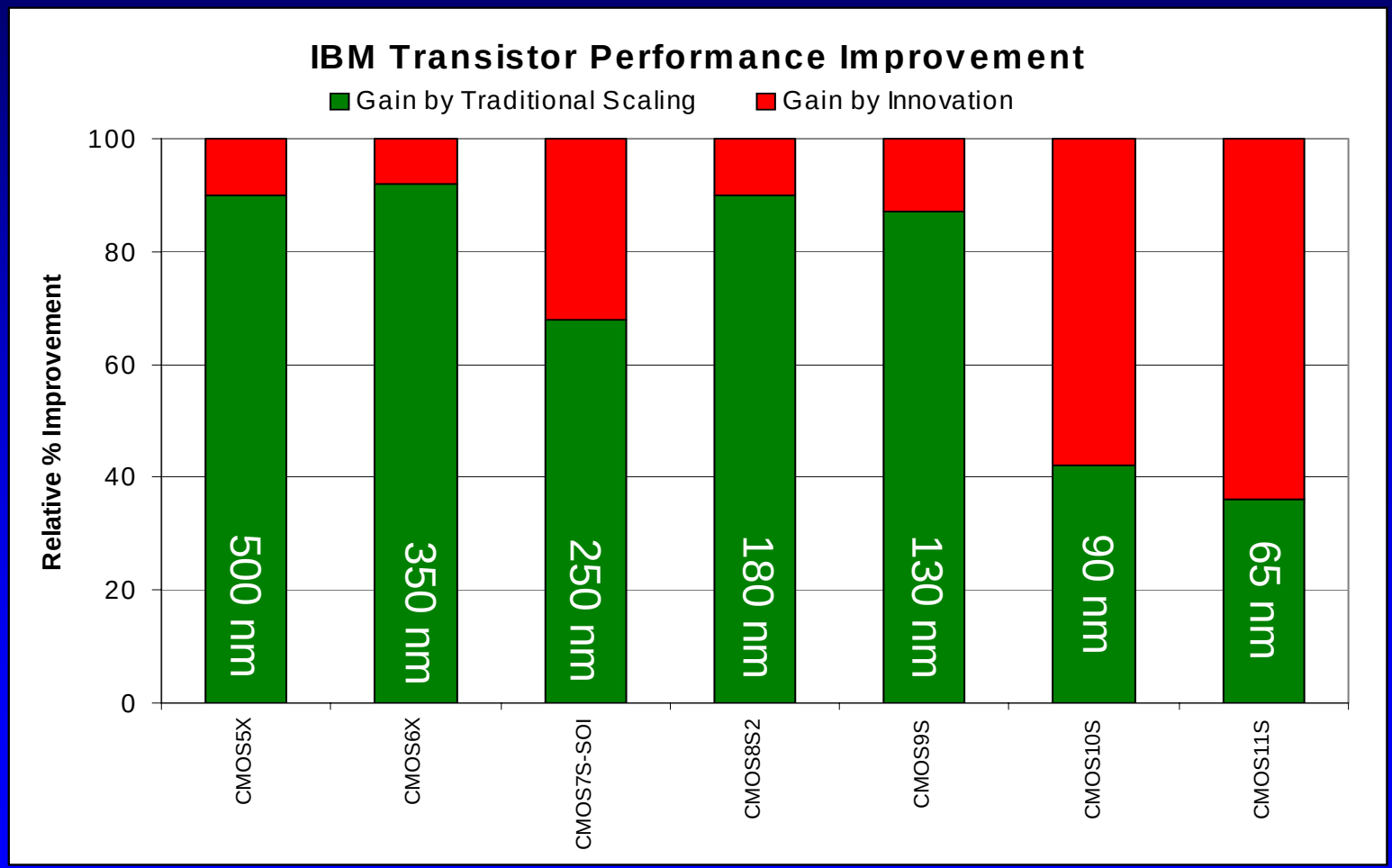
WAS Scaling Device Sizes

IS Scaling Device Sizes
+
Introducing New Technology

High-κ, Stressed Channel, Ultrathin-body SOI, Schottky S/D *etc.*

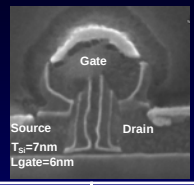
Innovation Overtakes Scaling in Driving Performance

- Innovation (invention) will increasingly dominate performance gains
  - Scheduled "invention" is now the majority component in all plans
    - Risk has increased significantly



Source: H. S. Philip Wong, Stanford Univ.

Time Horizon

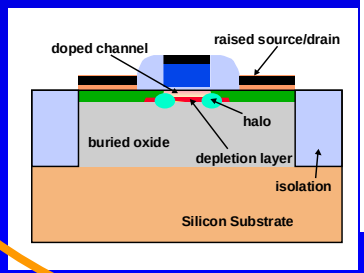


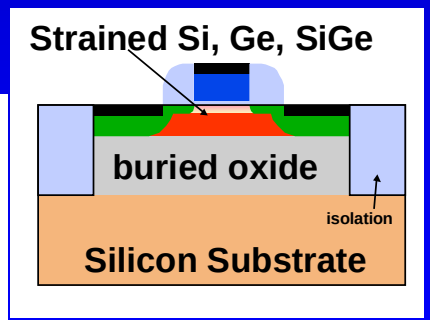
Proof of concept

Dawn of nano-era

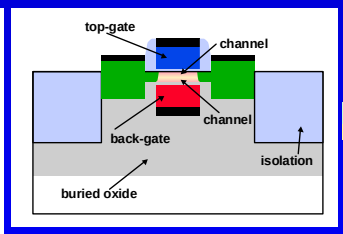
ITRS'01	2004	2007	2010	2013	2016	2019	2022	2025
General Litho.	90 nm	65 nm	45 nm	32 nm	22 nm	15 nm	10 nm	7 nm
Printed Gate	53 nm	35 nm	25 nm	18 nm	13 nm	9 nm	6 nm	4 nm
Physical Gate	37 nm	25 nm	18 nm	13 nm	9 nm	6 nm	4 nm	3 nm

High *k* gate dielectric

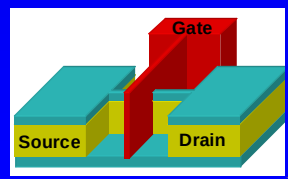


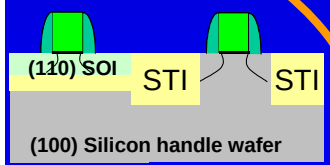


Metal gate



Double-Gate CMOS





Source: H. S. Philip Wong, Stanford Univ.

Today's Topic

- Ultrathin-body (UTB) MOSFETs
  - ✓ Better Short Channel Immunity
  - ✓ Lower Parasitic Capcitance
  - ✓ Reduced S/D Leakage
  - ✓ Lower Substrate Impurity Conc.
- Schottky Source/Drain MOSFETs
  - ✓ Better Short Channel Immunity
  - ✓ Lower Parasitic Resistance
  - ✓ Abrupt Junction

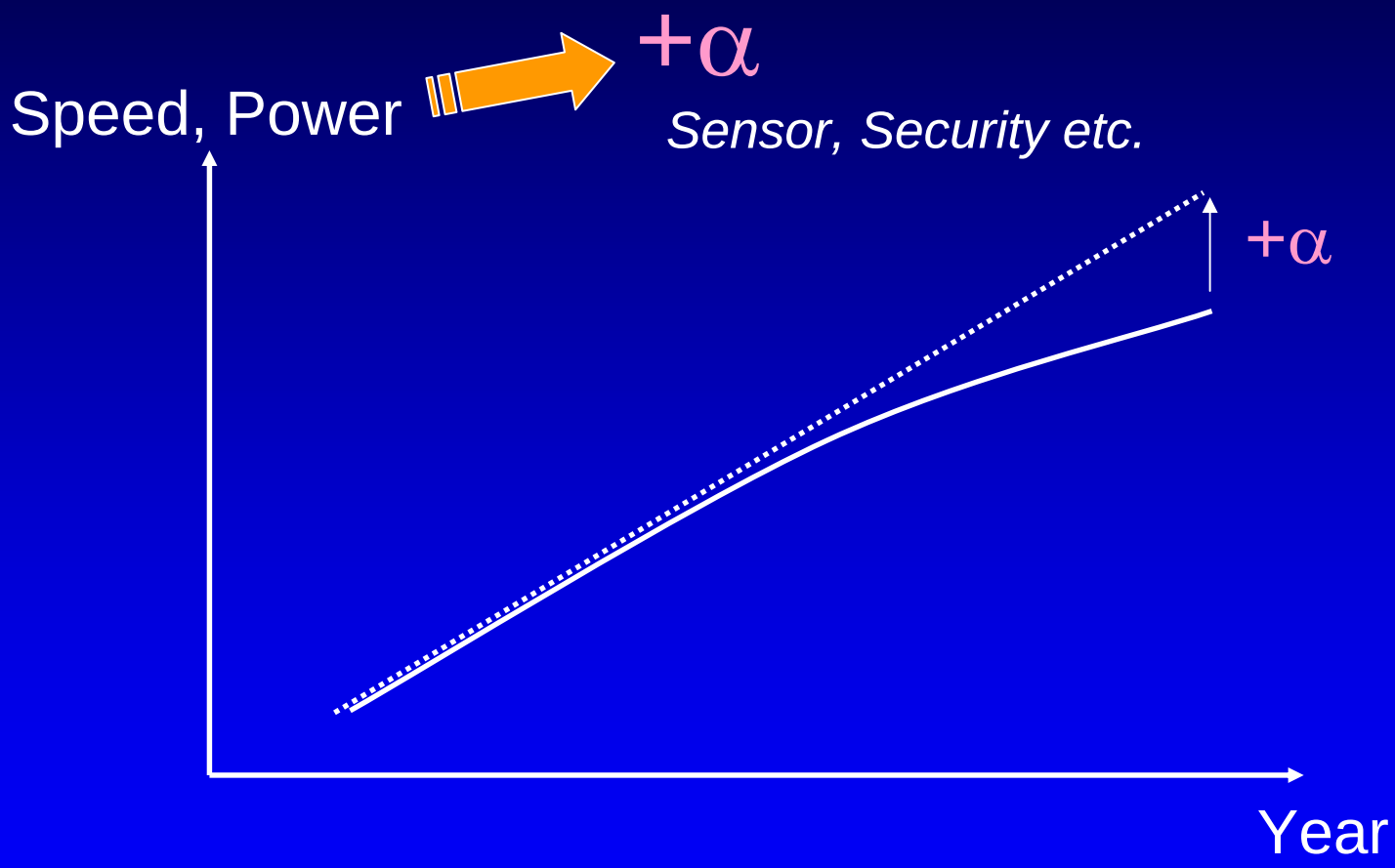
Requirement for LSI

- High Speed and Low Power

  Yes, it has been required and will be required in future as well.
  If we have high-performance LSI, we can do almost everything, such as complicated scientific calculation, MPEG encode, decode, game.

However, in ubiquitous era, requirements for LSI will be changed. LSI should *communicate* with environments and users *securely*.

Paradigm Change (II)



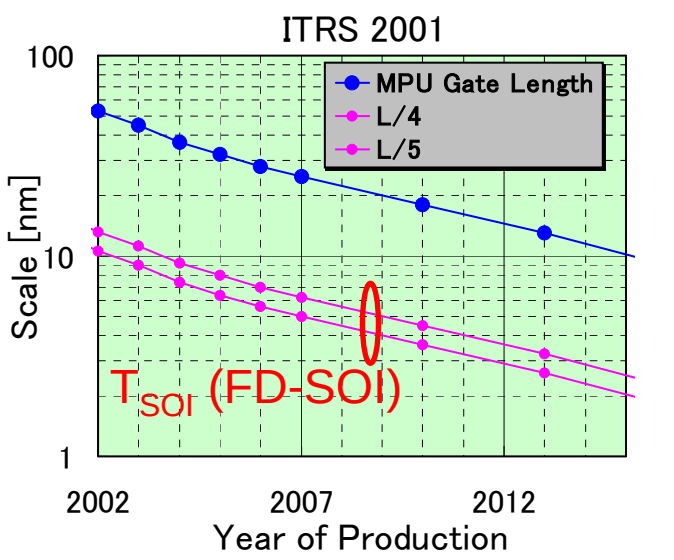
Outline

- Single-Electron Devices for Security Applications

Ultrathin-body MOSFETs

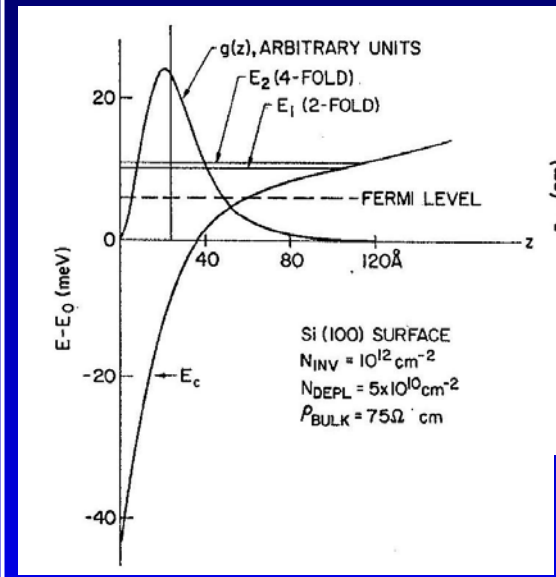
UTB MOSFETs

T_{SOI} of less than 10nm is required.

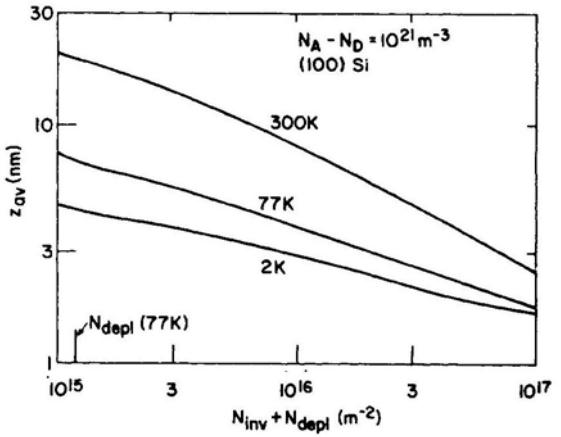


UTB (Ultrathin-body SOI) Tr.

Wavefunction width is larger than 10nm

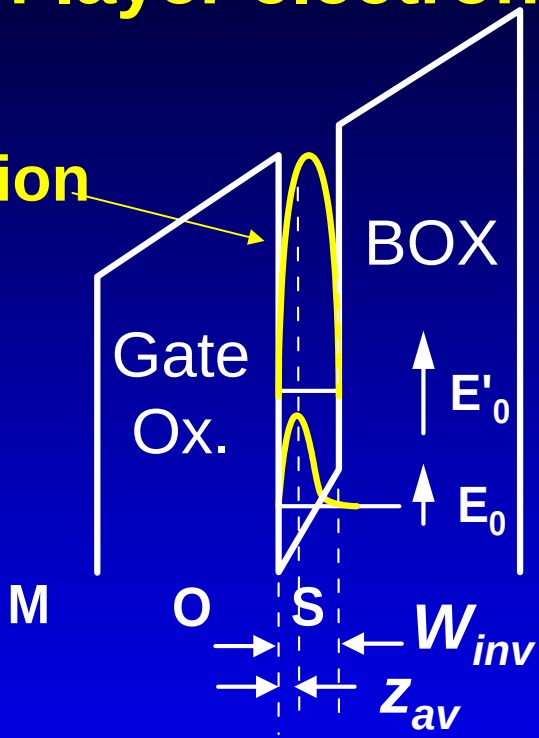


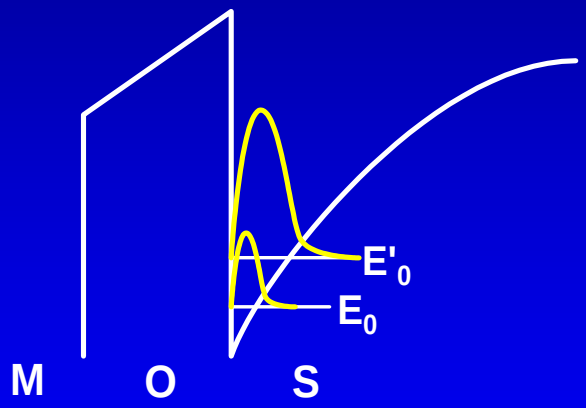
F. Stern *et al.*, *Phys. Rev.* **163** (1967) 816.



F. Stern *et al.*, *Phys. Rev.* **B5** (1972) 4891.

Quantum-mechanical confinement effects
on the inversion-layer electrons of UTB MOSFETs





E'_0: subband energy level in 4-fold valleys

E_0: subband energy level in 2-fold valleys

γz_{av}: effective thickness of inversion layer

W_{inv}: thickness of inversion layer

QMC effects on wavefunction are

- The decrease of z_{av} *and* W_{inv}
- The increase of *subband energy levels*

Impact of quantum-mechanical effects on the characteristics of UTB MOSFETs

As W_{inv} and z_{av} decrease, we can expect …

- the decrease of electron mobility μ_{eff} .

  $\mu_{ac} \propto |W_{inv}|$ / T_{SOI} **μ_{ac}: acoustic phonon-limited mobility**

  S. Takagi, IEDM97, p219.

- **the increase of Inversion-layer capacitance C_{inv} .**

  $C_{inv} = \varepsilon_{Si} / \gamma |z_{av}|$ **A. Hartstein, PRB38, p1235, 1988.**

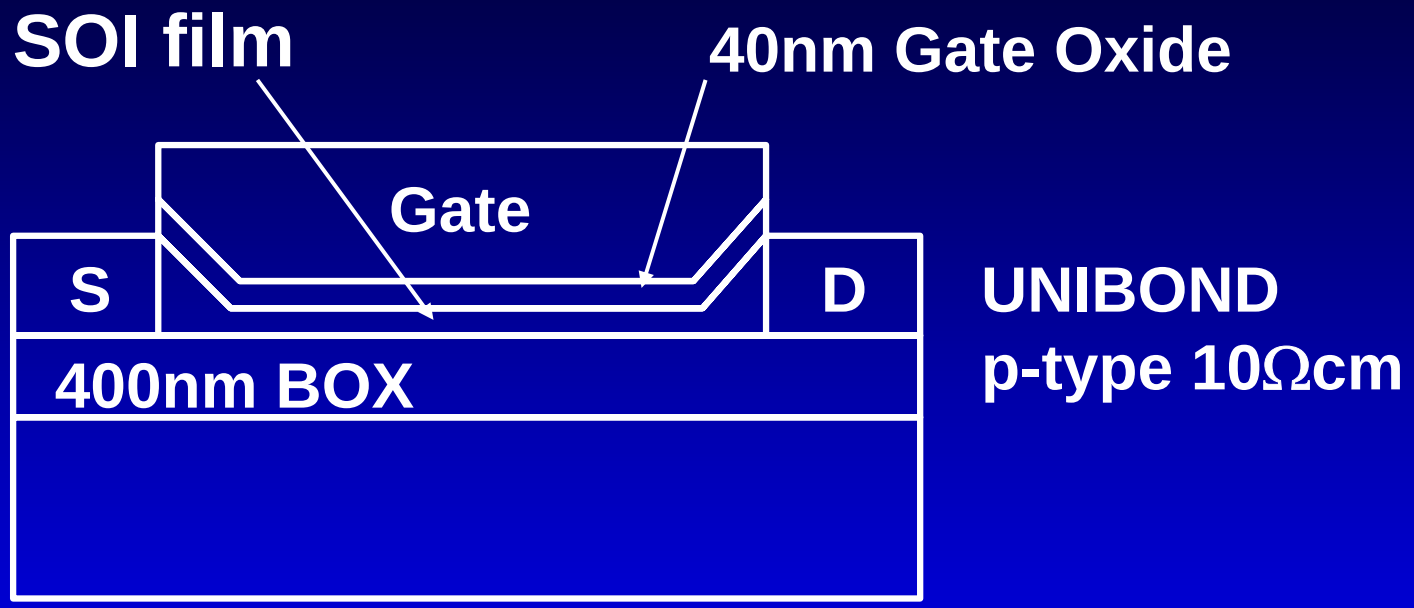
- **the increase of Gate-channel capacitance C_{gc} .**

  $1/C_{gc} = 1/C_{ox} + 1/C_{inv}$

As E_n and E'_n increase, we can expect …

- **the increase of V_{th} .**

Device Structure



L / W = 500 / 200μm

Recessed (Raised S/D) structure minimize the parasitic resistance.

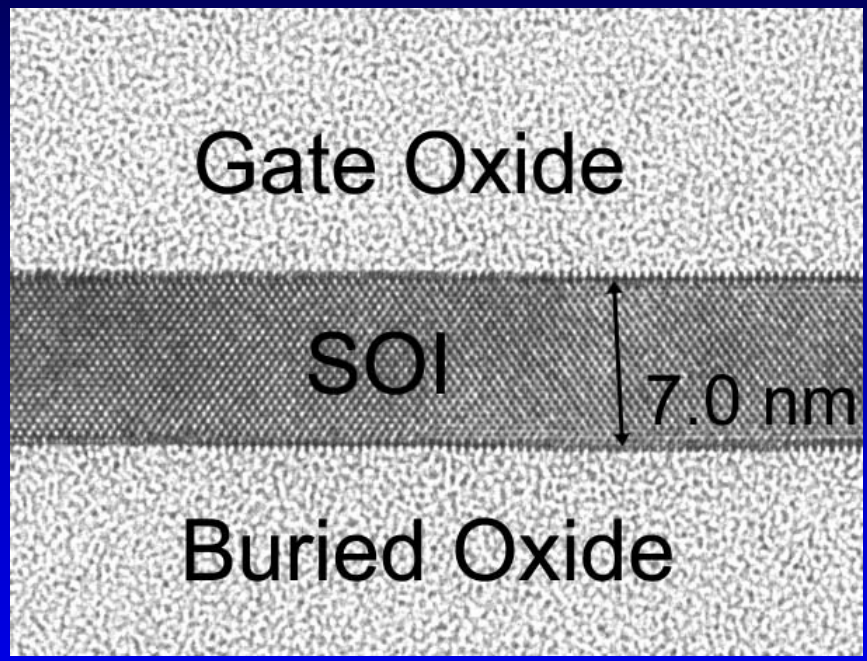
In order to investigate QM effects correctly,

- Uniform SOI film
- Stress-free SOI film

are required.

Thickness & Uniformity Evaluation

TEM Observation

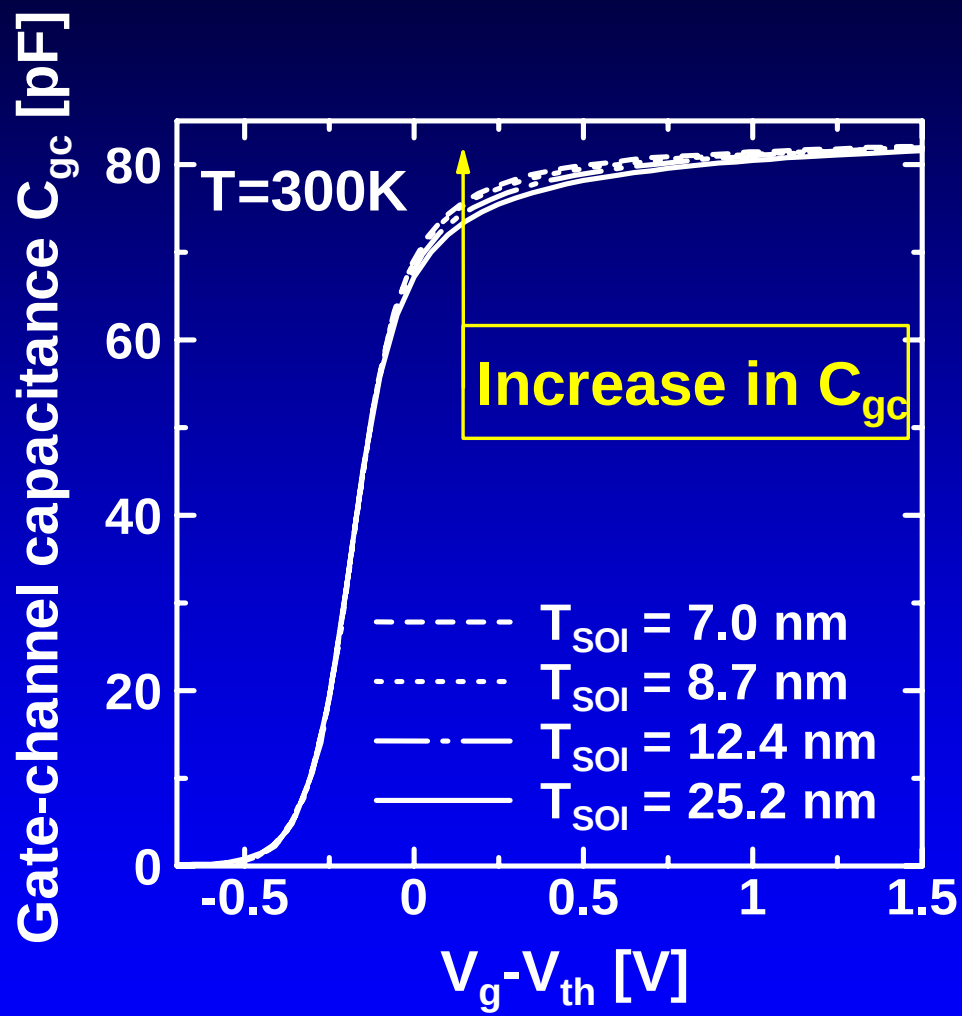


Cross section of the channel

- Ultrathin (7.0 nm ~ 12.4 nm)
- Uniform

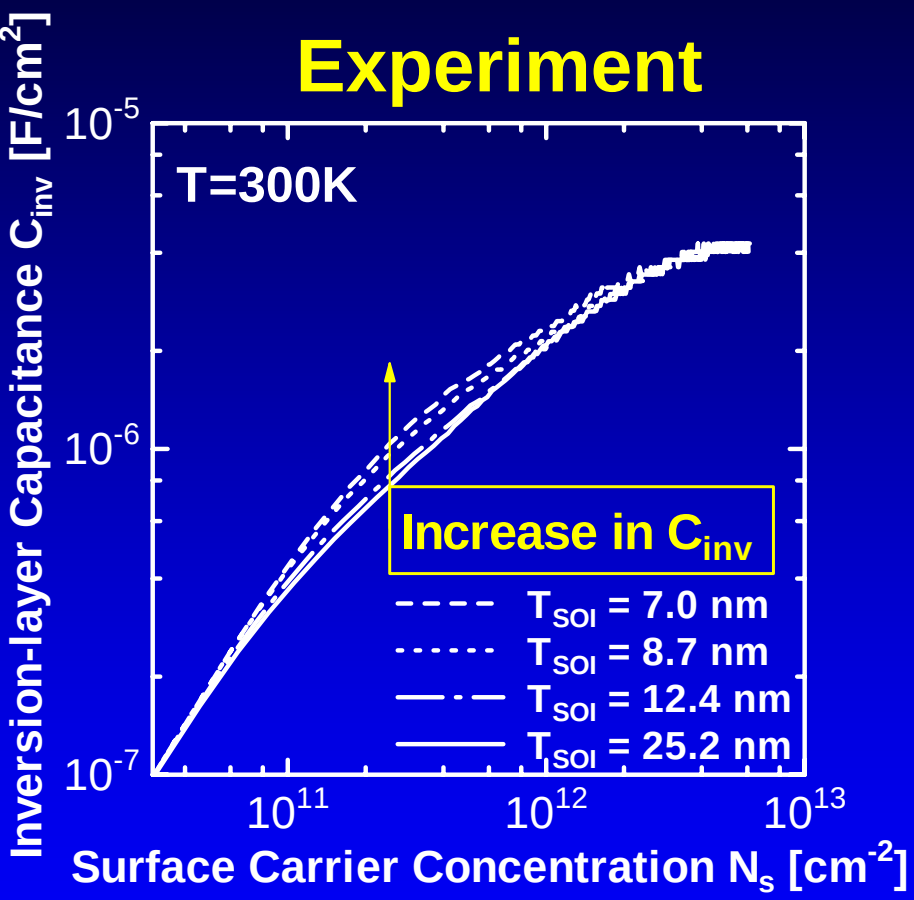
SOI films are successfully fabricated.

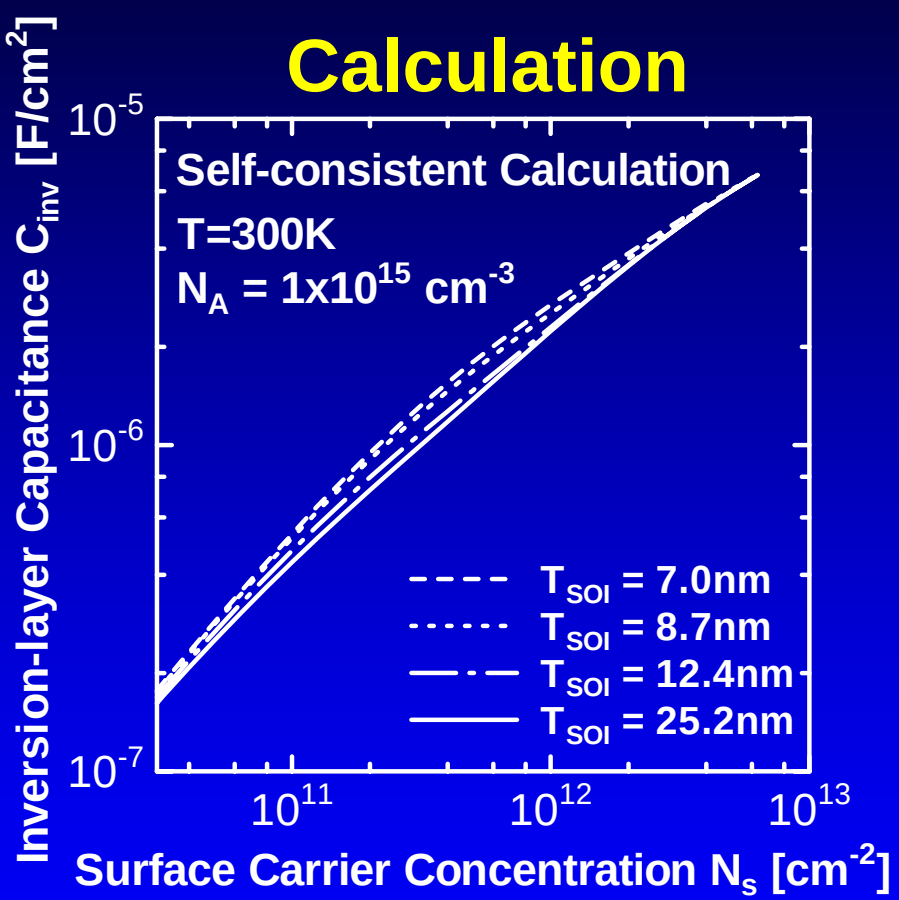
C_g-V_g characteristics for various T_{SOI}



C_{gc} increases as T_{SOI} decreases.

C_{inv}-N_s Characteristics for various T_{SOI}

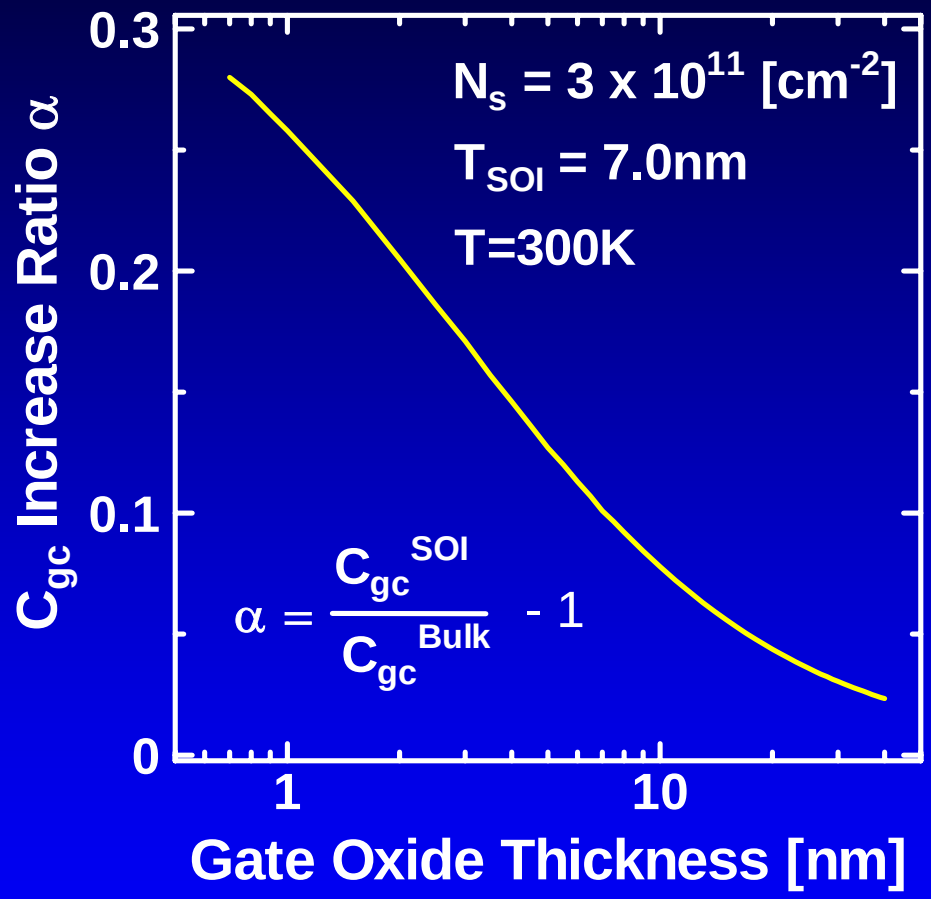




Experimental and Calculated results are consistent.

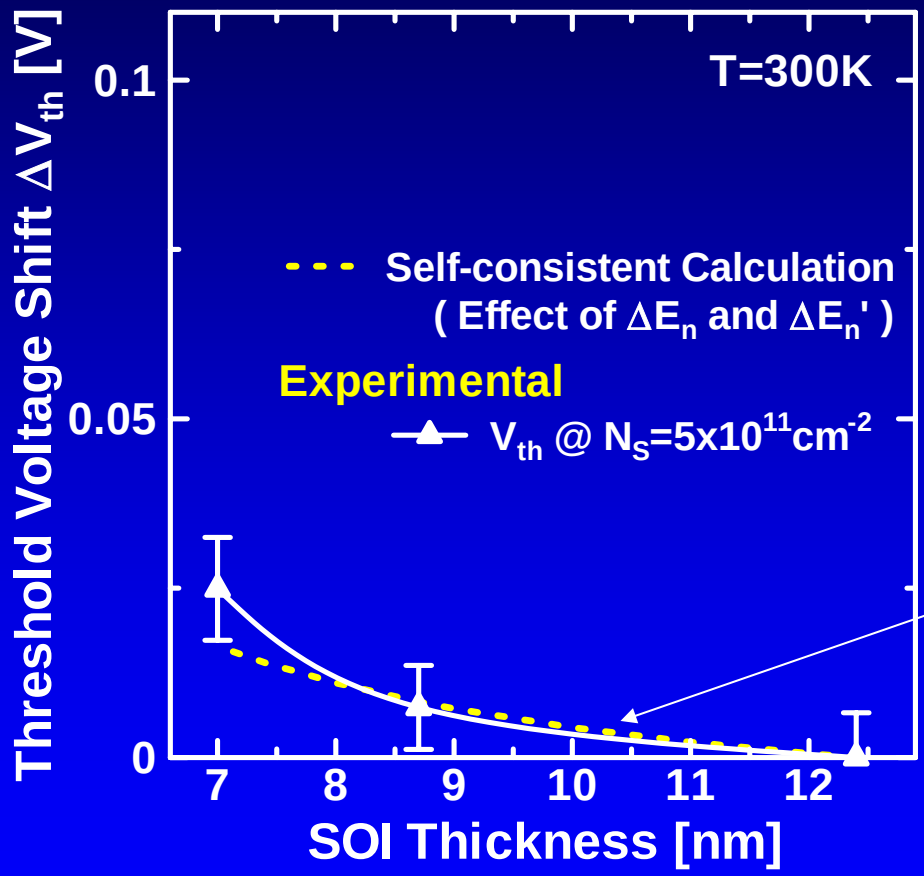
➡ ***The increase of C_{inv} and C_{gc} is due to QM confinement.***

C_{gc} Increase ratio as a function of T_{SOI}



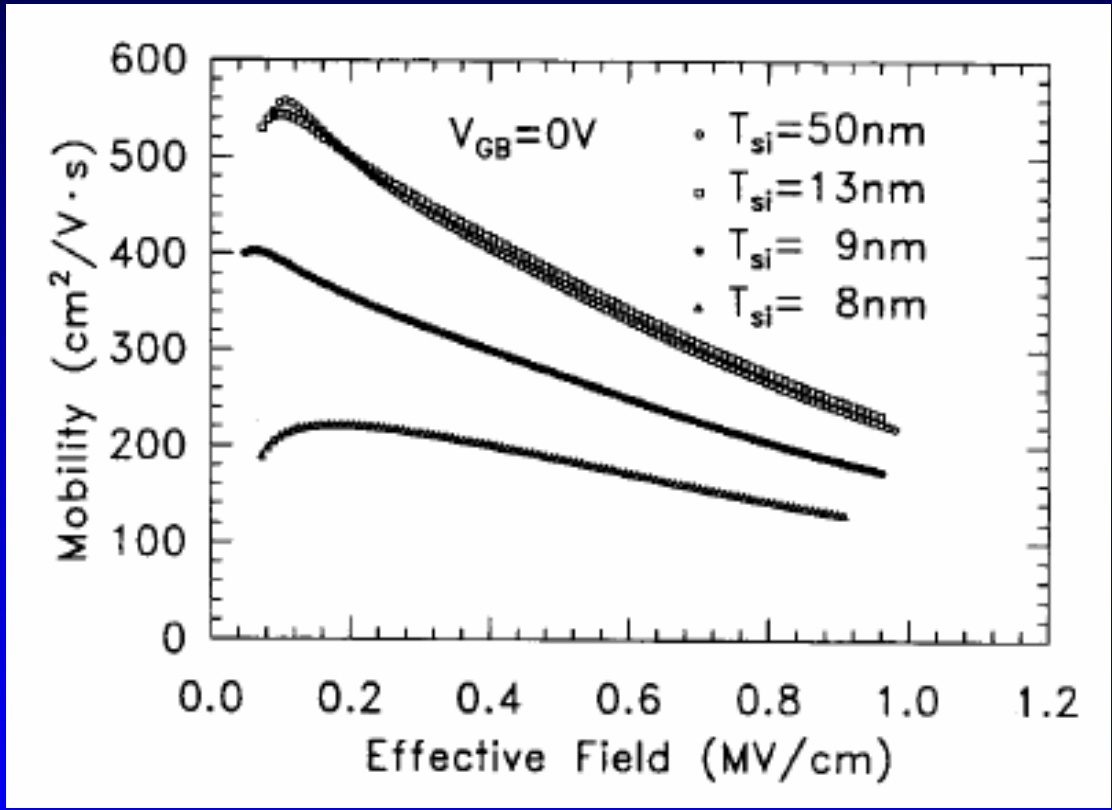
C_{gc} of 7nm UTB MOSFETs is 25% greater than that of bulk MOSFETs in 1nm T_{ox} regime.

V_{th} determined from C-V



***Agree* well !**

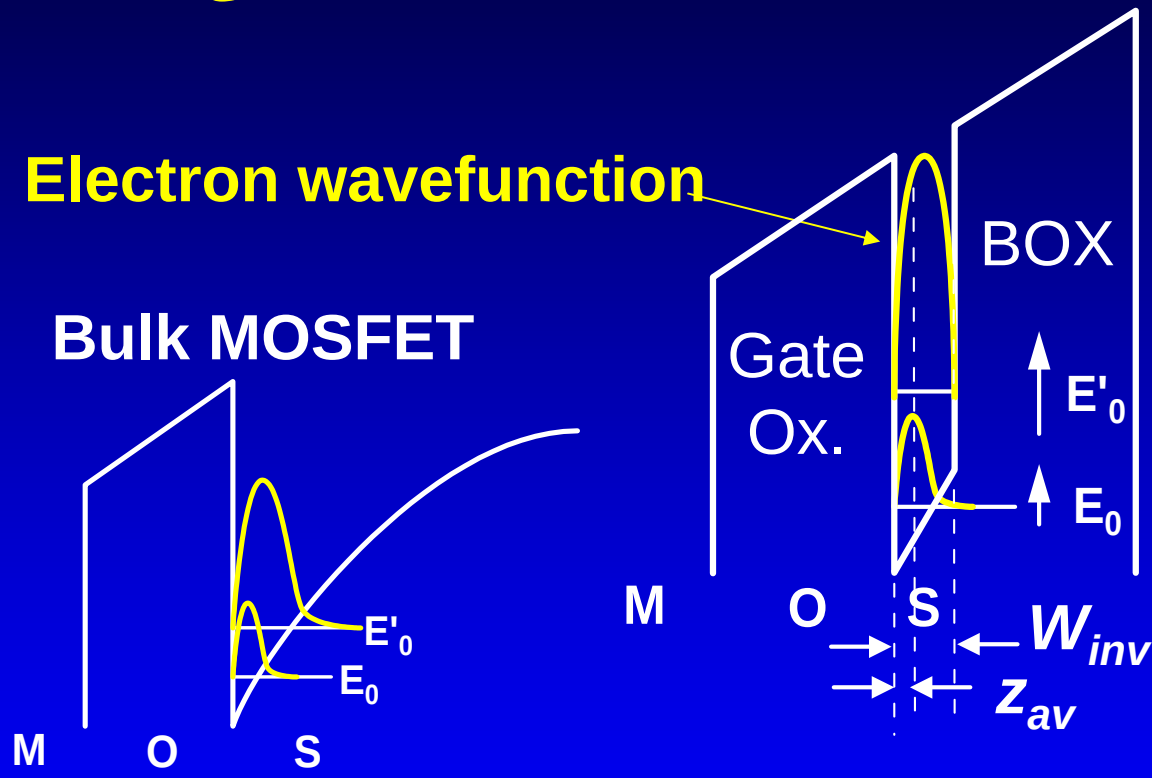
Mobility Degradation in Ultrathin-body SOI MOSFETs



J.-H. Choi, EDL **16** (1995) 527.

Mobility degradation have been observed in SOI MOSFETs with T_{SOI} of less than ~20nm.

Increase of Phonon Scattering due to Quantum-Confinement Effects



W_{inv}: thickness of inversion layer

Electron mobility decreases in thinner T_{SOI}.

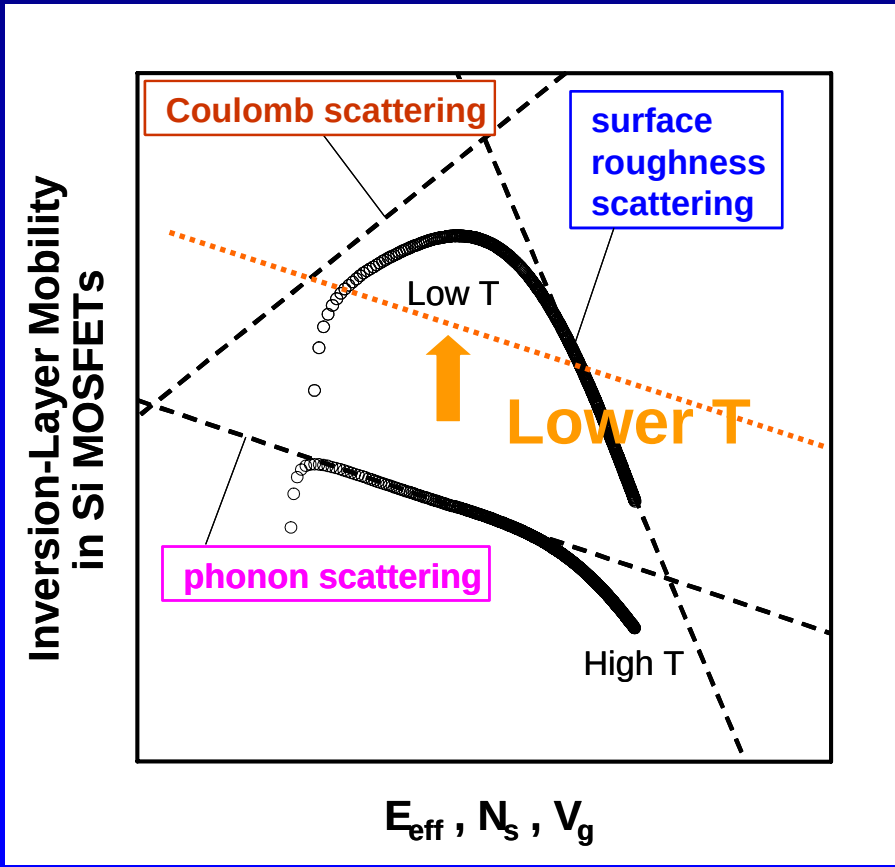
$\mu_{ac} \propto |W_{inv}|$ $\quad$ μ_{ac}: acoustic phonon-limited mobility

T_{SOI}

S. Takagi, IEDM97, p219.

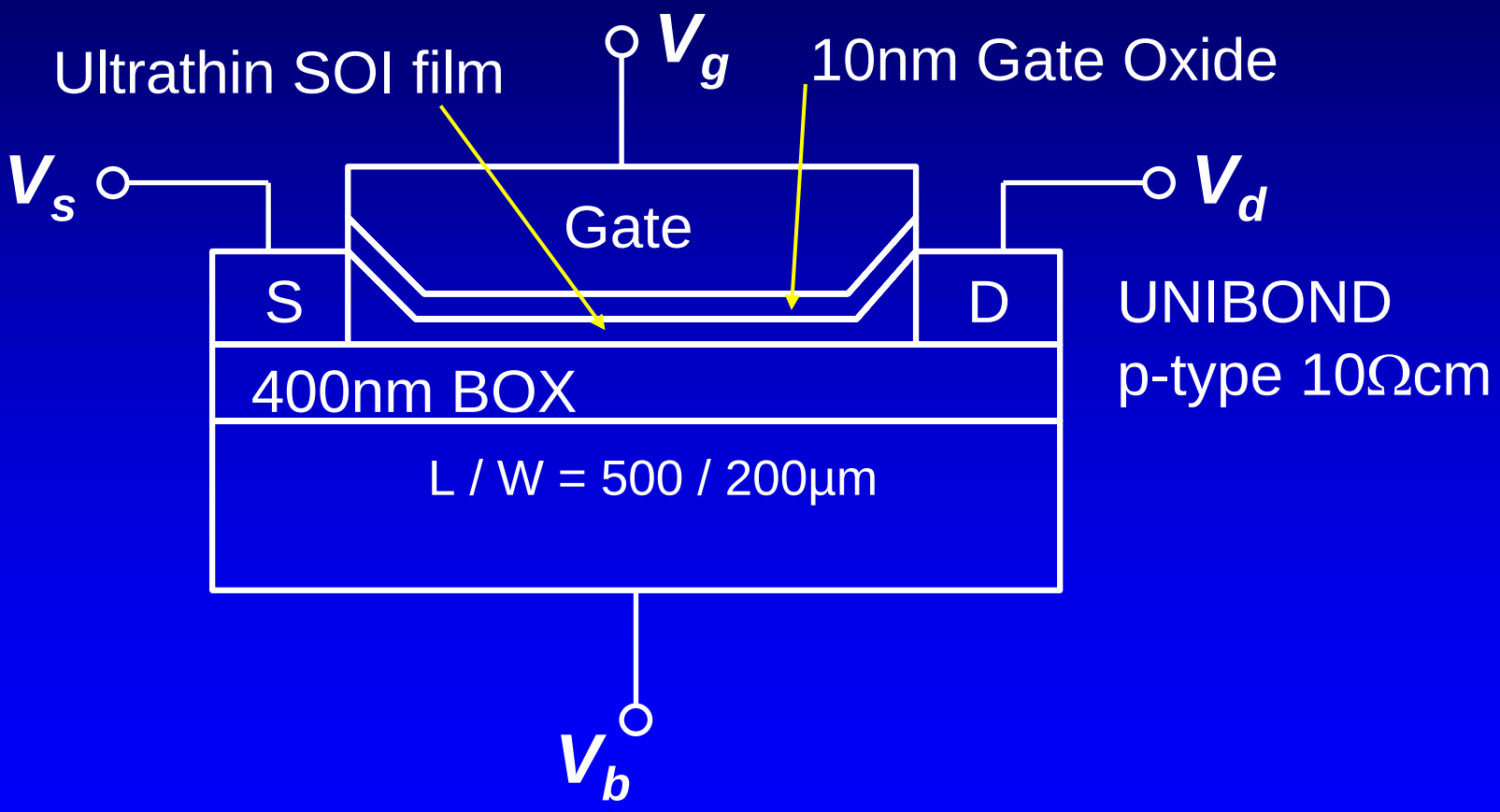
Hypothesis: Mobility degradation is due to phonon scattering increase.

Verification: Low temperature measurement of mobility

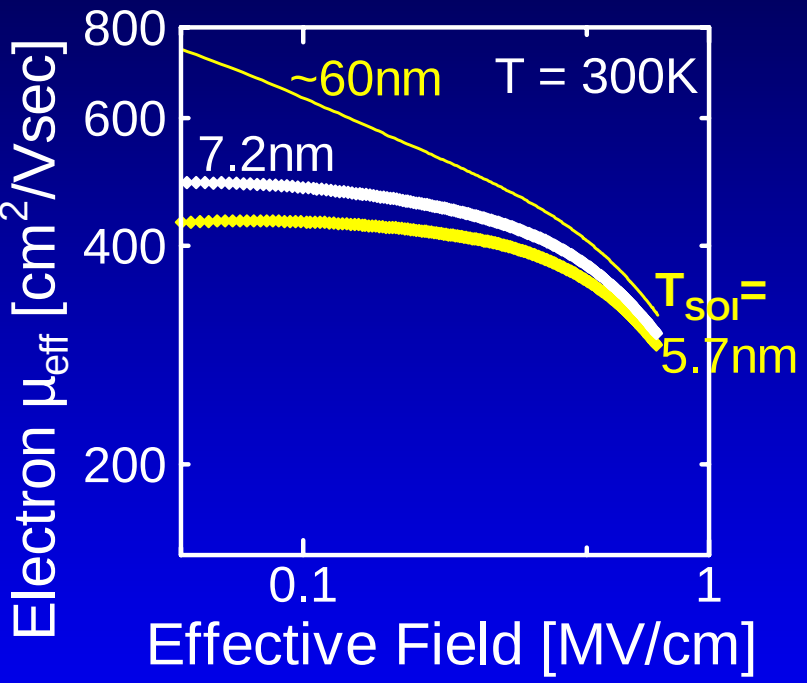


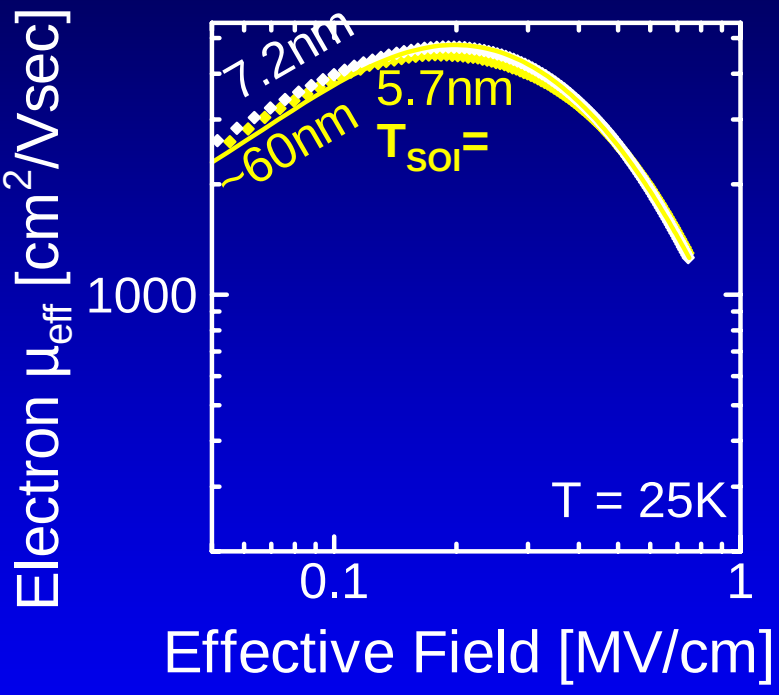
S. Takagi

Device Structure



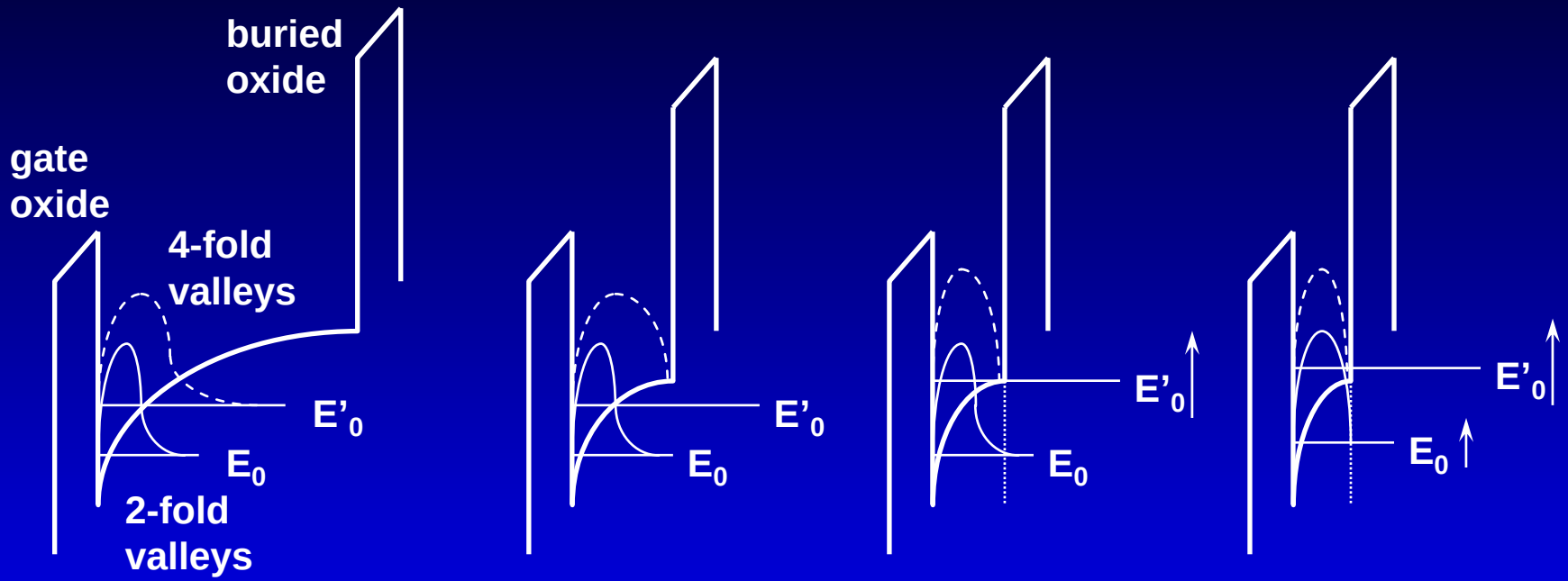
Temperature Dependence





Mobility reduction in UTB MOSFETs with T_{SOI} of greater than 5nm is due to the increase of phonon scattering.

Mobility Increase with a decrease in T_{SOI}



T_{SOI} > 20 nm

20 nm > T_{SOI} > 5 nm
- decrease of μ in 4-fold valleys

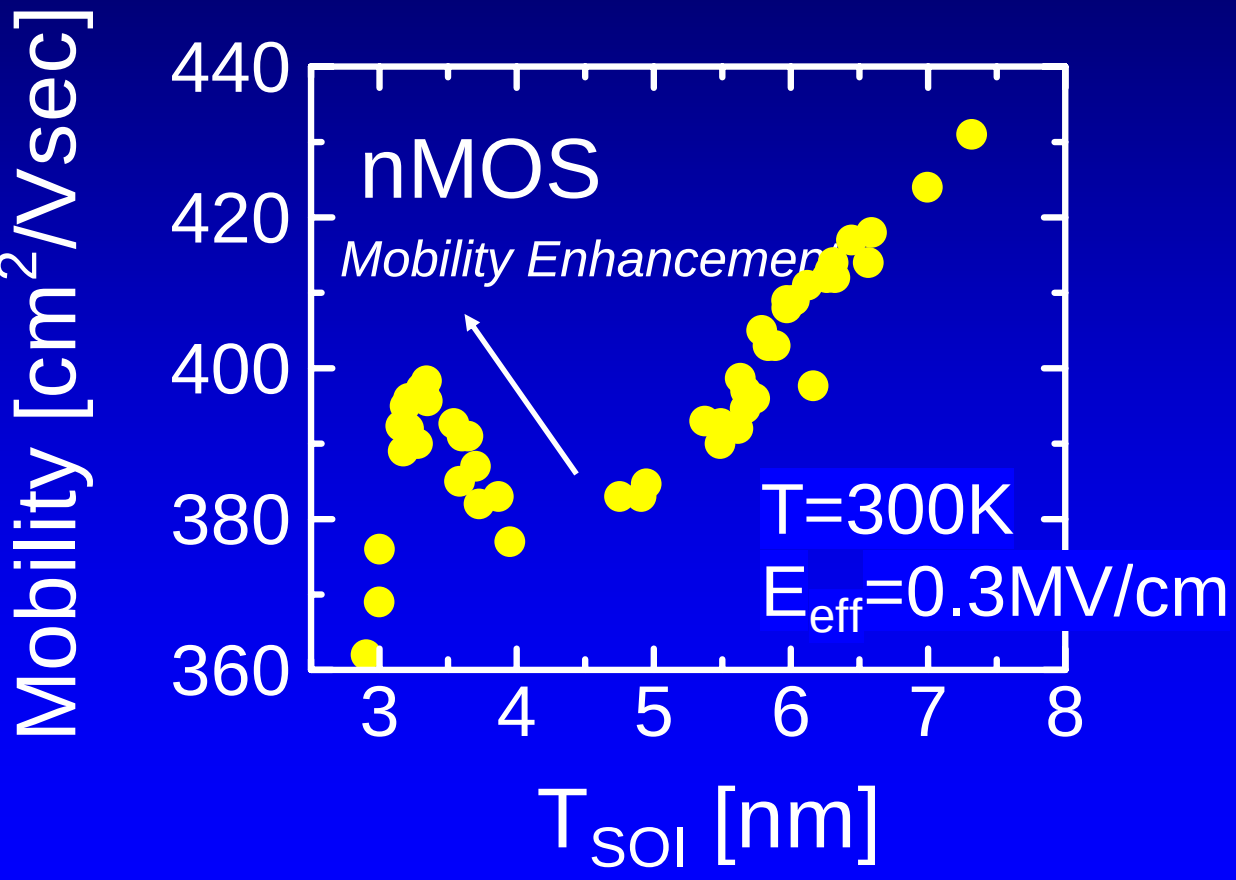
5 nm > T_{SOI} > 3 nm
- increase of μ and occupancy in 2-fold valleys

3 nm > T_{SOI}
- decrease of μ in 2-fold valleys

S. Takagi

Mobility Increase is expected in T_{SOI} range from 3 to 5nm.

Electron Mobility as a function of T_{SOI}

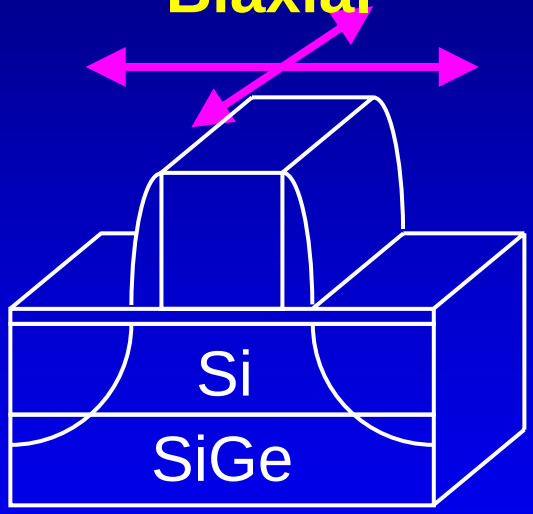


Background

- Uniaxial versus Biaxial -

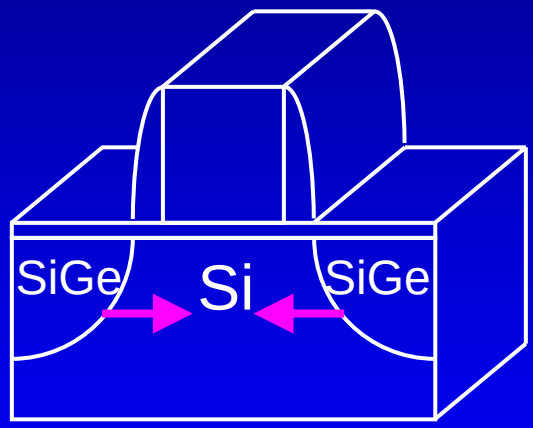
Biaxial / Uniaxial stress engineering is promising as a drain current booster in the present and future FETs.

Biaxial

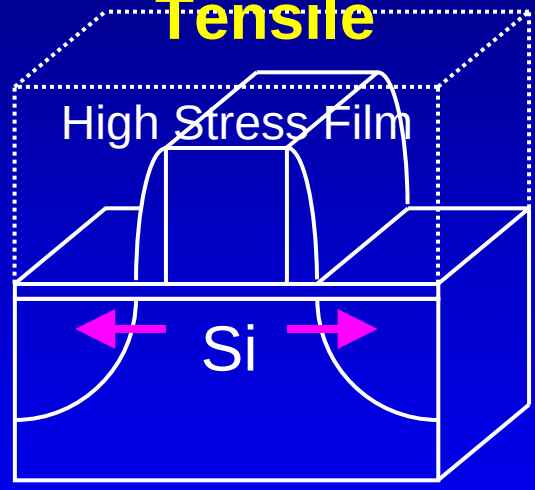


J.J.Welser, IEDM 1992, p1000.

Uniaxial Compressive



Uniaxial Tensile



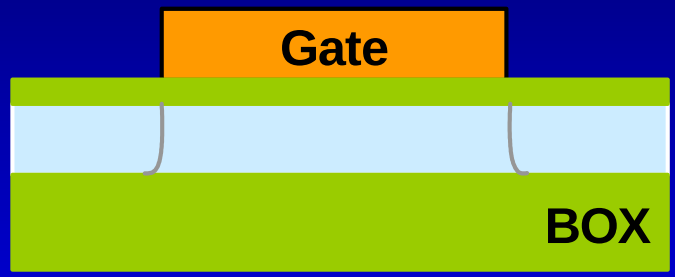
T.Ghani, IEDM 2003, p978.

- The advantages of biaxial (uniaxial) stress engineering over uniaxial (biaxial) stress engineering are not clear.
- The effect of uniaxial stress on mobility is not clear.

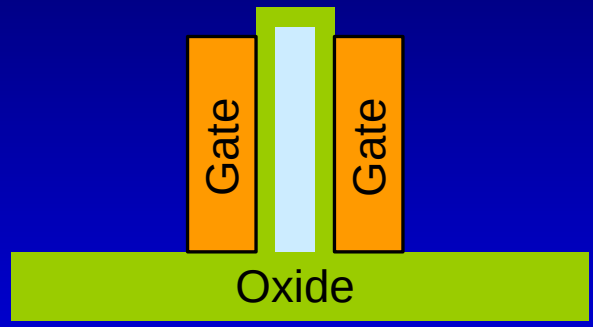
Background (Cont'd)

- UTB Structure -

MOSFETs utilizing ultrathin Si layers are promising as a 20nm-regime device structure.



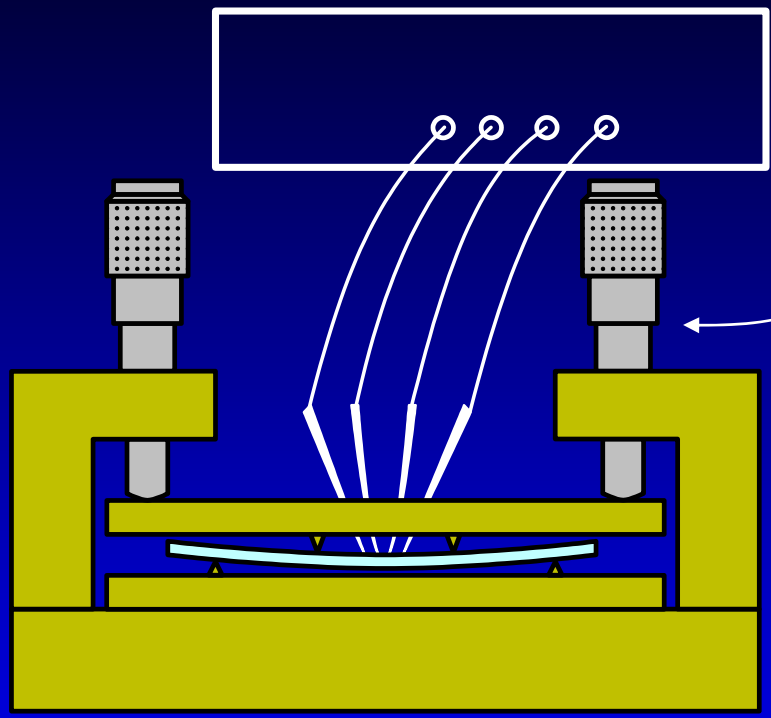
Ultrathin-body (UTB) FET

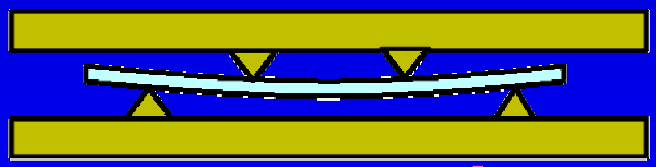


FinFET

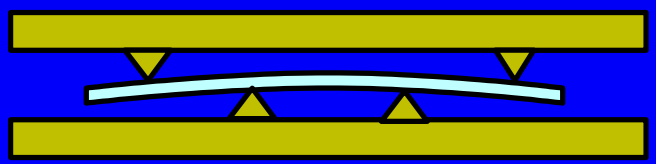
The effectiveness of biaxial/uniaxial stress engineering in Si films of less than 5nm has not been clarified yet.

Bending Apparatus



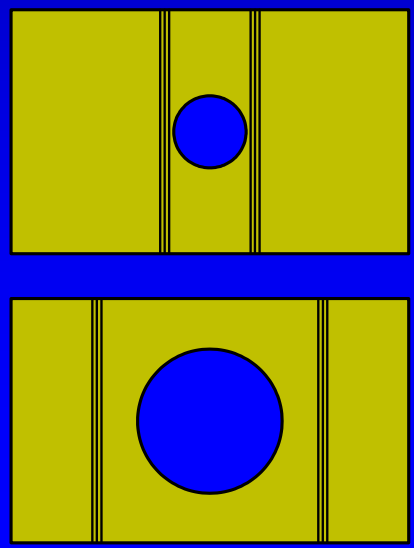


compressive

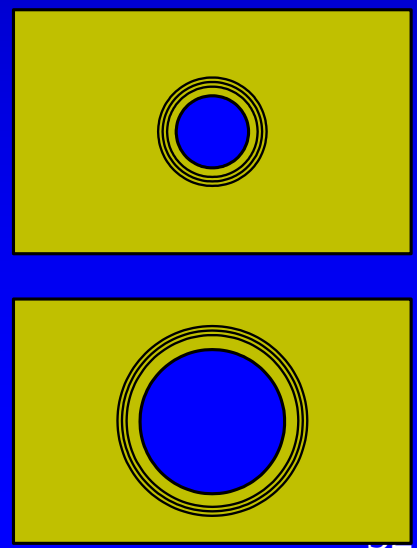


tensile

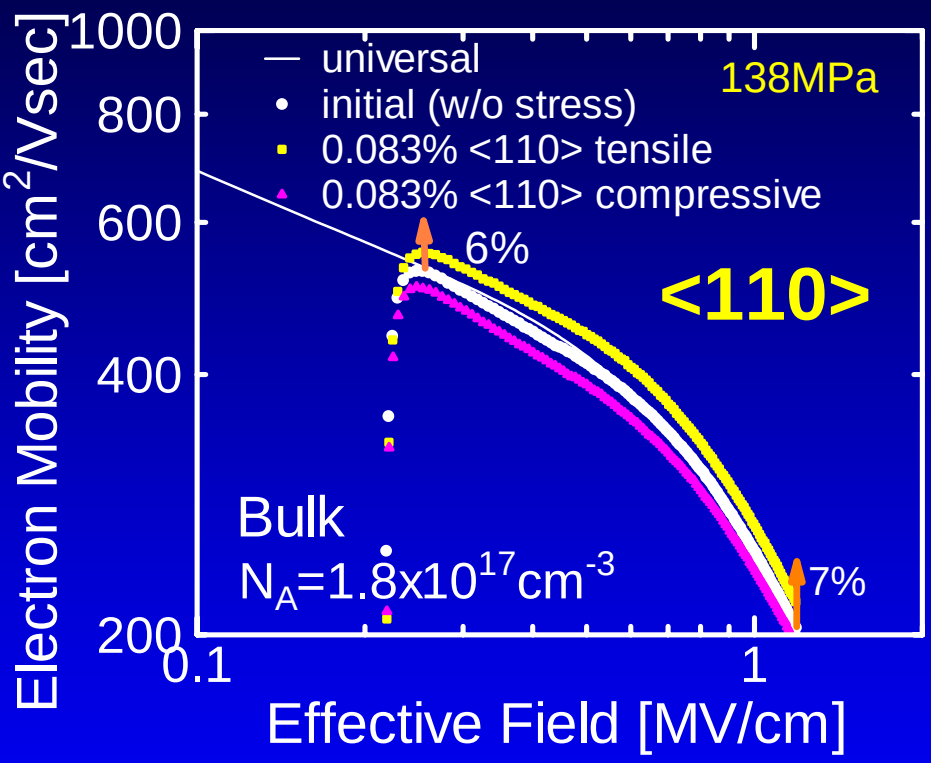
Uniaxial

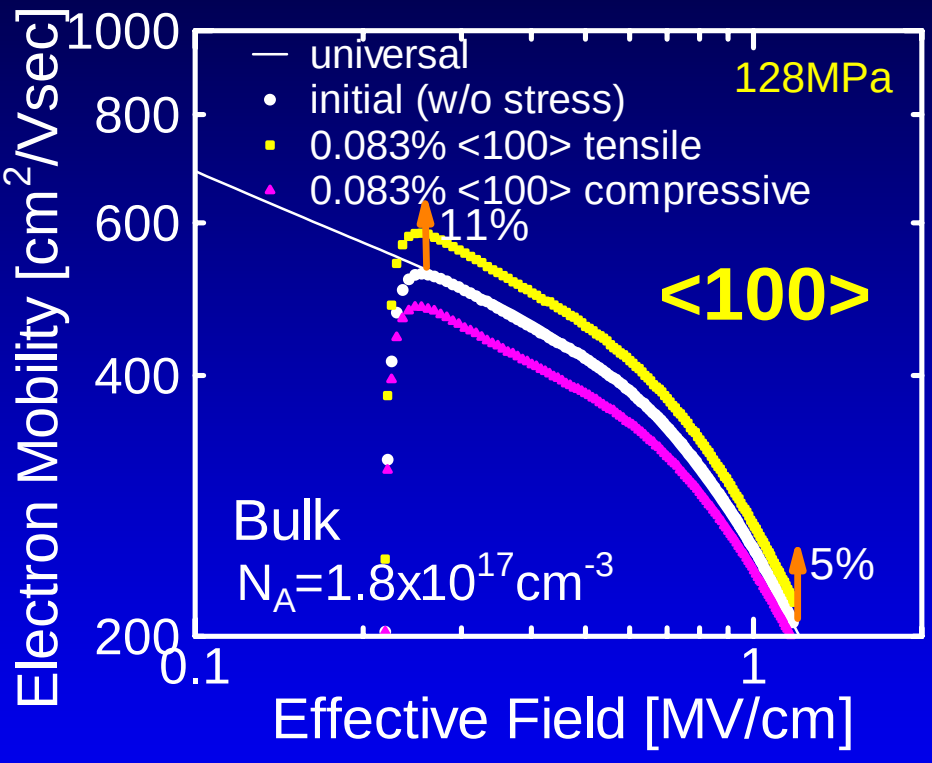


Biaxial



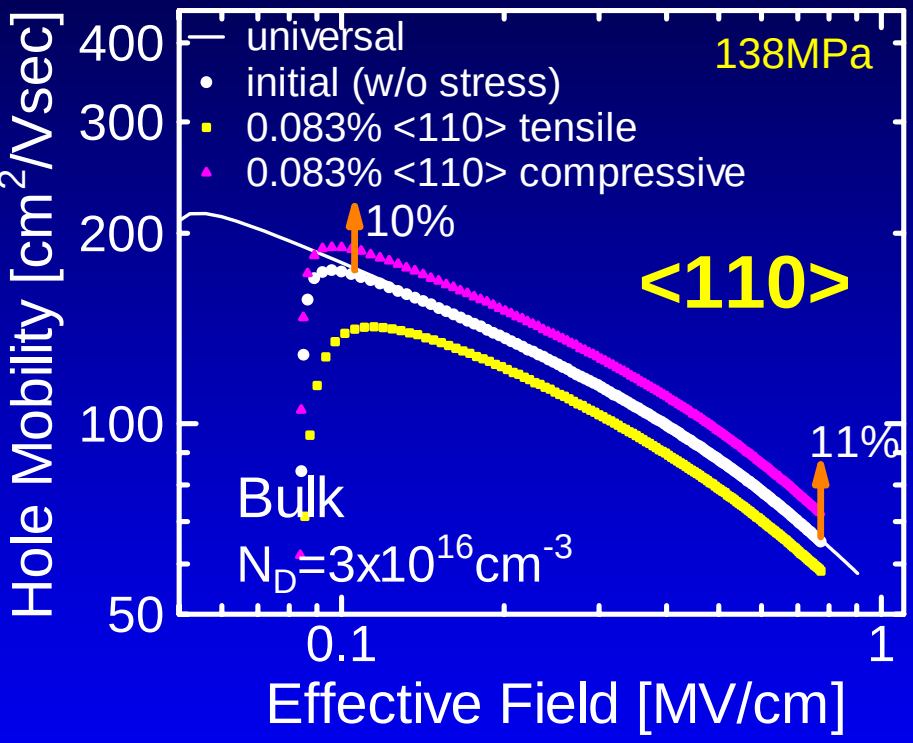
Electron Mobility

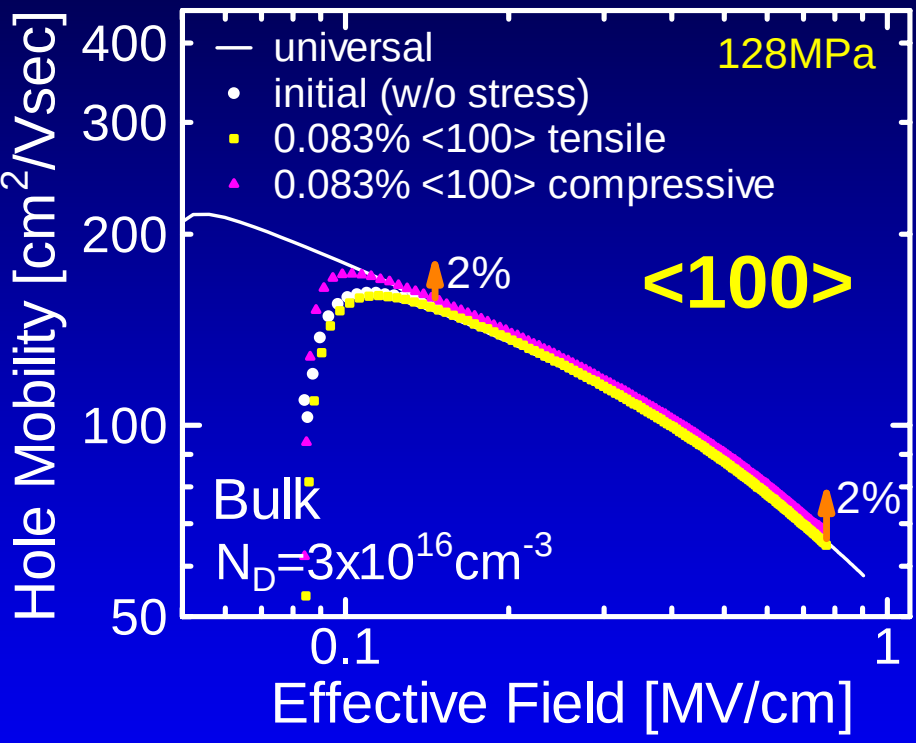




Electron mobility enhancement is greater in <100> case than in <110> case.

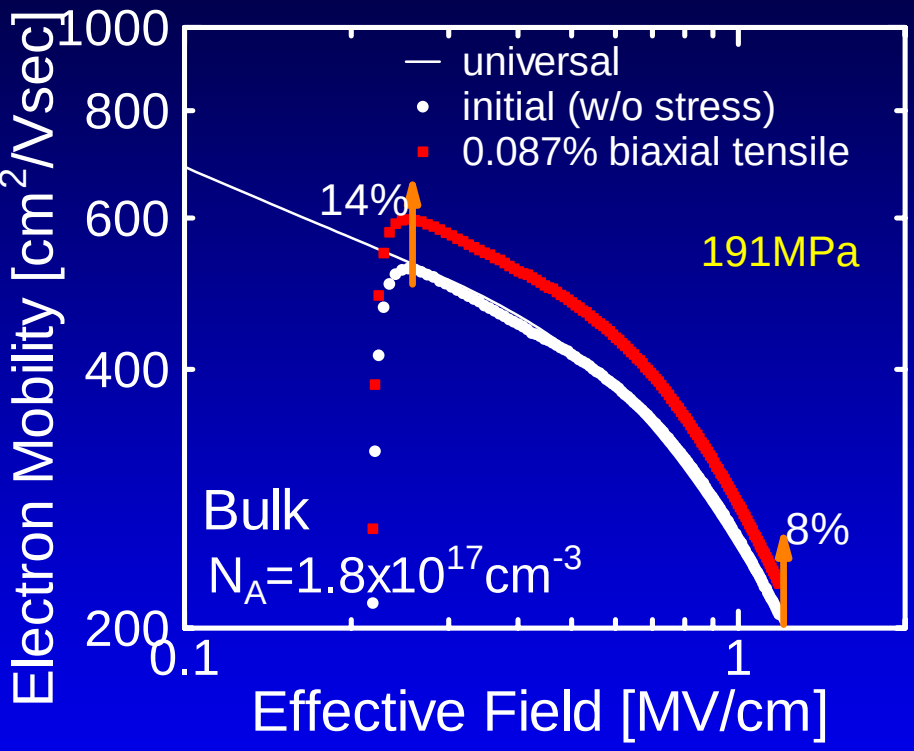
Hole Mobility

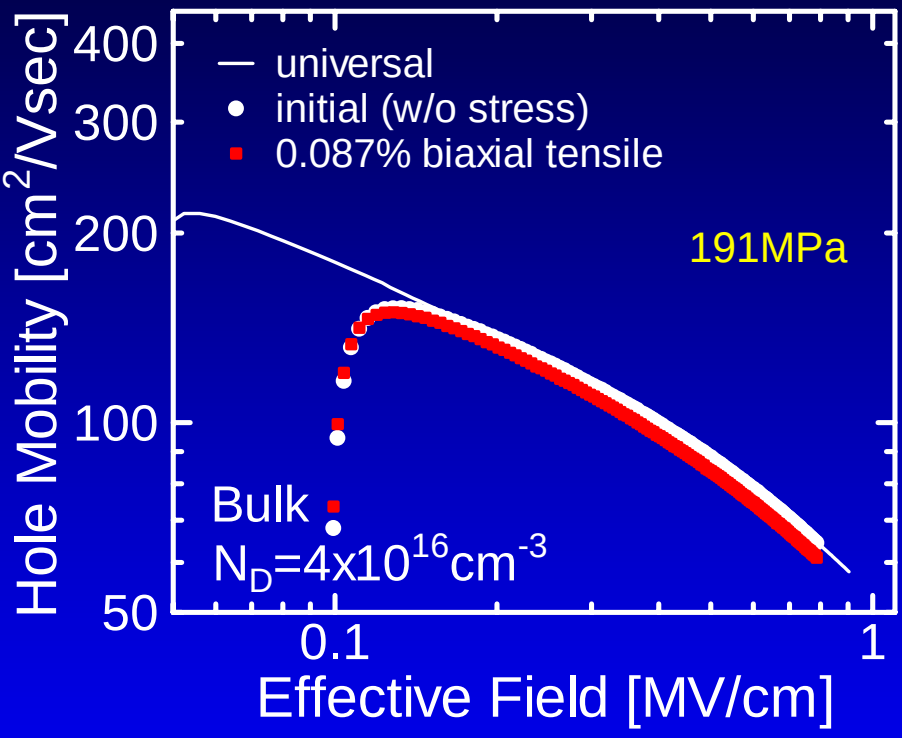




The hole mobility enhancement is much greater in <110> case than in <100> case.

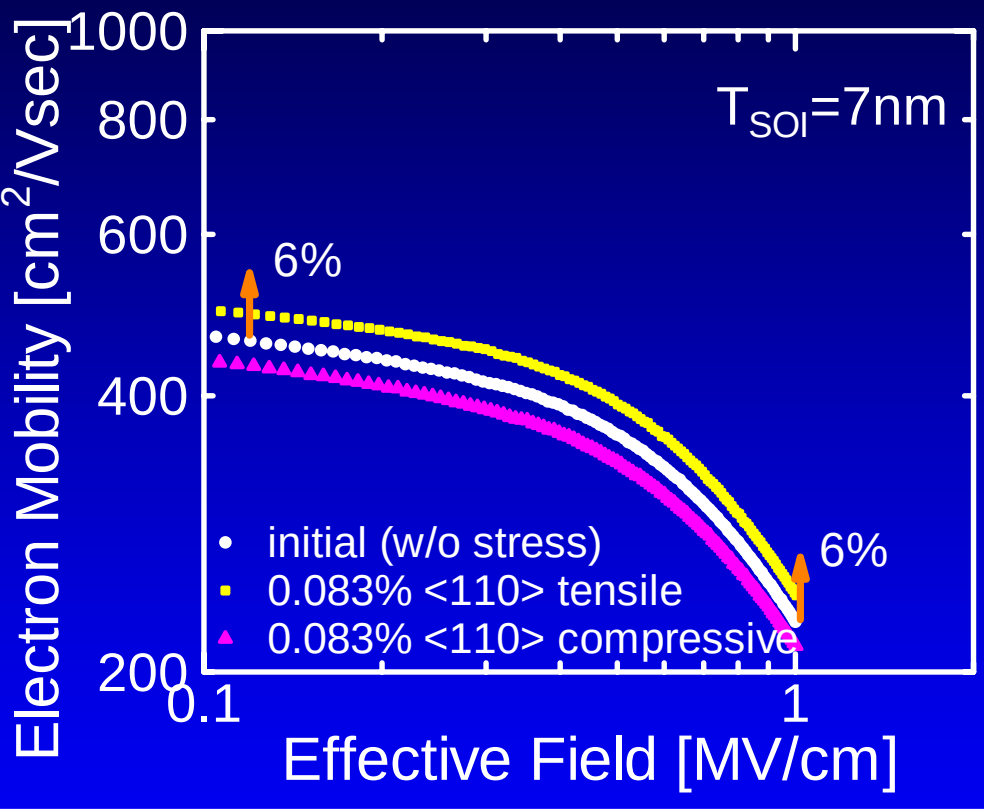
Biaxial Tensile Stress





The enhancement of electron mobility is better than that of <110> and <100> uniaxial tensile strained FETs under almost the same amount of strain. However, hole mobility enhancement cannot be observed due to the small amount of strain induced by bending.

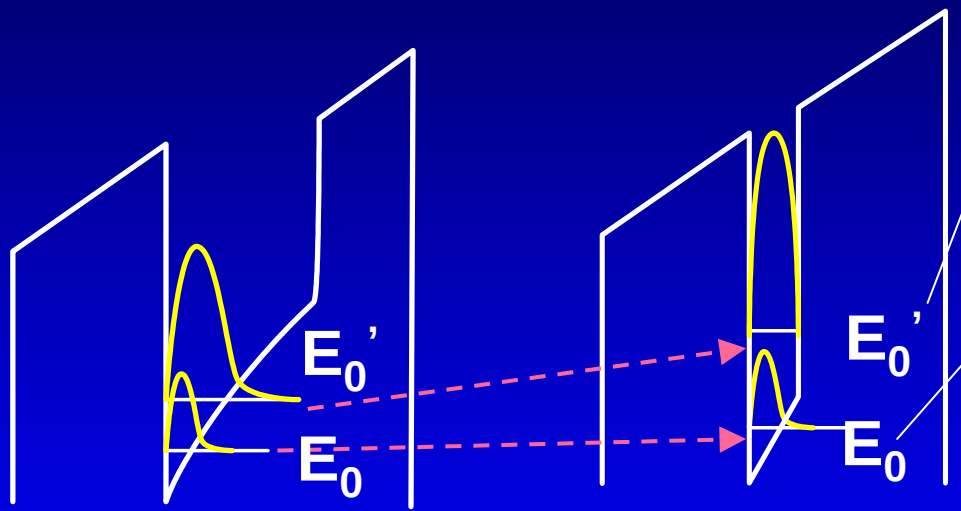
Effectiveness of Uniaxial Stress Engineering



It is demonstrated, for the first time, that uniaxial strain engineering is effective even in UTB MOSFETs with T_{SOI} of less than 10nm. The enhancement ratio is almost the same as that of bulk FETs.

Uniaxial Stress Engineering in 3.5-nm UTB MOSFETs

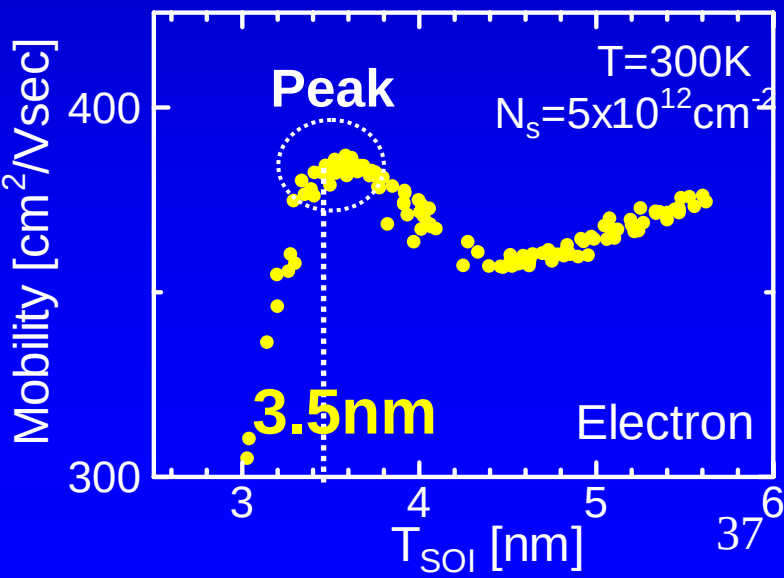
- Cooperation with Subband Structure Engineering in UTB FETs -



Subband Structure Engineering

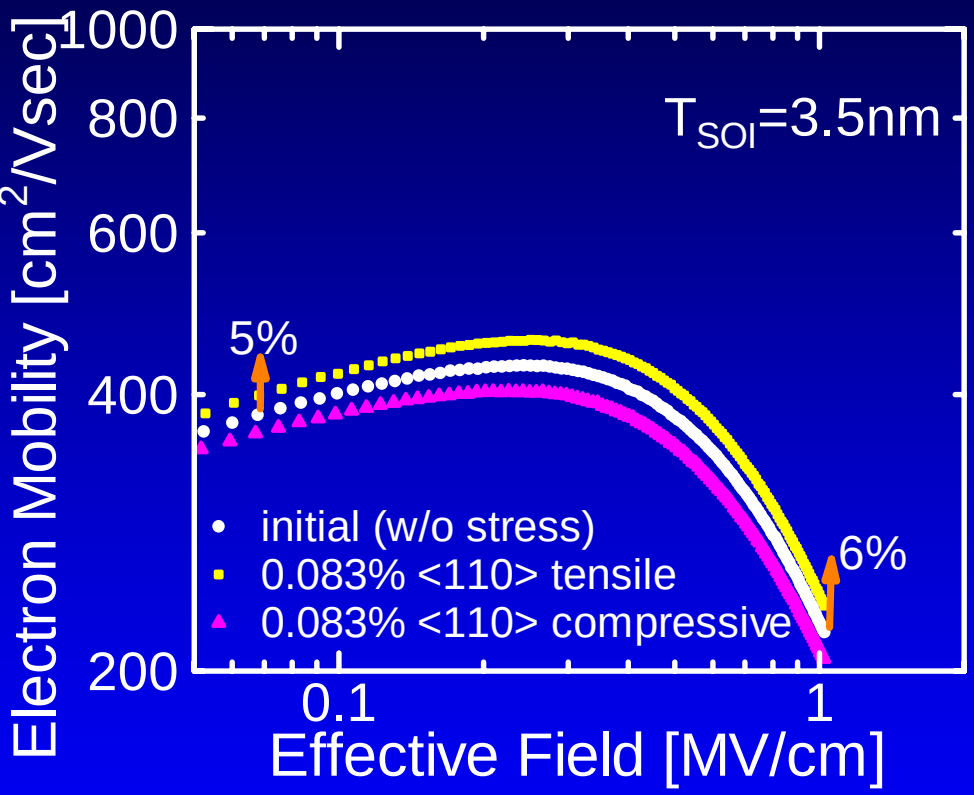
4-fold valley
- Heavier conductivity mass
- Lower mobility

2-fold valley
- Lighter conductivity mass
- Higher mobility



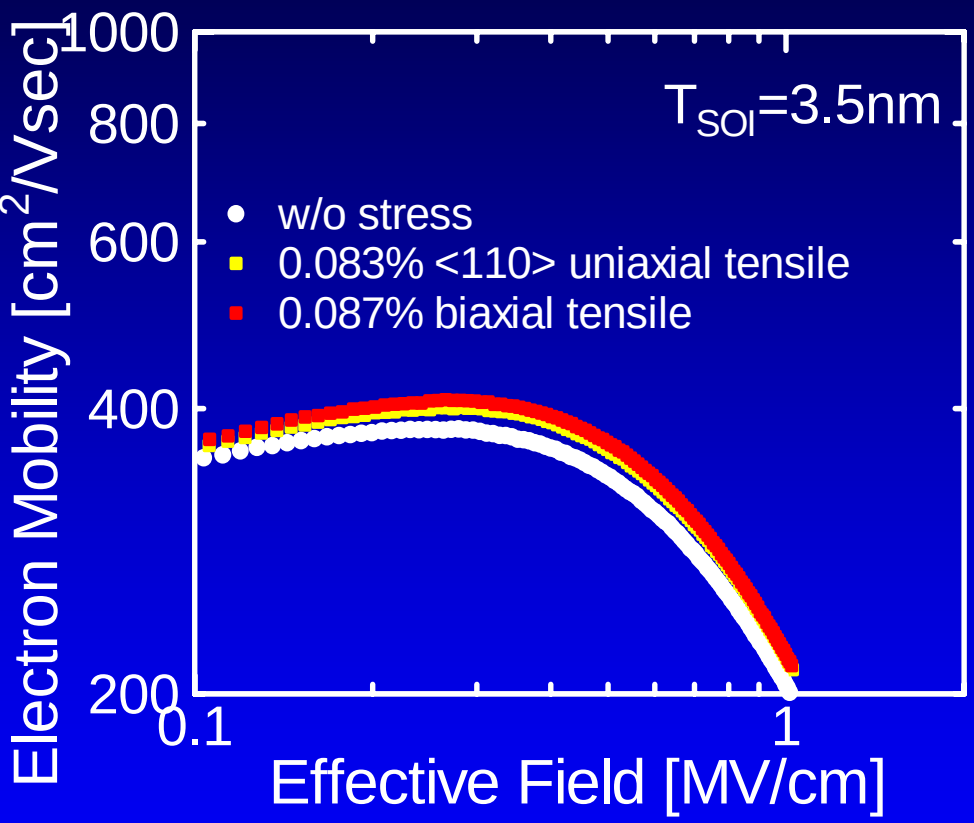
Subband Structure Engineering
+
Stress Engineering

Uniaxial Stress Effects in 3.5-nm UTB nMOSFETs



It is demonstrated that uniaxial strain engineering is still effective in UTB MOSFETs with T_{SOI} of less than 5nm, and can be used with subband structure engineering by TSOI optimization at the same time to enhance mobility.

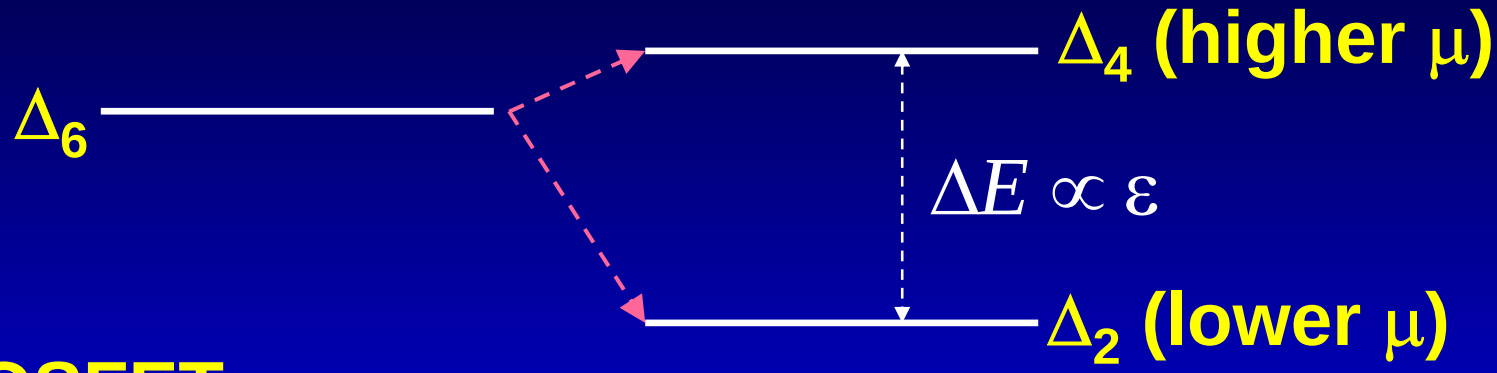
Uniaxial versus Biaxial in 3.5-nm UTB nMOSFETs



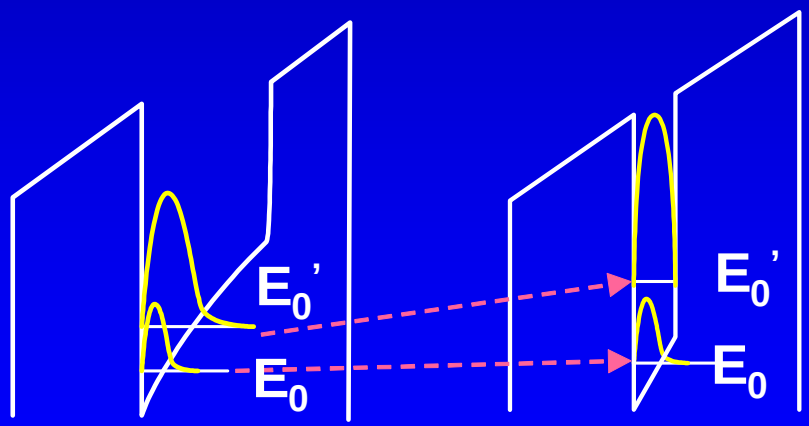
It is demonstrated that the advantage of biaxial tensile strain over uniaxial tensile strain in terms of electron mobility becomes less in 3.5-nm UTB FETs.

Why Mobility Enhance?

Conventional Model: split of 2-fold and 4-fold valley

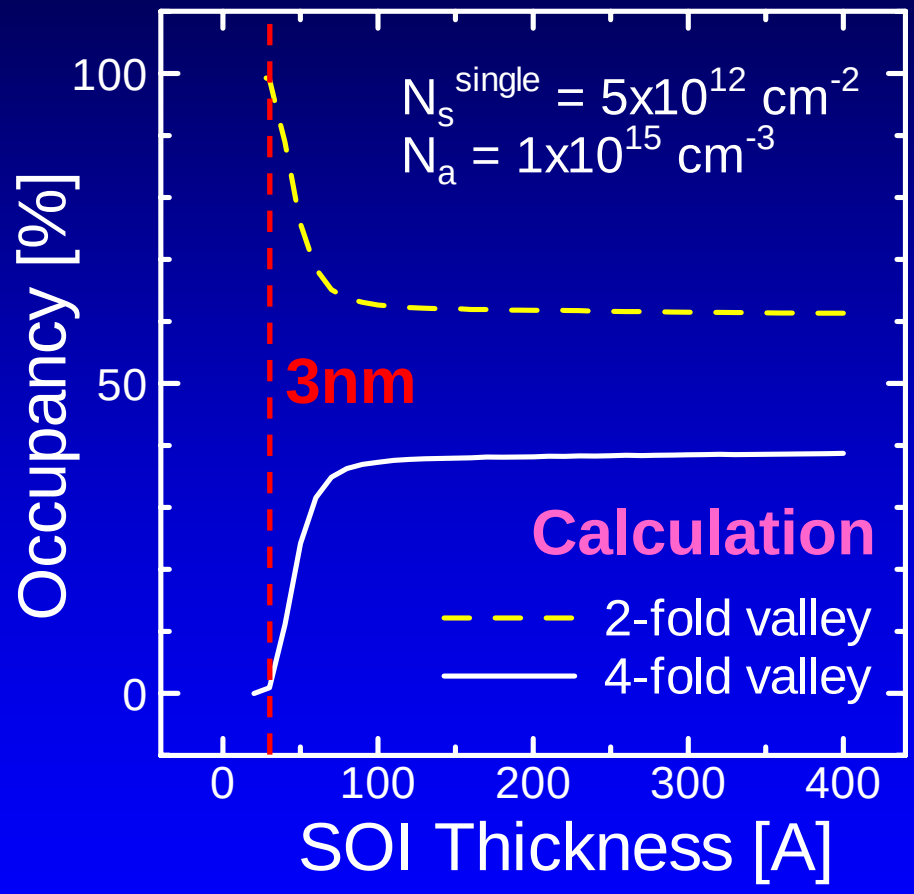


In UTB MOSFETs,
the split of 2-fold and 4-fold valley already takes place.



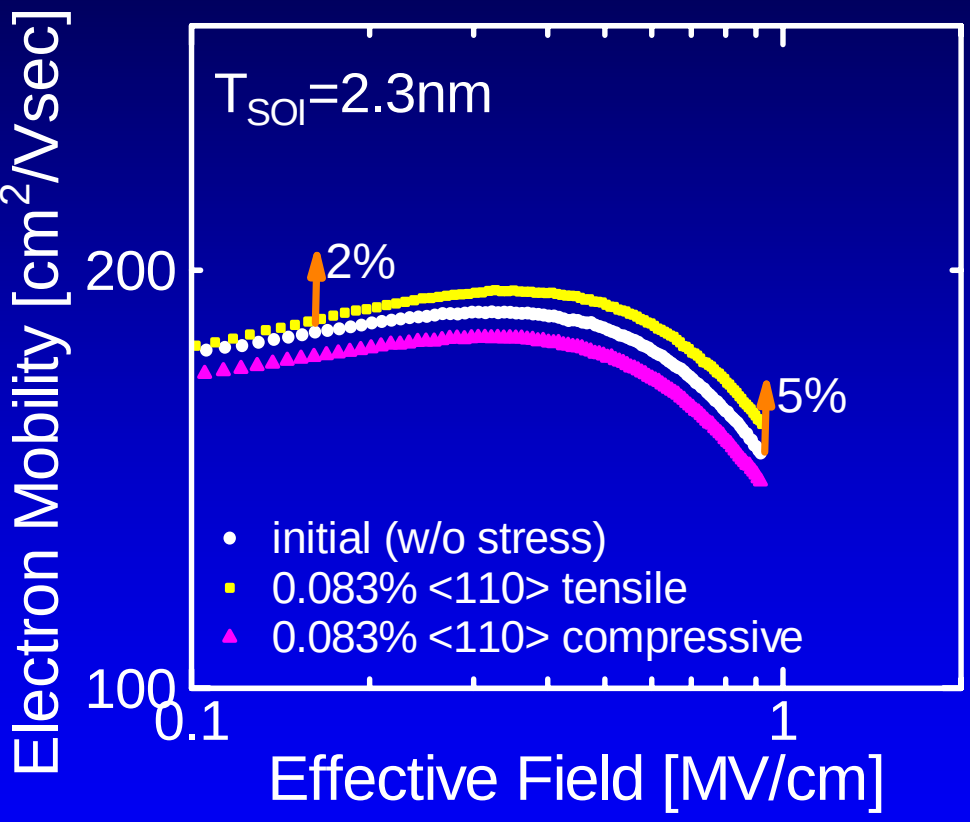
The mobility enhancement in UTB MOSFETs cannot be simply explained by the conventional model.

Occupancy of Electrons in 2-fold and 4-fold Valleys of UTB FETs



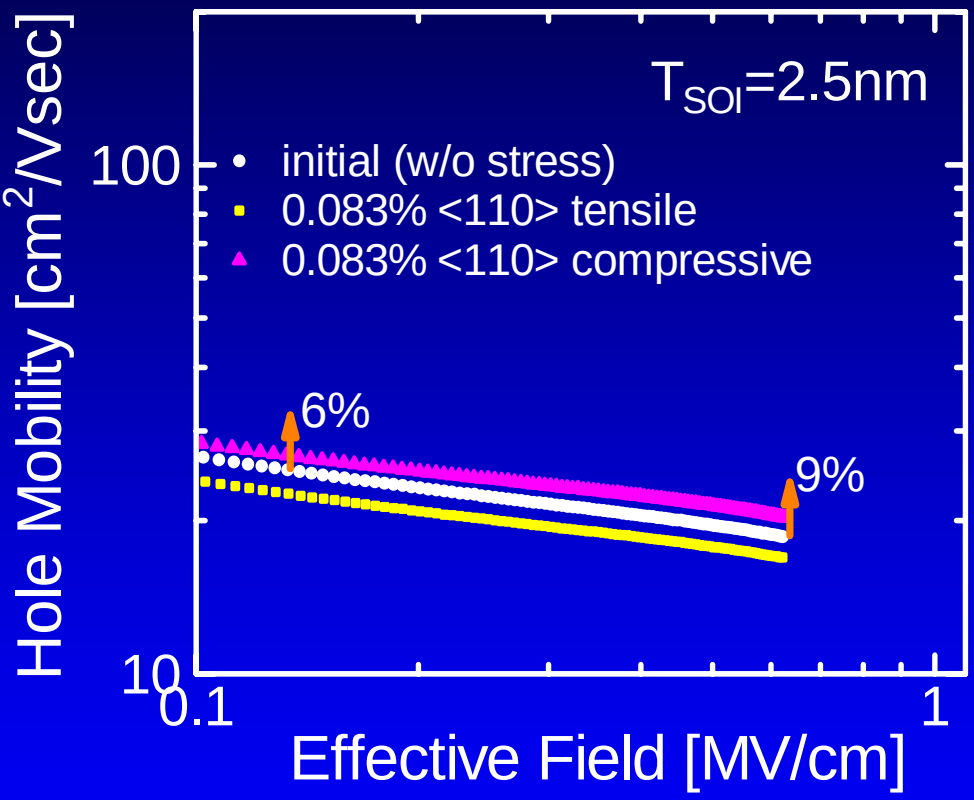
The occupancy of 2-fold valley becomes almost 100% if SOI thickness is less than 3nm.

Uniaxial Stress Effects in 2.3-nm UTB nMOSFETs



The electron mobility enhancement in this device is not due to the split of 2-fold and 4-fold valleys.

Uniaxial Stress Effects in 2.5-nm UTB pMOSFETs



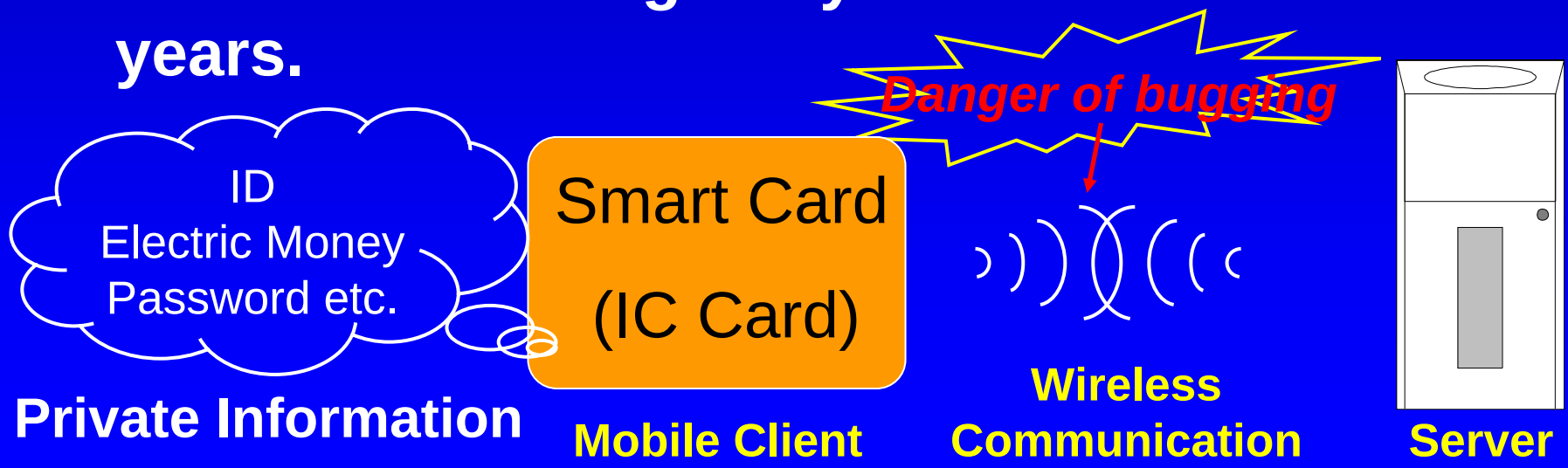
The hole mobility in UTB MOSFETs with T_{SOI} of less than 3nm is also increased by uniaxial stress engineering.

Single Electron Device for Security Applications

Introduction

In Ubiquitous Computing Era,

- **A variety of services (*ticket service*, *e-commerce* etc.) will be provided on the basis of electrical authentication with wireless ubiquitous client (*RFID*, *non-contact Smart Cards* etc.).**
- **The security requirements for the ubiquitous client have been greatly increased in recent years.**



Introduction

RNGs are essential components for electrical security systems.

- **The security of modern cryptographic technique relies on *unpredictability* and *irreproducibility* of random numbers. (eg. digital secret key)**
- **Random numbers can be used to jumble inner electrical signals of mobile clients, and thus disturb bugging or tampering by intentional hackers.**

The realization of high-quality RNGs in a small area with low power consumption is strongly required for mobile client in ubiquitous era.

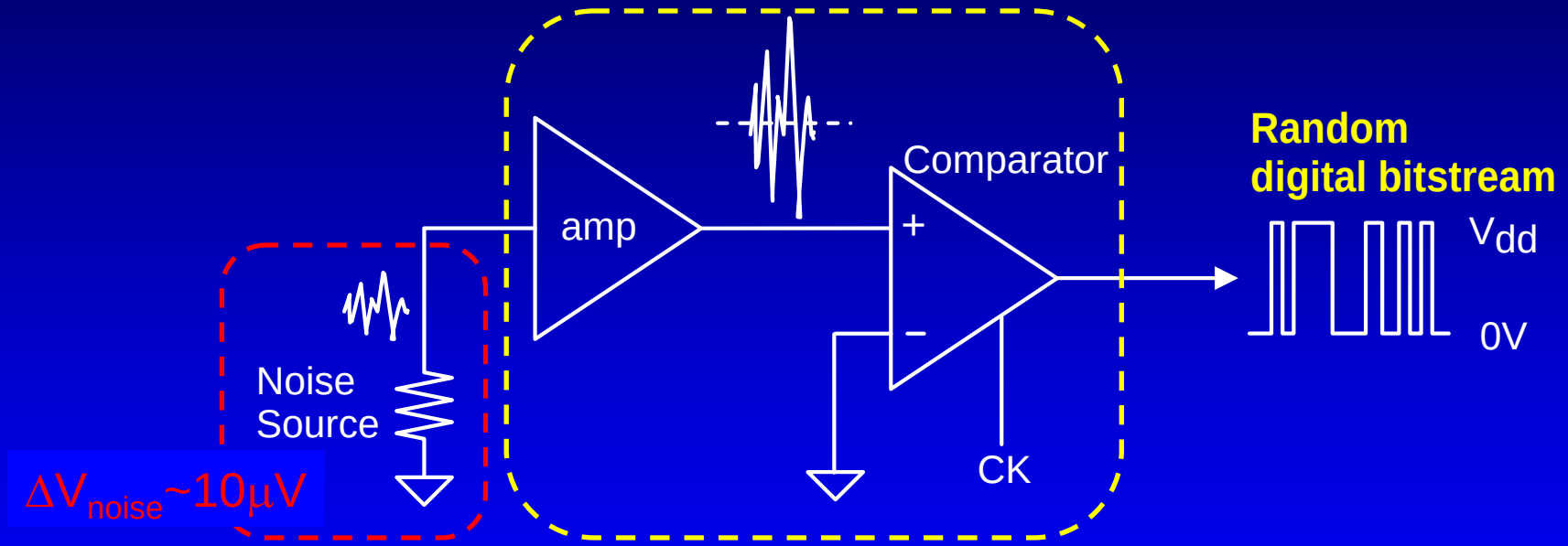
Introduction
- Class of RNGs -

- Physical RNG
- Pseudo RNG

Introduction

-Example of Physical RNG-

Electrical RNGs based on Physical Phenomena



Small Noise Signal ***Large, Power-consuming Circuit***

Present high-quality RNG is large, power-consuming circuit, and is not suitable for ubiquitous applications.

Introduction

-Pseudo RNG-

Pseudo Random Number

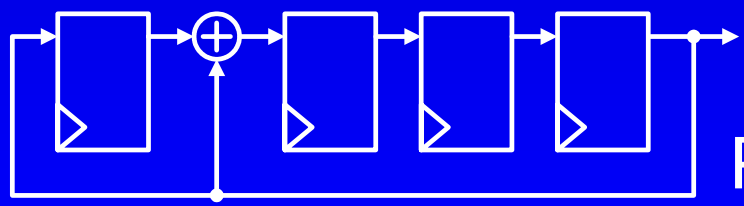
Pseudo random numbers are digital sequences that have long correlation, and can be regarded as "random numbers". They are generated by a certain algorithm, and therefore they are reproducible and predictable.

➡ ***Pseudo RNGs cannot provide high security.***

However, pseudo RNGs have small and low-power properties.

Example of pseudo RNG

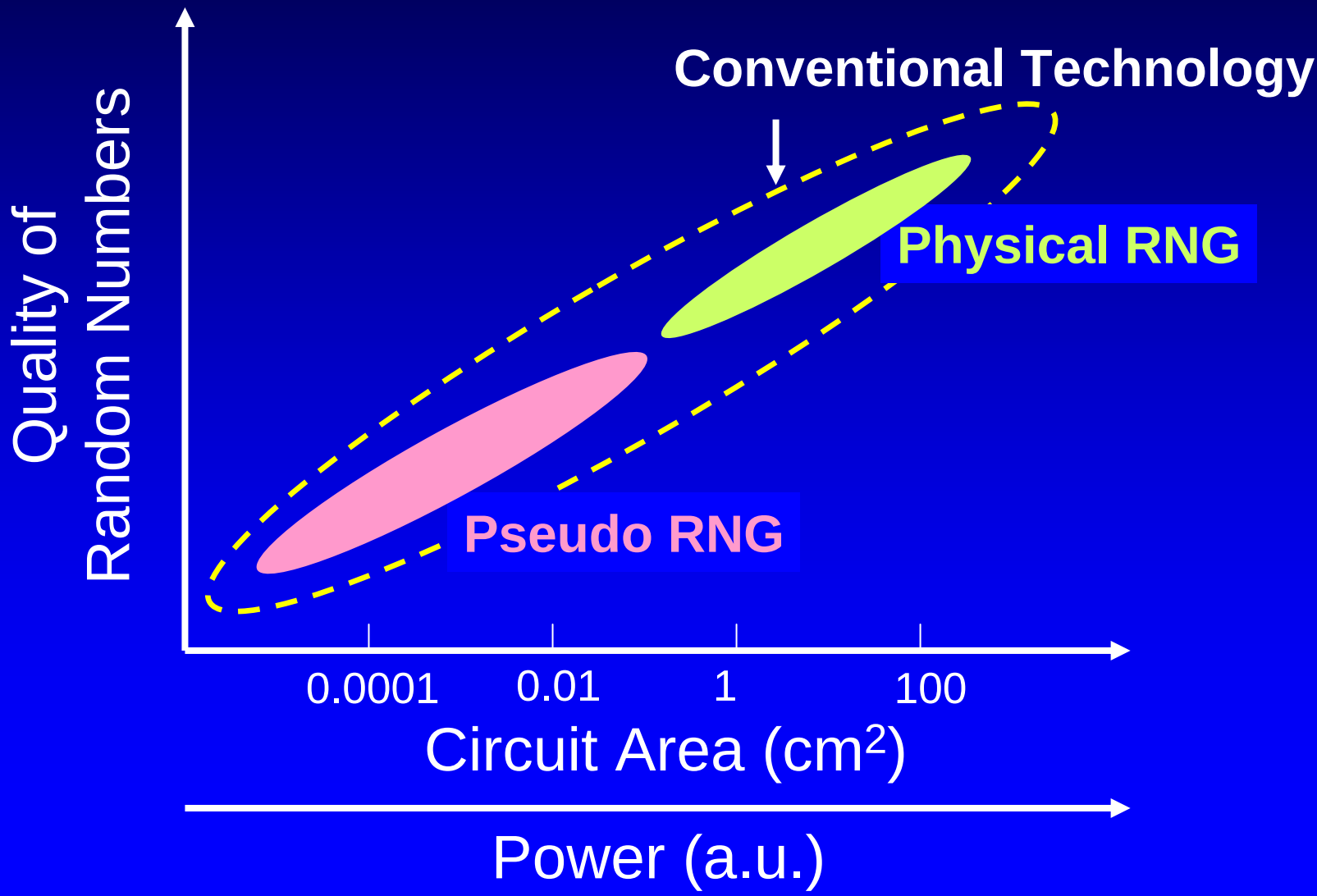
Linear Feedback Shift Resister (LFSR)



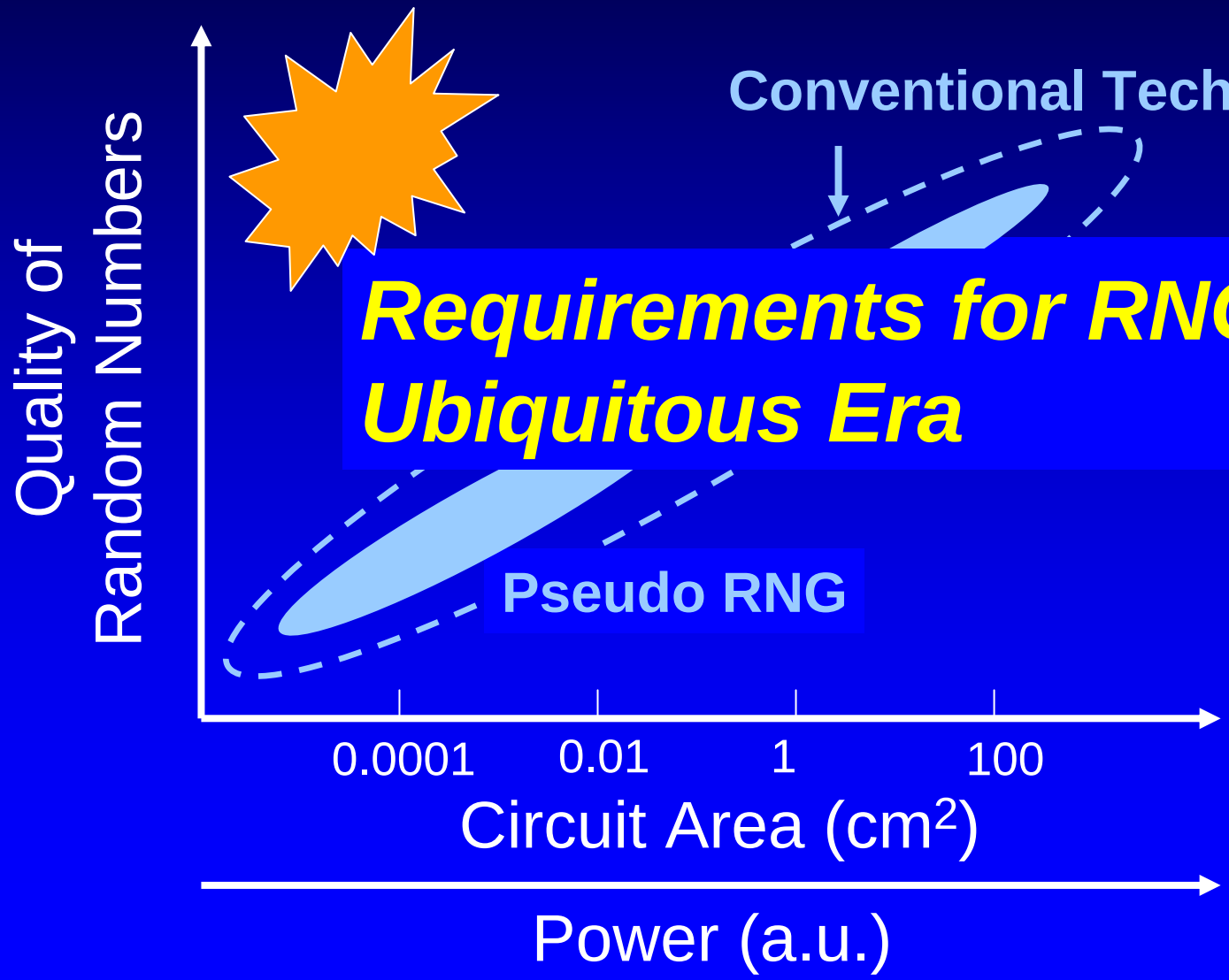
Four-bit LFSR

LFSRs are small digital circuits, but they were already hacked (see, J.A. Reed, *Cryptologia* 1 (1977) 20)!

Introduction
-Technology Map-

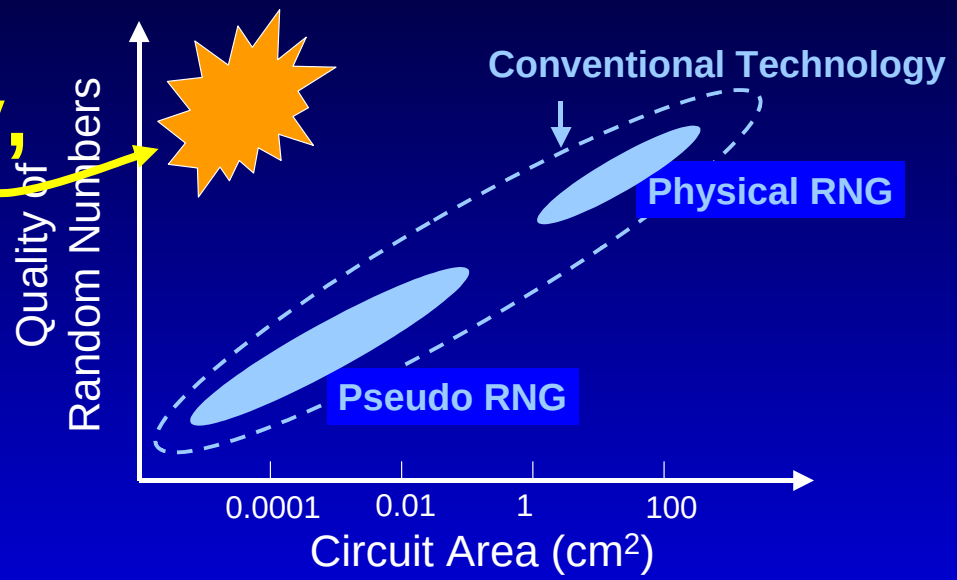


Introduction
-Technology Map-



Objective

To realize high-quality, small and low-power RNGs Suitable for Secure Ubiquitous Computing Era



In This Work,

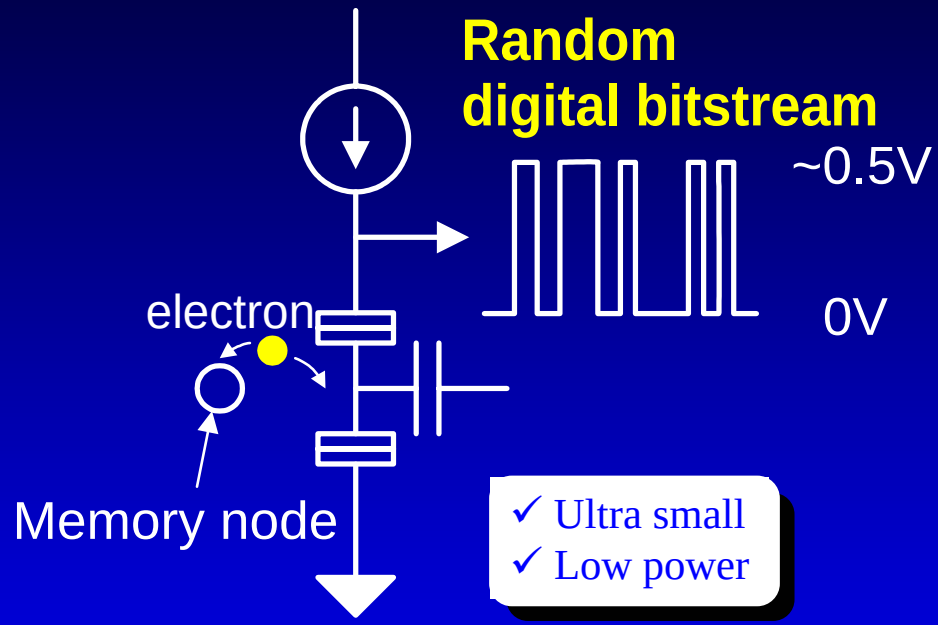
- **Propose the concept of single-electron RNG**
- **Justify whether the single-electron RNG is useful for generating high-quality random numbers in a small area with low power consumption or not.**

Concept of Single-Electron RNG

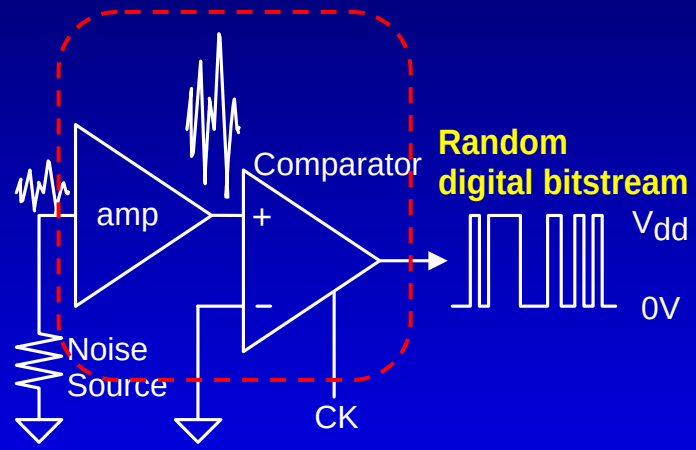
- Utilize ***stochastic*** single-electron capture/emission process to/from an electron pocket as physical seeds for random numbers.
- Detect single-electron capture/emission process with ***single-electron transistor***.

Single-Electron RNG =
SET + Single-Electron Pocket (Trap)

Advantages of Single-Electron RNG



Eliminate these large, power-consuming circuit.



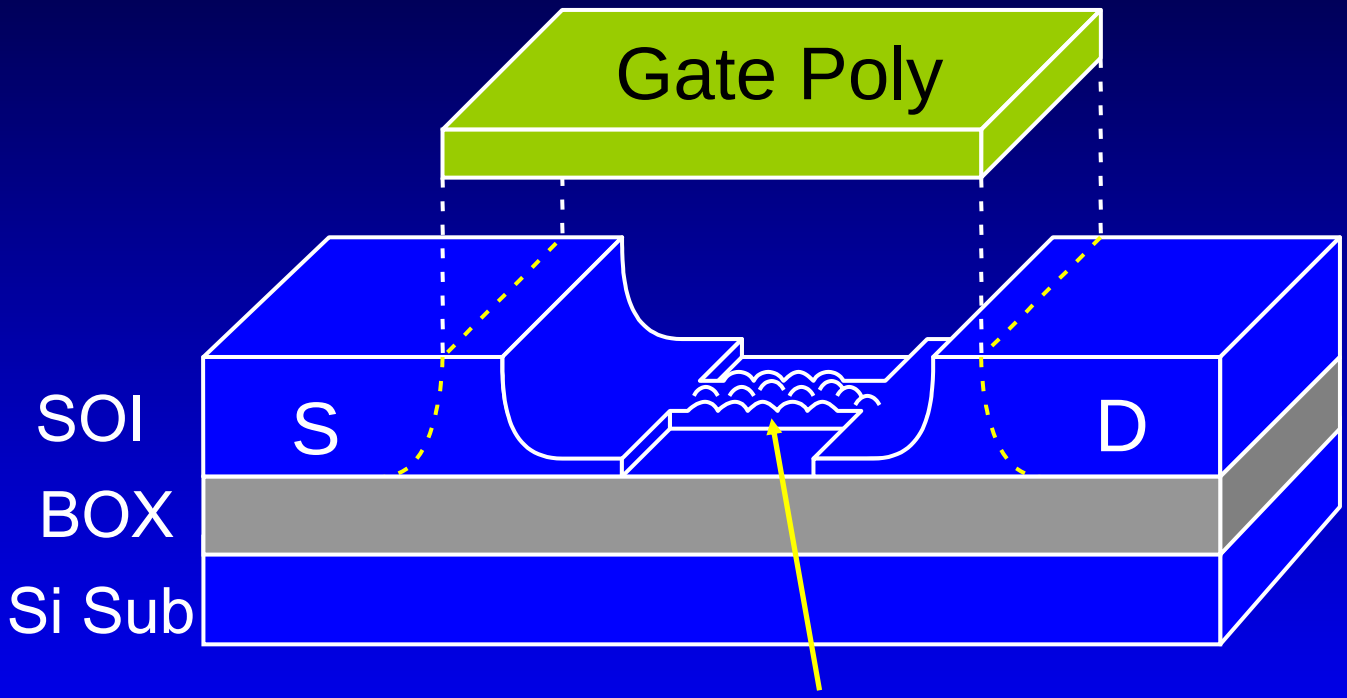
Single-electron capture/emission processes change SET current abruptly.

➡ No need for comparator

Single-electron processes are detected with SET.

➡ No need for differential amplifier

Device Structure



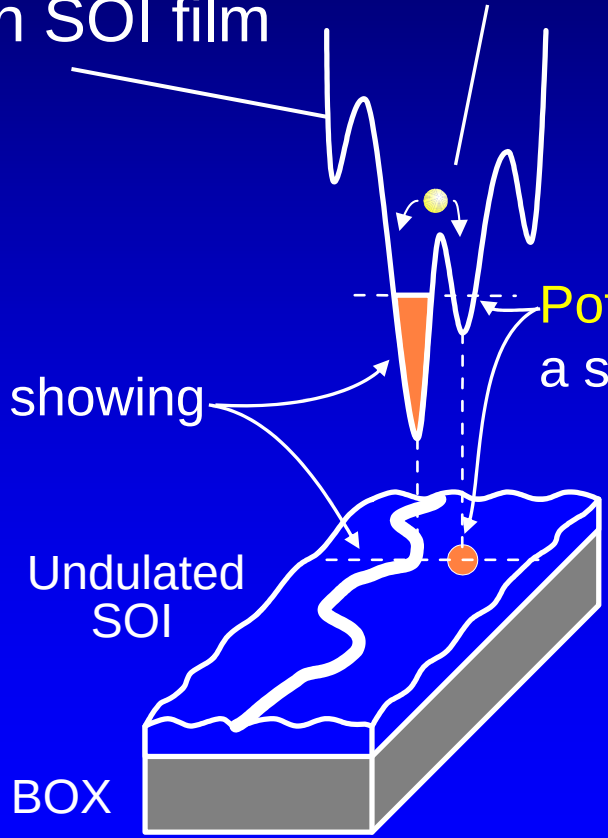
Ultrathin (< 2.5 nm) SOI film
whose surface was undulated by alkaline-based solutions.

K. Uchida et al., DRC 1999, p138.
K. Uchida et al., IEDM 2000, p863.
K. Uchida et al., J. Appl. Phys. 90 (2001) 3551.

Potential Profile

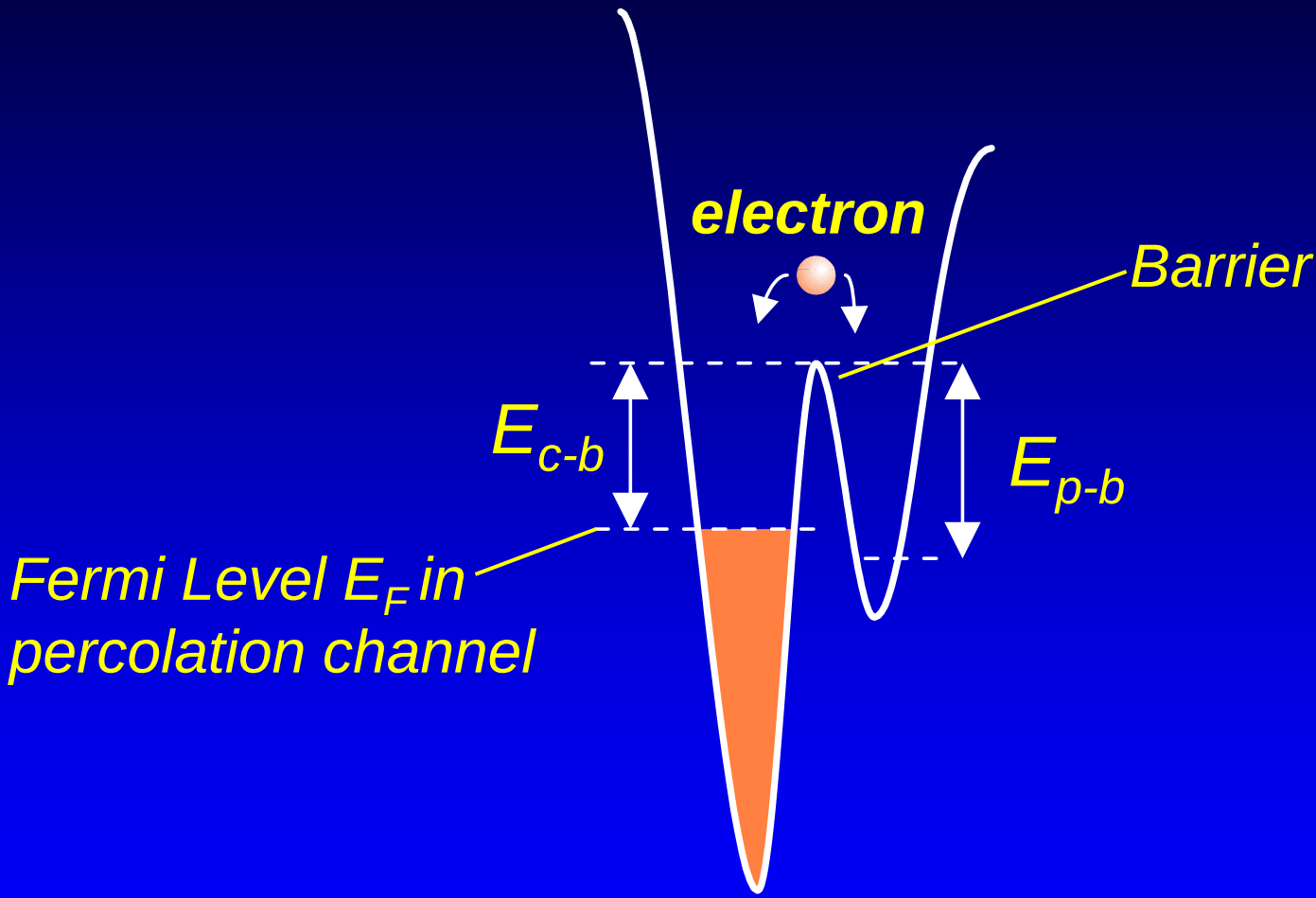
Potential Profile in undulated ultrathin SOI film

Single-electron capture/emission to/from potential pocket, due to thermal agitation



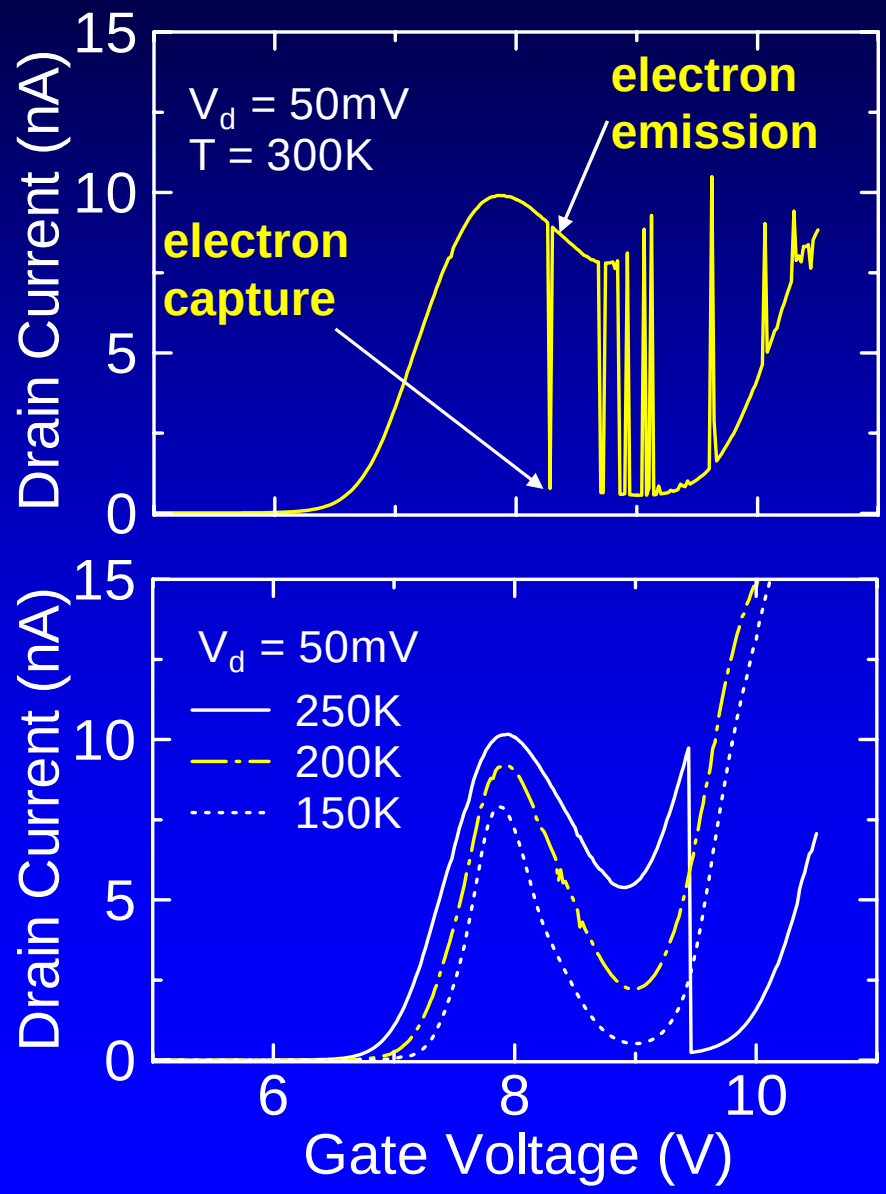
Both an SET and a potential pocket are formed in the film

Operation Principle



At the moderate gate voltage, single-electron capture/emission can be observed frequently.

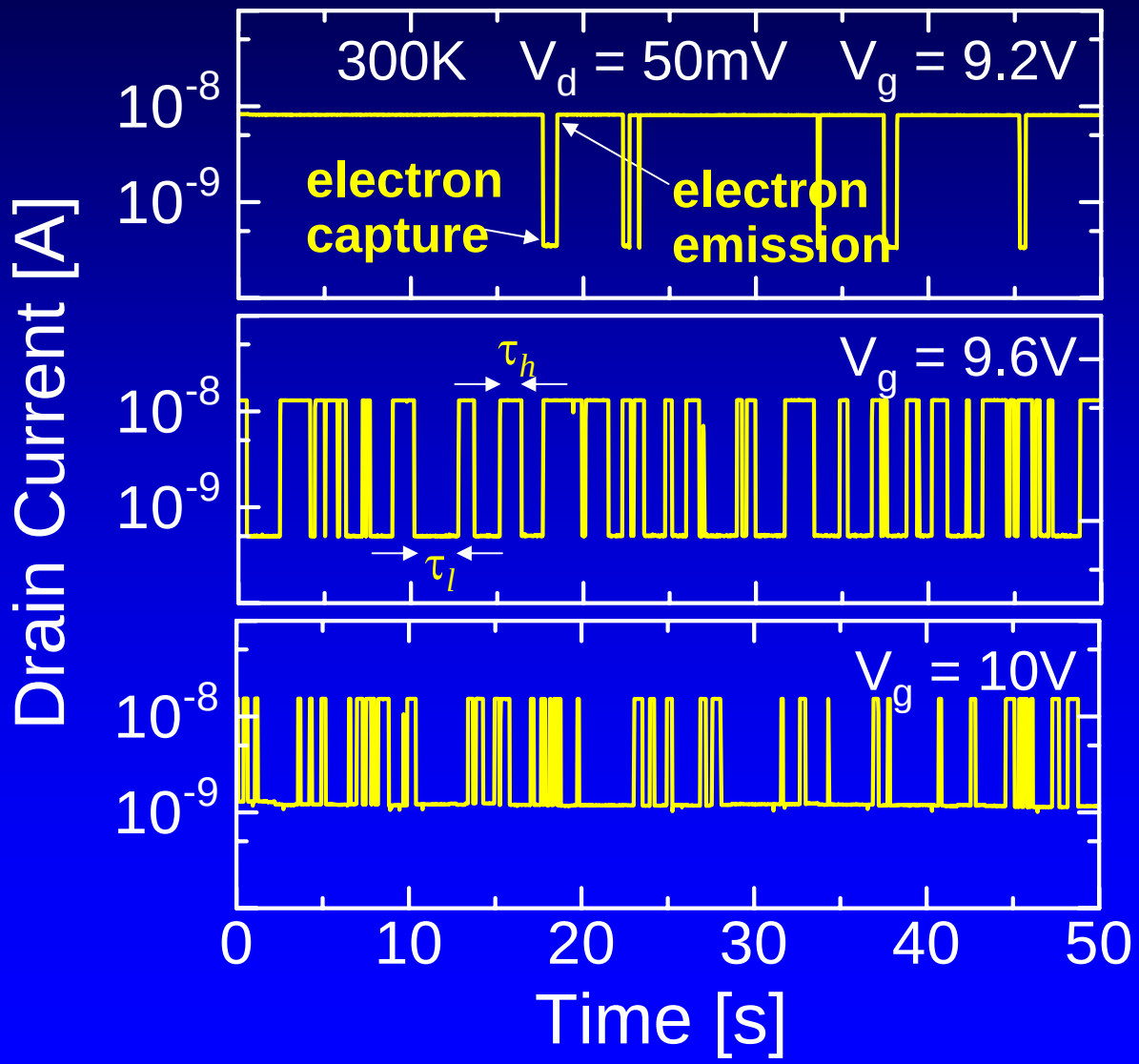
I_d-V_g Characteristics



Single-electron C/E process is thermal activation process.

The electron pocket is not in the oxide.

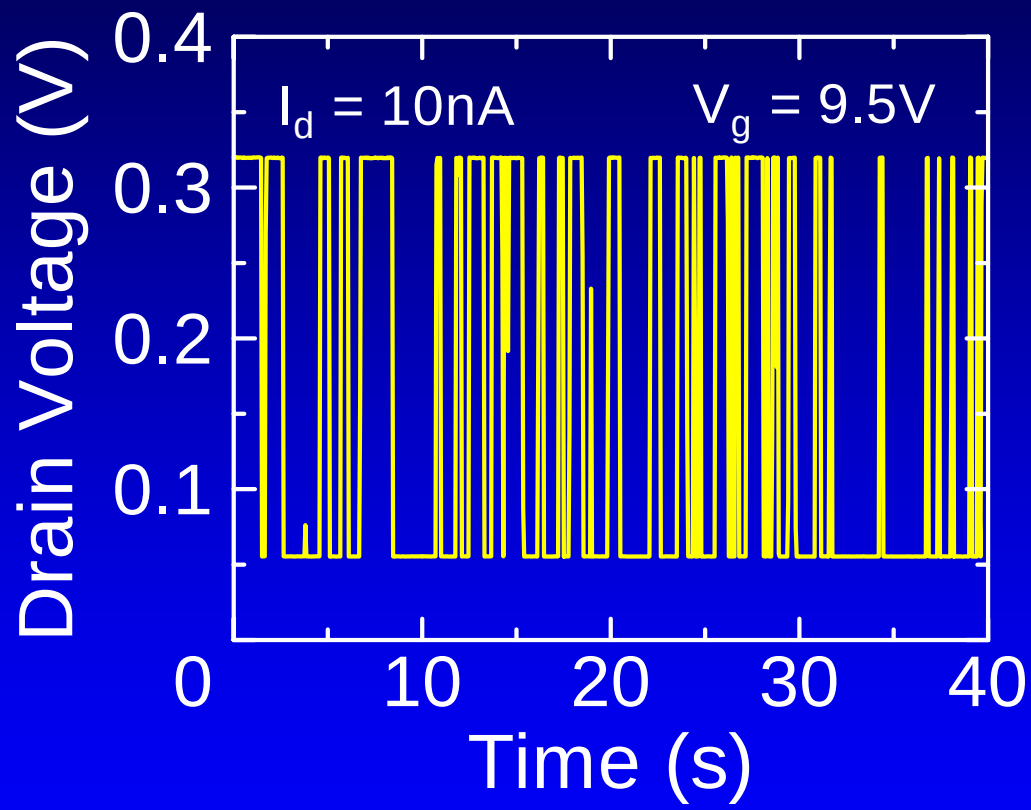
Time Dependence of I_d



RTS: Random Telegraphic Signal

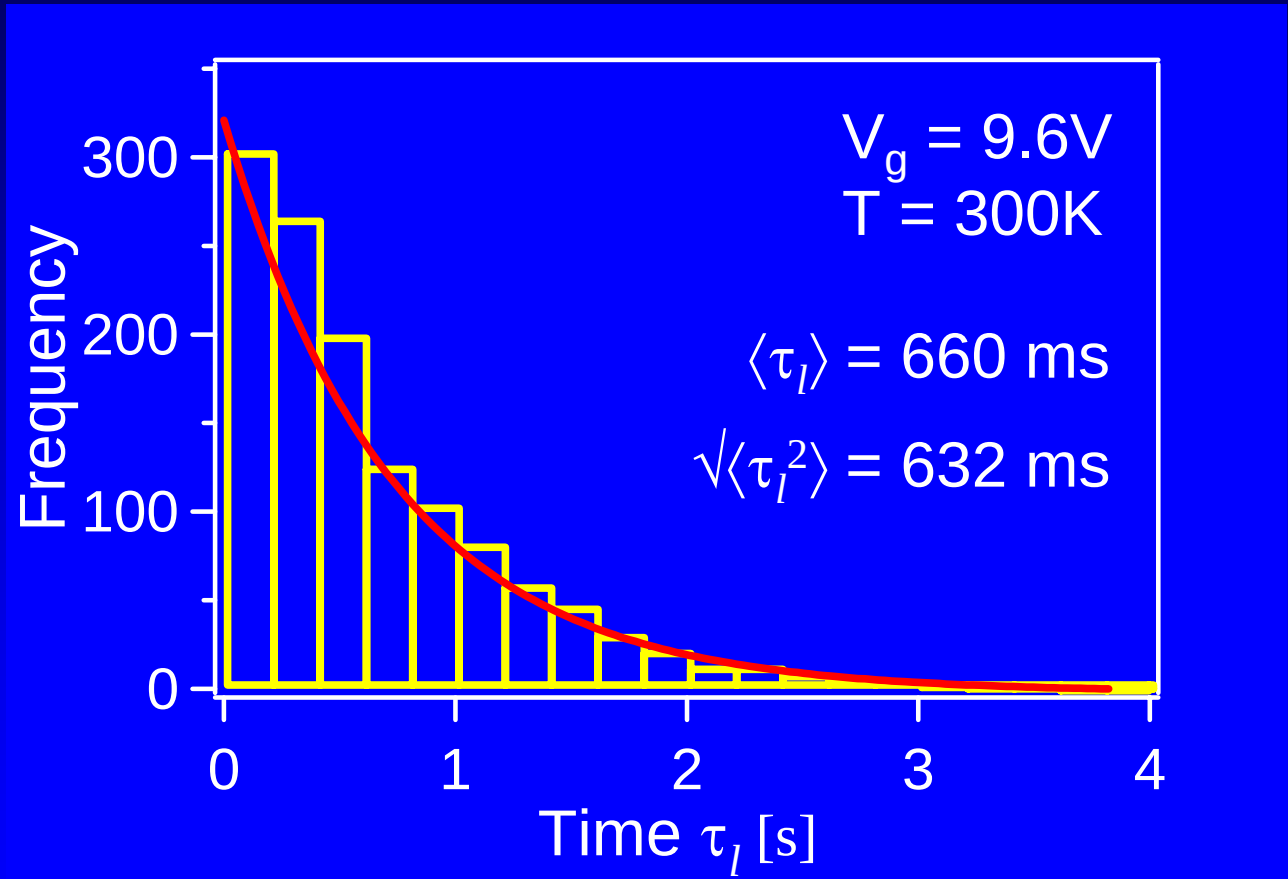
RTS ratio ($\Delta I_d/I_d$) is greater than one decade, which is the highest RTS ratio.

Time Dependence of V_d

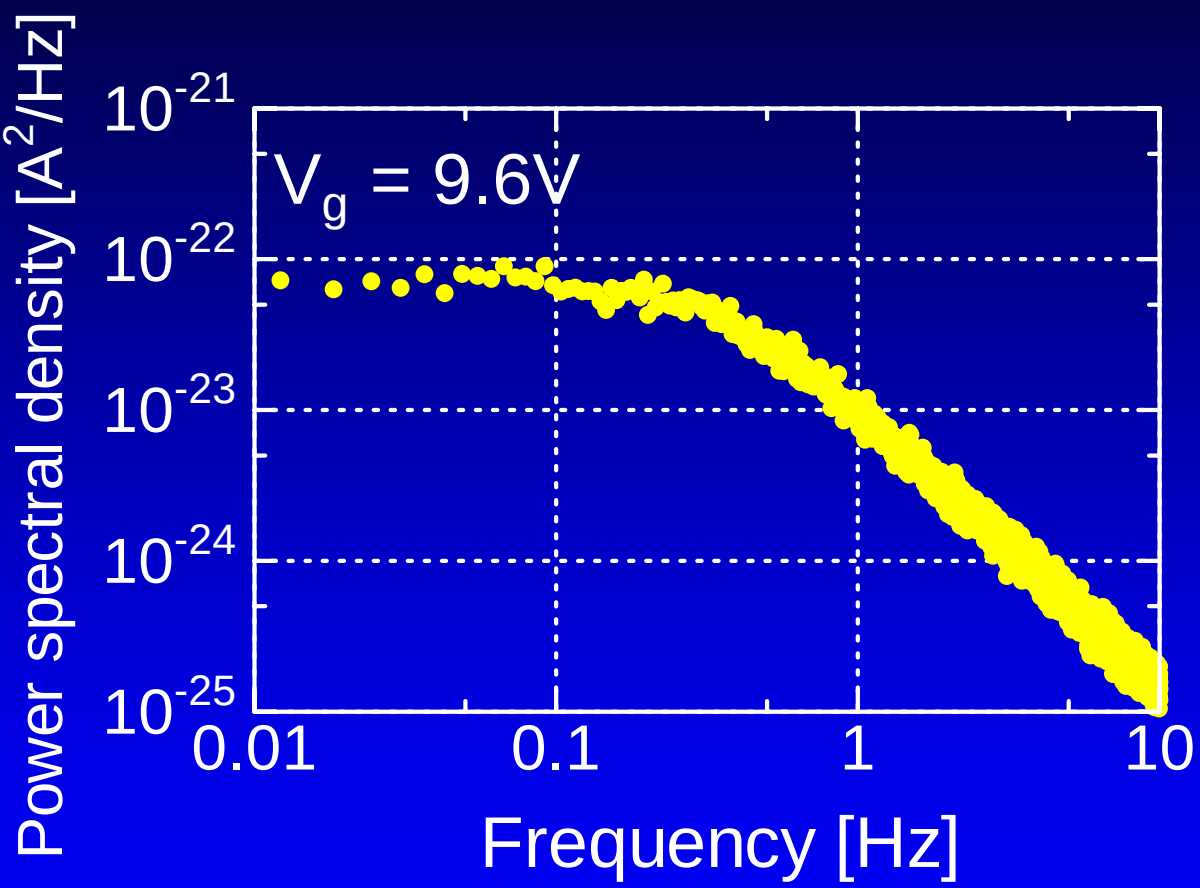


No need for high-gain amplifier.

Distribution of low time (τ_l)



Power Spectrum Density of I_d



Single-electron C/E process is a stochastic process (Poisson process).

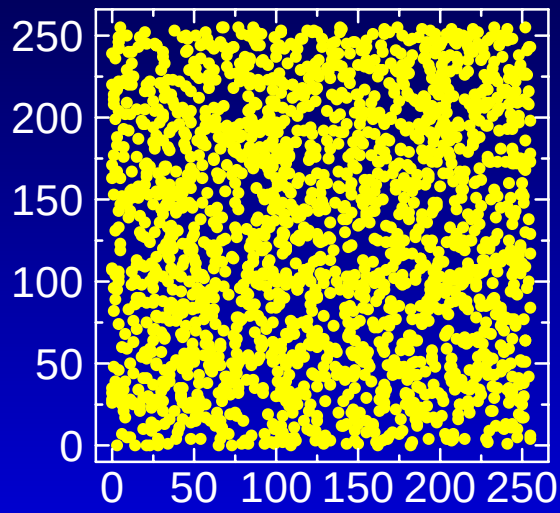
Results of Tests for Random Number -Tests for Re-Sampled Data-

	Test	Pass Condition	Noise-based RNG	This Work
FIPS PUB 104-2	Monobit	9655 - 10346	10059 ***Pass!***	10043 ***Pass!***
	Poker	2.16-46.17	10.23 ***Pass!***	15.88 ***Pass!***
	Longest Run	1 - 33	15 ***Pass!***	14 ***Pass!***
	Runs of length 1	2267 - 2733	[0] 2588 ***Pass!*** [1] 2564 ***Pass!***	[0] 2462 ***Pass!*** [1] 2409 ***Pass!***
	Runs of length 2	1079 - 1421	[0] 1282 ***Pass!*** [1] 1246 ***Pass!***	[0] 1243 ***Pass!*** [1] 1296 ***Pass!***
	Runs of length 3	502 - 748	[0] 610 ***Pass!*** [1] 650 ***Pass!***	[0] 647 ***Pass!*** [1] 586 ***Pass!***
	Runs of length 4	223 - 402	[0] 302 ***Pass!*** [1] 327 ***Pass!***	[0] 290 ***Pass!*** [1] 329 ***Pass!***
	Runs of length 5	90 - 223	[0] 148 ***Pass!*** [1] 139 ***Pass!***	[0] 147 ***Pass!*** [1] 177 ***Pass!***
	Runs of length 6+	90 - 223	[0] 144 ***Pass!*** [1] 148 ***Pass!***	[0] 166 ***Pass!*** [1] 158 ***Pass!***
NIST SP 800-22	χ^2	>0.05	0.140 ***Pass!***	0.648 ***Pass!***
	Run	>0.01	0.153 ***Pass!***	0.556 ***Pass!***
	Freq. within block	>0.05	0.744 ***Pass!***	0.508 ***Pass!***
	Freq.	>0.05	0.275 ***Pass!***	0.085 ***Pass!***
	Serial	>0.05	0.106 ***Pass!***	0.693 ***Pass!***
	Serial Correlation	-0.023 - 0.022	-0.016 ***Pass!***	0.006 ***Pass!***
	Poker	>0.05	0.306 ***Pass!***	0.703 ***Pass!***
	Gap of '1'~'16'	>0.05	***Pass all!*** 0.08 - 0.90	***Pass all!*** 0.15 - 0.94

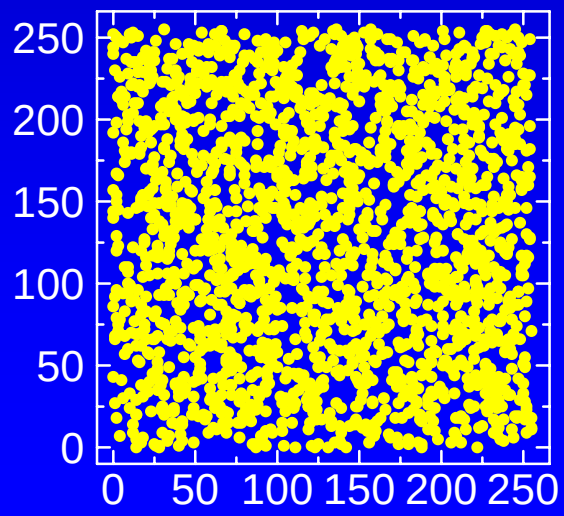
The score of the single-electron RNG is comparable to or even superior to that of the stat-of-the-art high-quality RNG.

Self-Correlation Plots

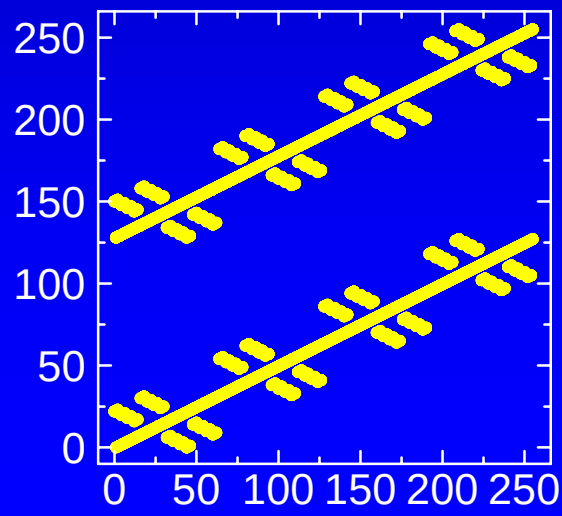
Single-electron RNG



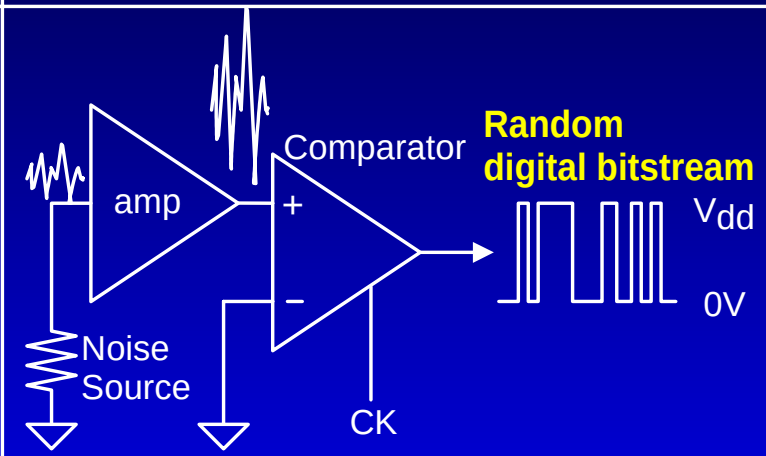
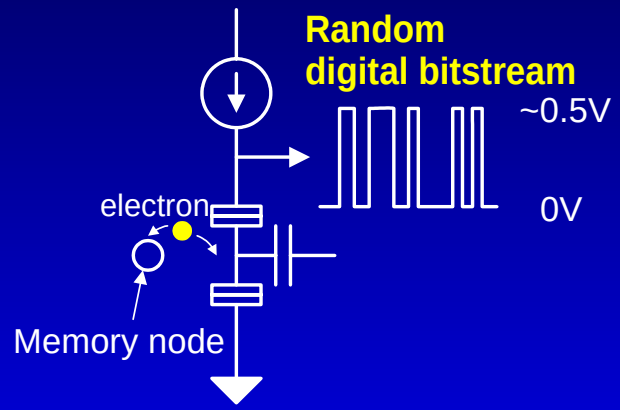
Thermal-noise-based RNG



Pseudo RNG (LFSR)



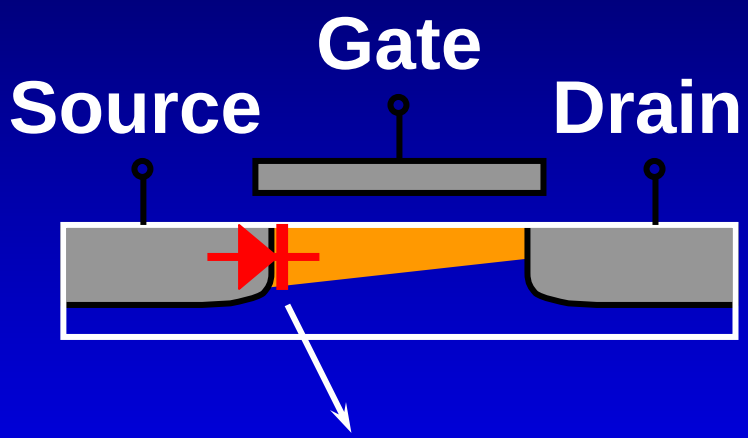
Advantage of Single-Electron RNG

	Conventional high-quality RNG	**This Work**
		
Source	Thermal noise, Shot noise	Single-electron C/E process
Noise V_{rms}	~0.01mV	120mV
Size	On-board (0.01-1000cm^2)	On-chip (~100μm^2)
Power	10mW-1W	1.5nW

Schottky Source/Drain MOSFETs

Introduction

Schottky source/drain MOSFETs



- Simple fabrication
- Low electrode resistances
- Better short-channel effect control
- Excellent junction abruptness

Schottky barrier at source / channel interface significantly lowers the driving current.

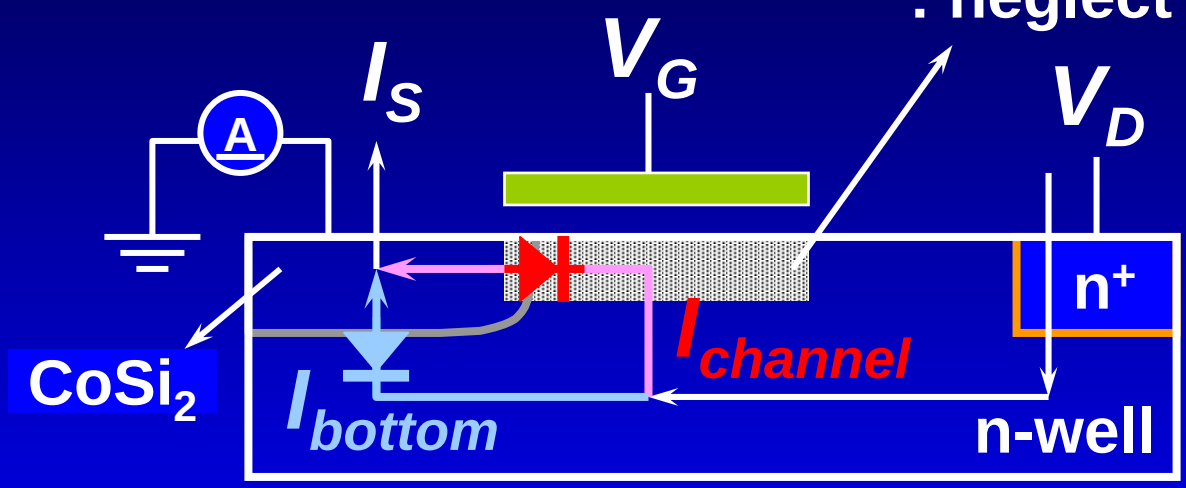
In this study...

➡ Effect of gate voltage on Schottky barrier height ϕ_B is thoroughly investigated.

A. Kinoshita et al., SSDM 2003

Sample structure and measurement setup

accumulation layer
: neglect pinch-off effect



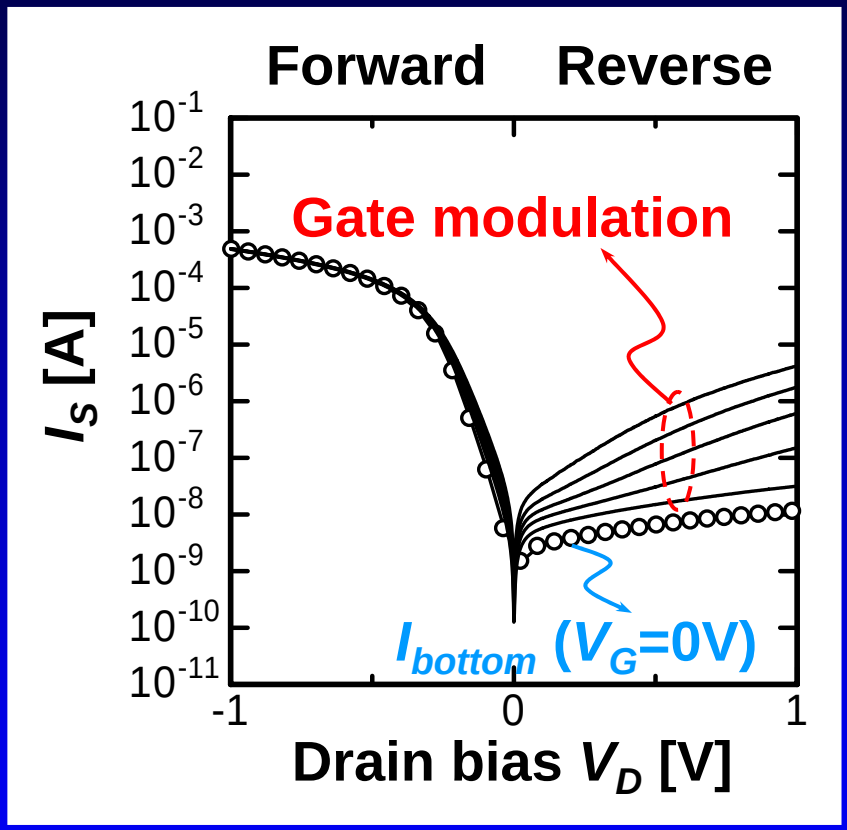
- T_{ox} = 10nm
- L/W = 10/10μm
- N_d = 1E17cm^{-3}
- V_G: 0 ~ 5V

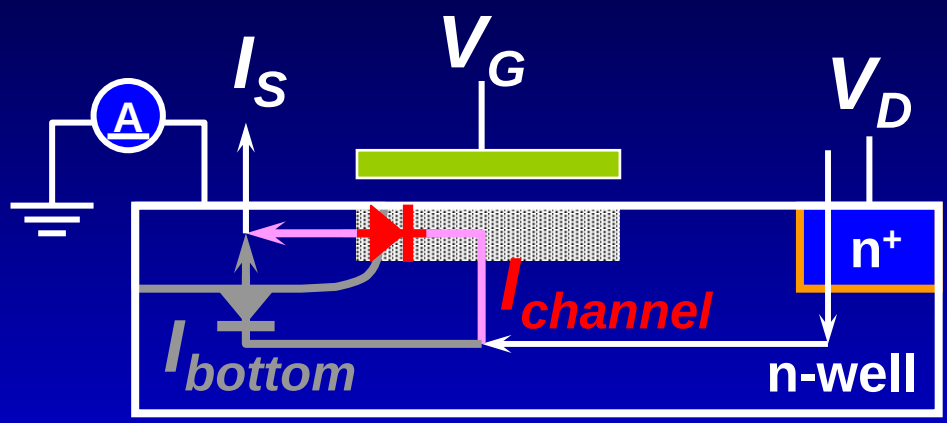
$$I_{channel} = I_S - I_{bottom}$$

($I_{bottom} \equiv I_S$ at V_G: 0V)

Gate modulation current ($I_{channel}$) can be extracted by subtracting I_{bottom} from I_S.

Measured I_S characteristics



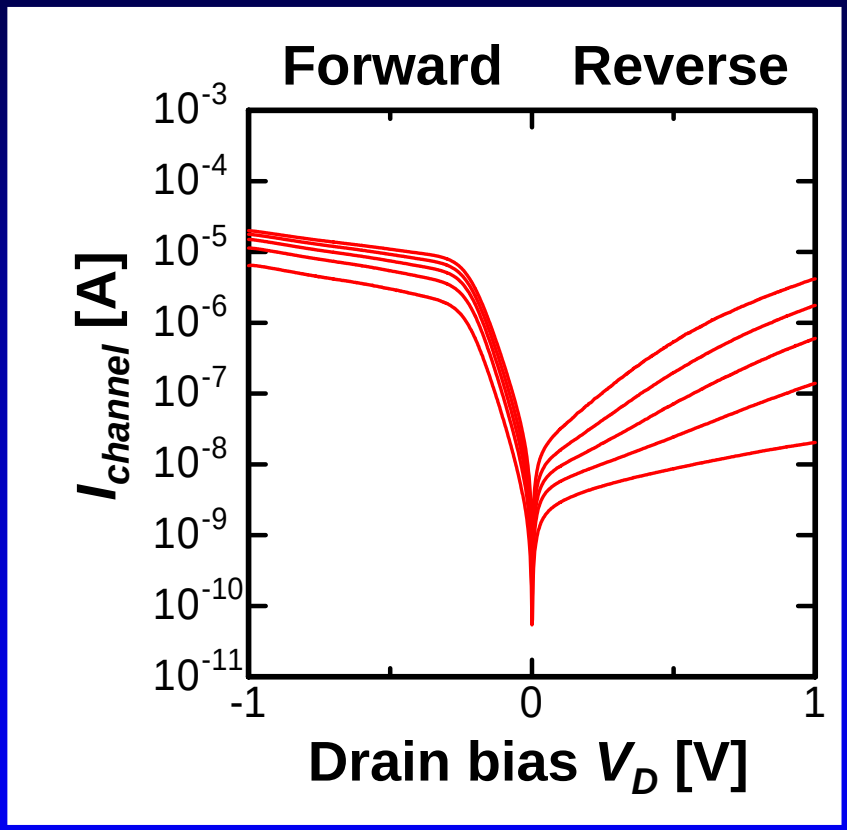


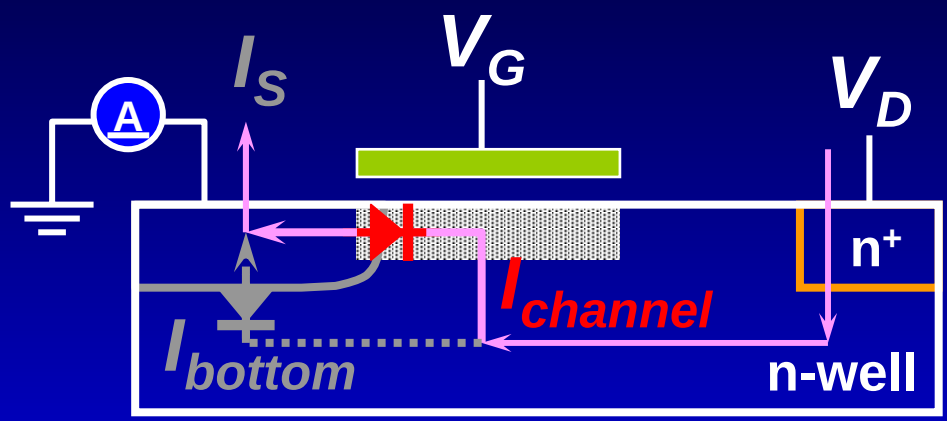
- V_G: 0 ~ 5V (1V step)
- Measured at 300K

V_G strongly modulates reverse current of the surface Schottky diode.

A. Kinoshita et al., SSDM 2003

Extracted $I_{channel}$ characteristics



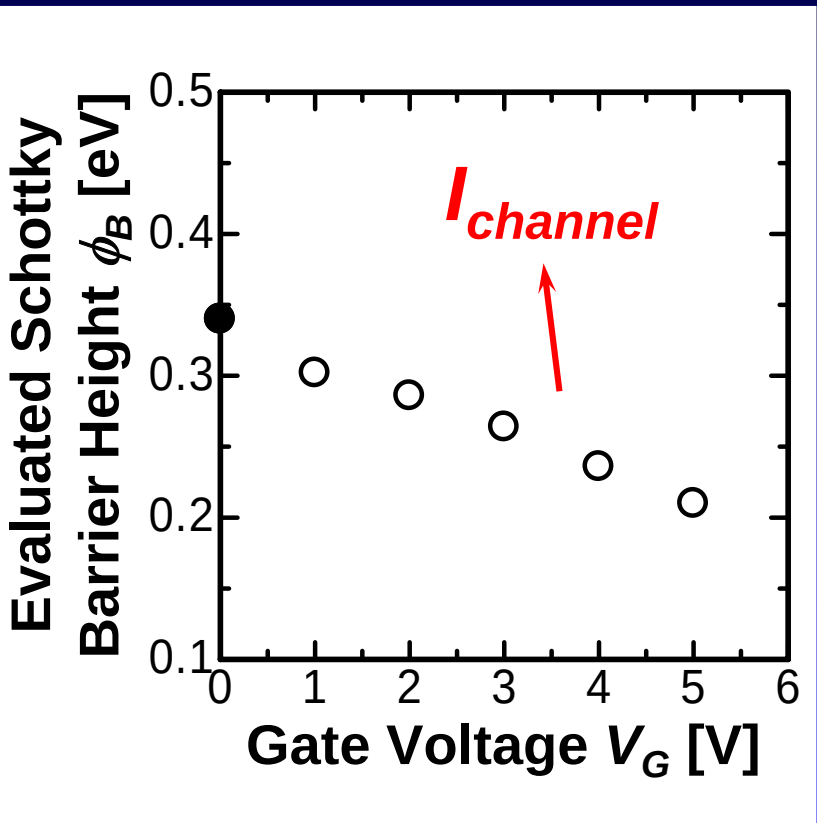


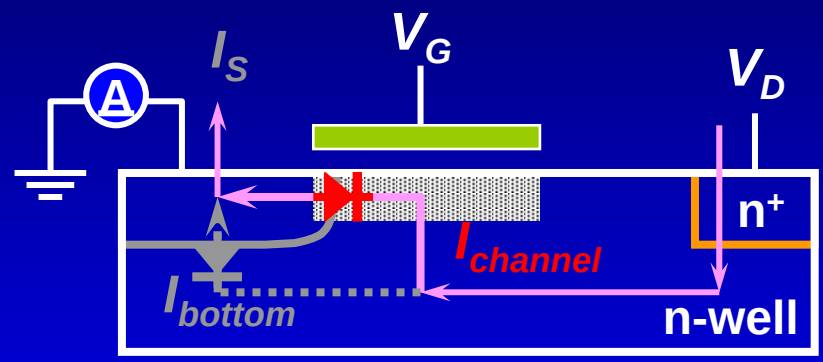
- V_G: 1 ~ 5V (1V step)
- Measured at 300K

Gate modulation current ($I_{channel}$) is successfully extracted.

A. Kinoshita et al., SSDM 2003

Evaluated Schottky barrier height

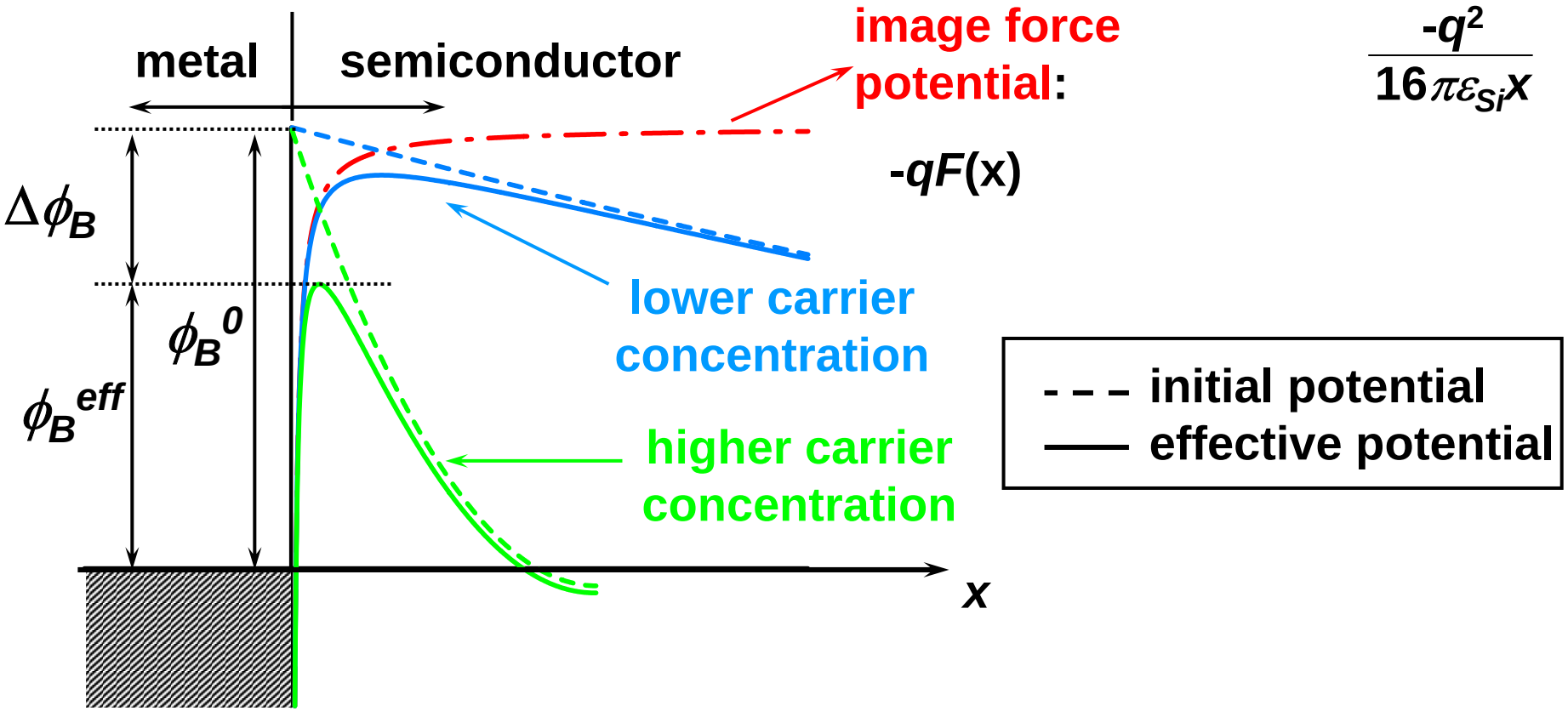




First experimental evidence of barrier height lowering due to gate electrical field.

A. Kinoshita et al., SSDM 2003

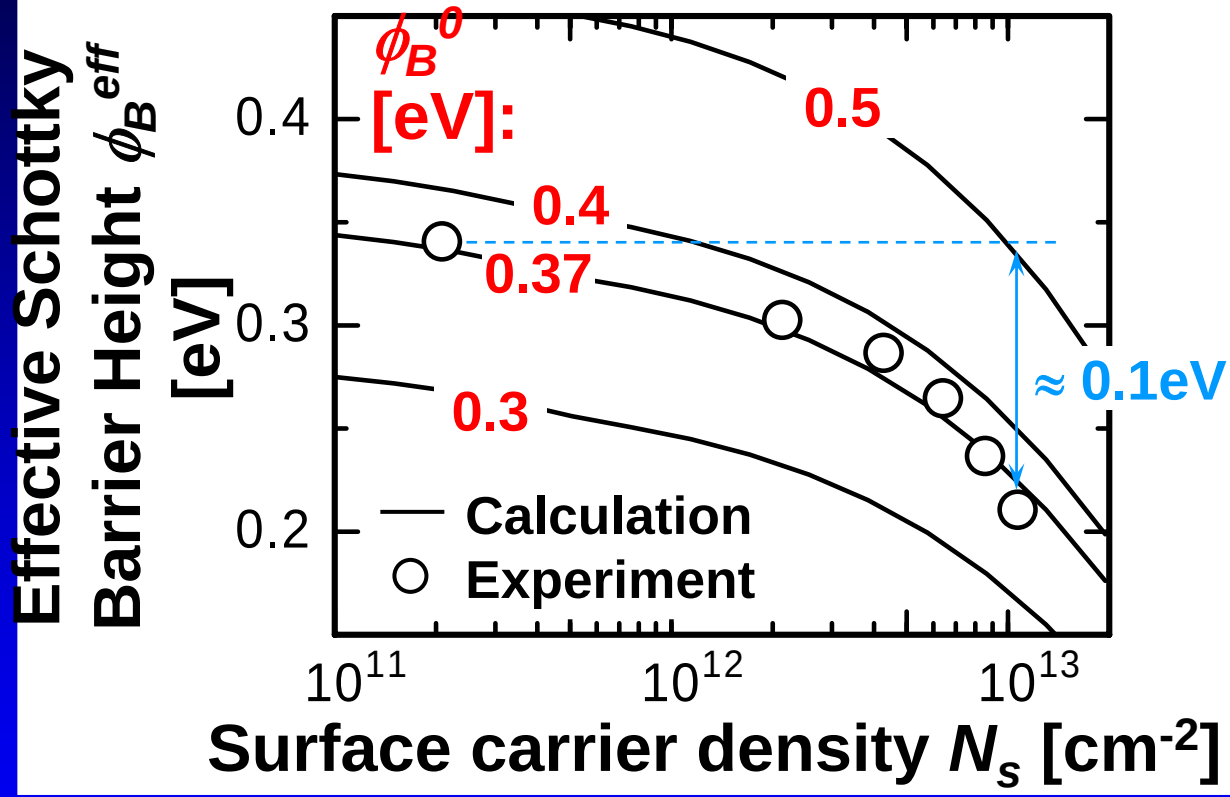
Image force potential



Effective Schottky barrier height can be modulated by carrier concentration

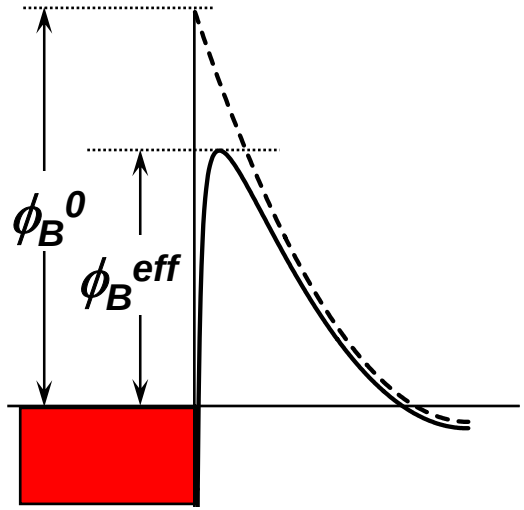
A. Kinoshita et al., SSDM 2003

ϕ_B lowering due to image force potential



Calculation:

- 1D Poisson equation
- Full depletion approximation



Good agreement of the calculated and experimental results suggests image force potential is the origin of the gate induced barrier height lowering.

A. Kinoshita et al., SSDM 2003

Conclusions

- In nanodevice era, we will encounter a number of challenges. However, if we can deal with those challenges, we will have new opportunities.
- In Ultrathin-body MOSFETs, quantum mechanical effects are very important. The QM effects offer us subband structure engineering.
- It is difficult to fabricate LSI of Single-Electron Devices. However, one single-electron device might enhance the security of LSI chips.
- In Schottky Source/Drain MOSFETs, Schottky brier at the source side plays a crucial role. However, the source side barrier might offers us another opportunity.