Engineering of Interfacial Layer between high-*k* (ZrO_2, HfO_2) and Semiconductor (Si, Ge)

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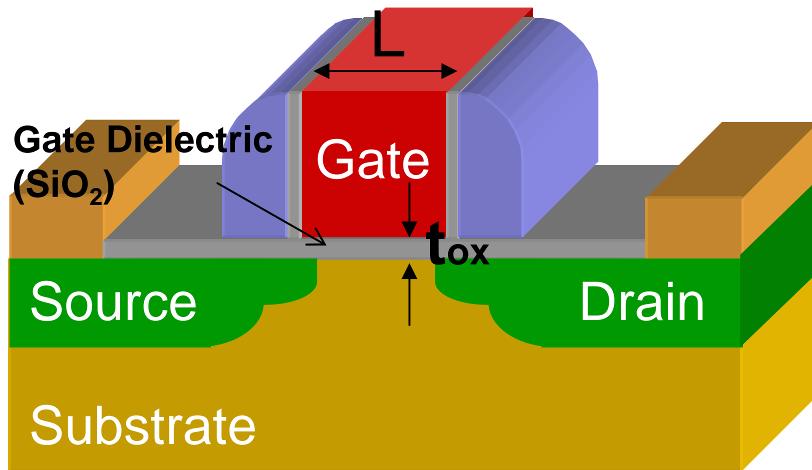
Outline

- Motivation
  - Scaling limit of MOS Gate Dielectric
  - Interface Issues in high-*k*/semiconductor (Si, Ge)
- Interfacial layer Engineering of high-*k* (ZrO_2) / Si(001) by Solid State Reaction
  - XPS, TEM, Electrical Results
- Chemical structures and Band alignment at HfO_2 / Ge(001) interface
  - SR-PES, Electrical Results
- Conclusions

Scaling of Si-MOSFETs



- Why we scale MOSFET ?
  - Increase Packing Density
    → Cost Down
  - Improve Performance
    (Speed ~ 1/L, $1/t_{ox}$)

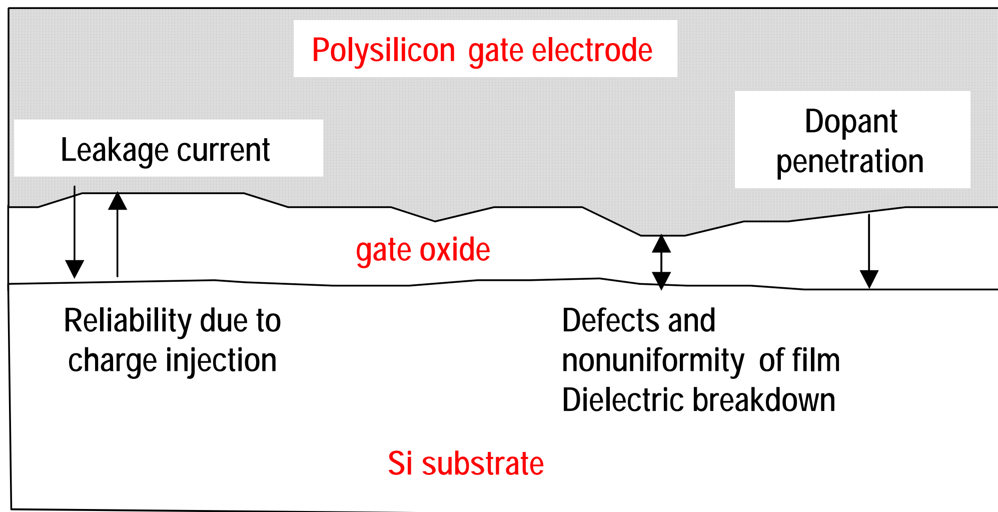
- Gate Oxide Scaling

Timp, *et al*, *Tech. Dig. Int. Elec. Dev. Meet.*, 1999

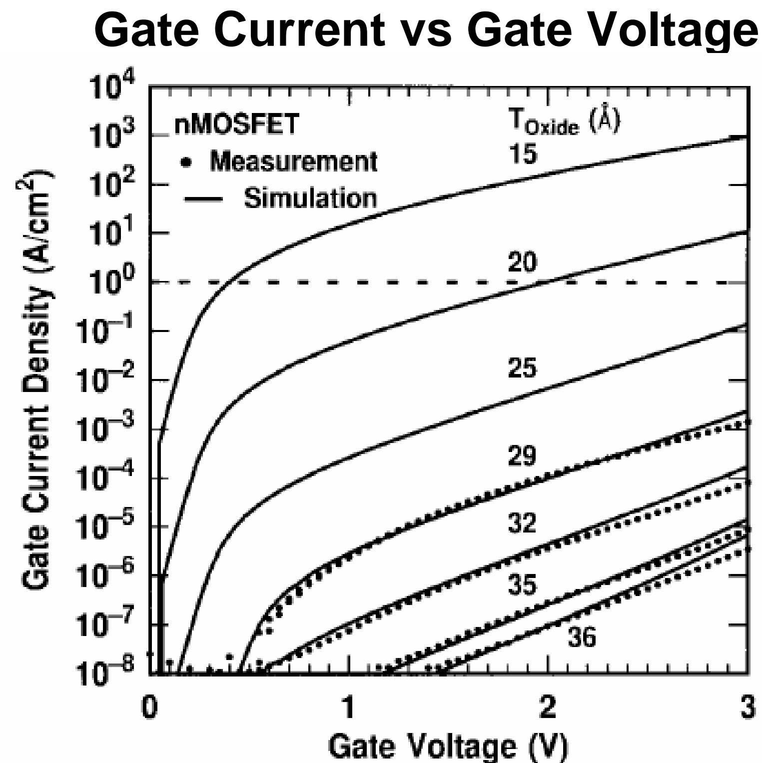
Year	Gate Length (nm)	EOT (nm)
1999	140	1.9-2.5
2000	120	1.2-2.5
2001	100	1.5-1.9
2002	85	1.5-1.9
2003	80	1.5-1.9
2004	70	1.2-1.5
2005	65	1.0-1.5
2008	45	0.8-1.2
2011	32	0.6-0.8
2014	22	0.5-0.6

How far we can push the gate oxide scaling ?

Problems in Scaling of Gate Oxide



Gate Current vs Gate Voltage

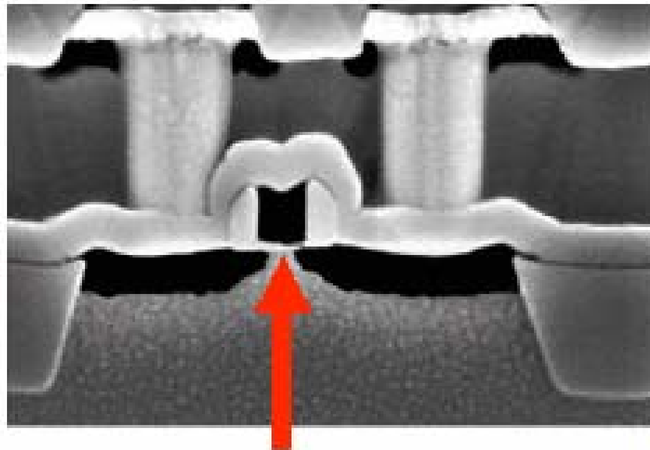


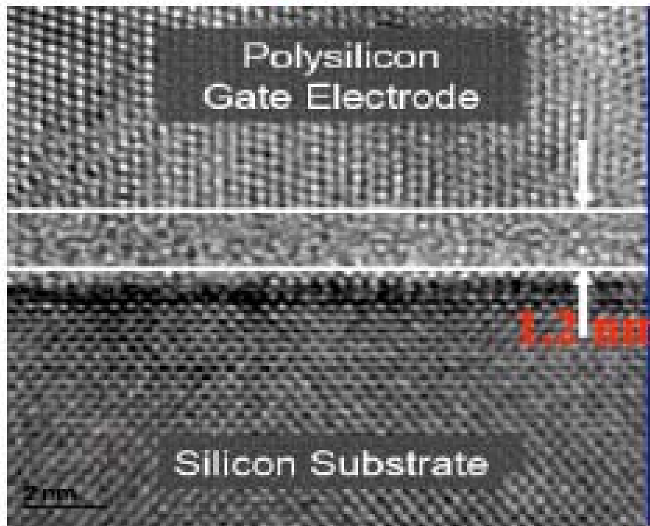
From S. Y. Lo et al., IEEE EDL, May 1997.

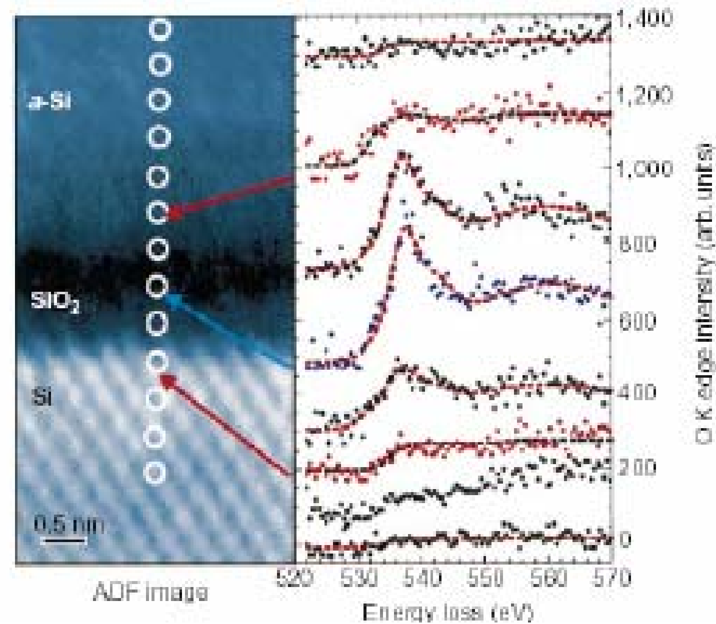
- Below 20 Å problems with SiO_2
  - Gate leakage => circuit instability, power dissipation
  - Degradation and breakdown
  - Dopant penetration through gate oxide
  - Defects

Below ~20 Å direct tunneling causes excessive gate current

Fundamental Limit of Gate Oxide Thickness







- EELS O-k edge spectra recorded point by point across a gate stack containing a thin SiO_2
- Bulk SiO_2 properties (e.g. large bandgap) lost for film thickness ≤8Å

D.A. Muller et al., Nature, 399, 758-761 (1999)

Why High-*k* MOS Gate Dielectrics ?

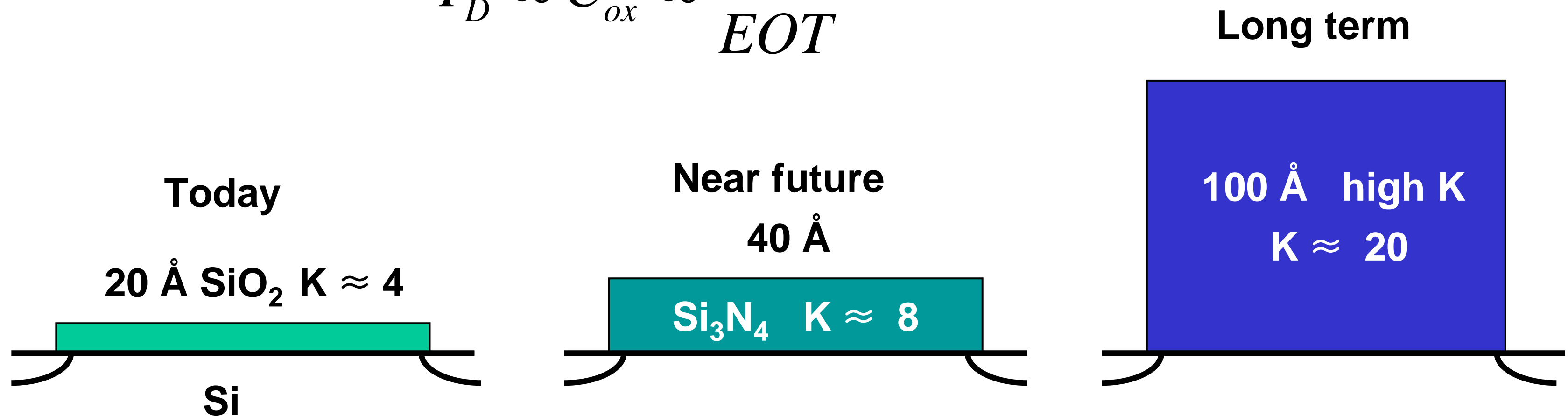
$I_{channel} \propto$ *charge x source injection velocity*

$\propto$ *(gate oxide cap x gate overdrive)* v_{inj}

$\propto C_{ox} (V_{GS} - V_T)\ E_{source}\ \mu_{inj}$

Historically C_{ox} has been increased by decreasing gate oxide thickness. It can also be increased by using a higher K dielectric

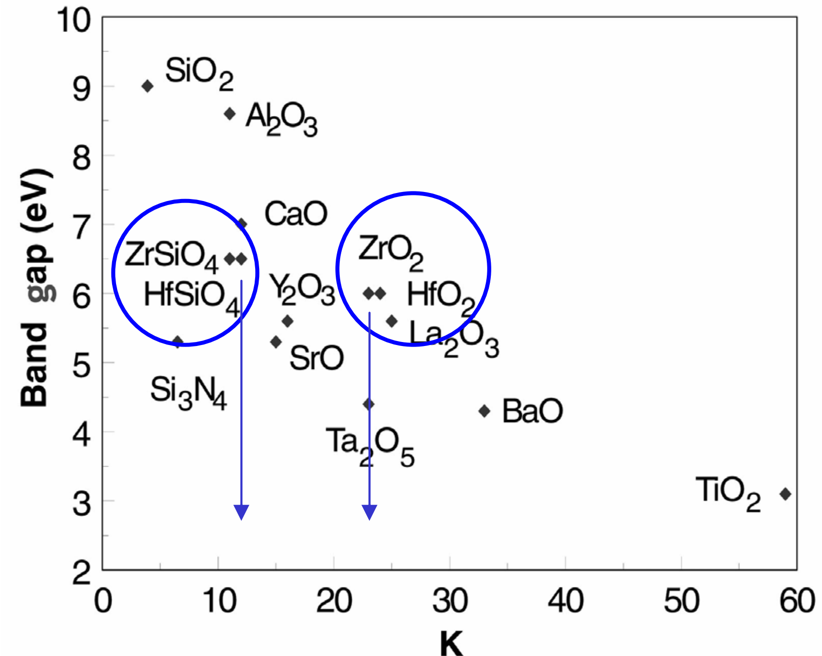
$$I_D \propto C_{ox} \propto \frac{K}{EOT}$$



Same Electrical Thickness (EOT)→ same C_{ox}
Larger physical thickness → Reduce gate leakage

Requirements for the high-k dielectrics

• High dielectric constant ⇒ higher charge induced in the channel
• Wide band gap ⇒ higher barriers ⇒ lower leakage
• Thermodynamically stable on Si(001)
• Low bulk and interfacial trap densities.
• Stability at higher processing temperatures and environments

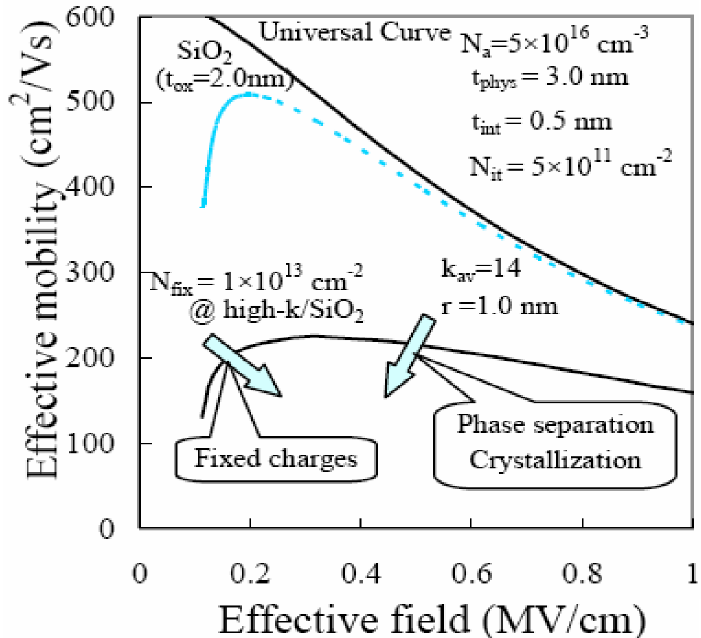


Robertson, J., Appl. Surf. Sci. (2002) 190 (1-4), 2

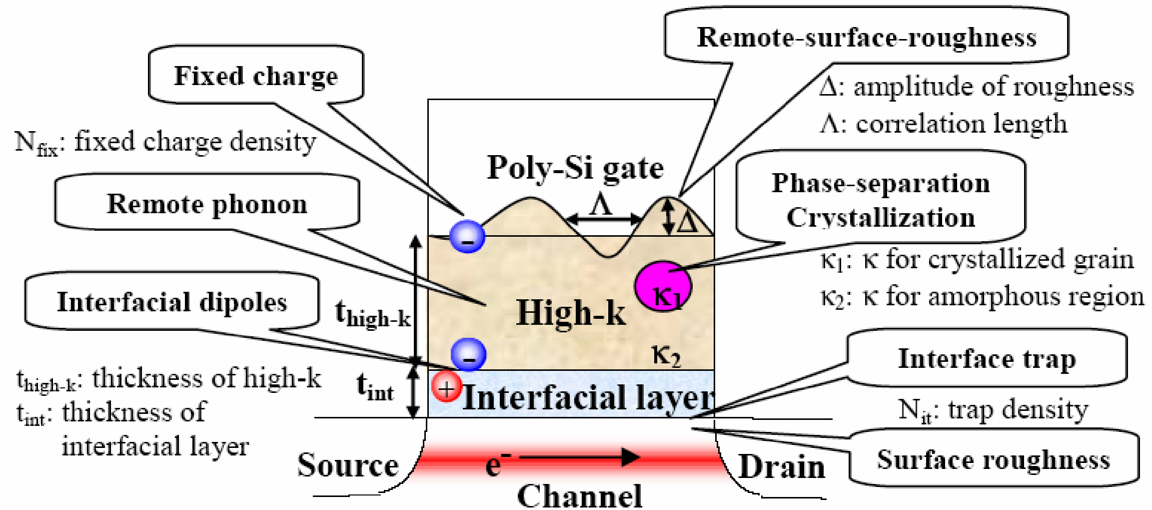
➔ ZrO_2, HfO_2, amorphous Zr and Hf-silicate (with nitridation) are the promising candidates

Problems in High-k Dielectrics - 1

- **Mobility Degradation**



- **Possible Sources for Reduced Mobility in High- K Gate Stacks**

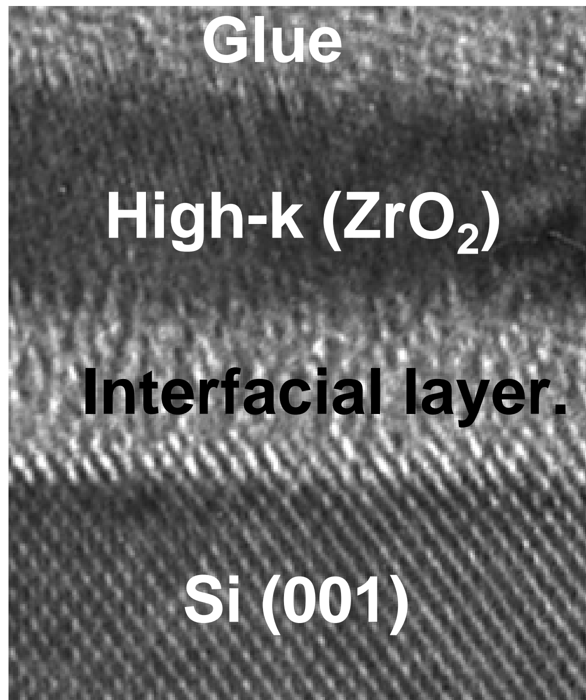


S. Saito, et al., IEEE IEDM, Washington, DC, Dec., 2003.

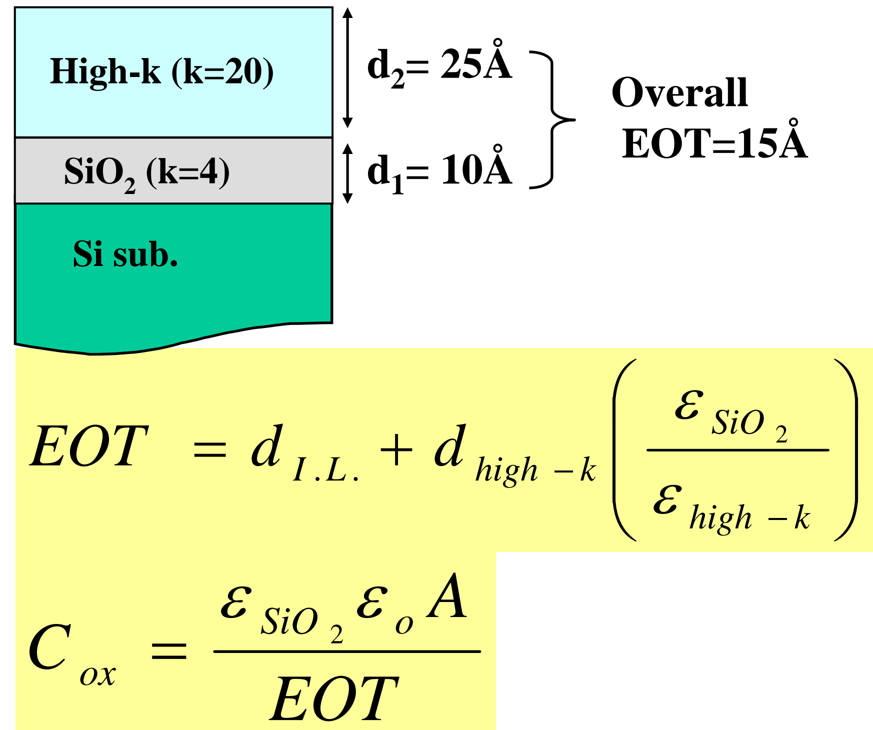
→**Mobility degradation is believed to be associated with the physical and electrical defects at the high-*k*/ Si(001) interface**
→ **Understanding the physical nature of the interfacial layer has been studied extensively**

Problems in High-k Dielectrics - 2

- Unavoidable SiO_2 like interfacial layer (I.L) with low-*k* dielectric constant forms either during high-k deposition or post-deposition thermal treatment that determines overall capacitance



XTEM picture of ZrO_2/I.L./Si(001)

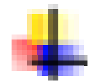


$$EOT = d_{I.L.} + d_{high-k}\left(\frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}}\right)$$

$$C_{ox} = \frac{\varepsilon_{SiO_2}\varepsilon_o A}{EOT}$$

→ Need to minimize the I.L. layer or increase the dielectric constant of I.L.

Outline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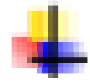
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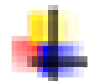
- XPS, TEM, Electrical Results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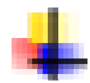
- SR-PES, Electrical Results


Conclusions

Modulation of I.L. by Solid State Reaction

- By controlling solid state reaction kinetics after metal deposition, physical and electrical properties of I.L can be modulated.

Metal (Zr) depo.

Metal (Zr)
SiO_2
Si sub.

in-situ Vacuum Annealing

$(Zr + ZrO_x)$
Si sub.

Possible reduction of interfacial SiO_2

$SiO_2 + Zr \rightarrow ZrO_2 + Si$

(ΔG = -185 J/mol)

in-situ UV-O_3 oxidation of residual metal to form stoichiometric ZrO_2

ZrO_2
Si sub.

thinner or higher-*k* interfacial layer
→ Decrease EOT

XPS results after Zr depo. and Vacuum Anneal

Zr 3nm depo. on ~1.5nm Chemical SiO_2/Si → *in-situ* Vacuum Anneal (<$5x10^{-7}$ Torr, 200^oC, 30min) → *ex-situ* XPS

(a) Si *2p*

Si-sub.

Zr-Si

SiO_2

~0.4eV

Zr 3nm + Anneal

~99.3eV

~103.3eV

Zr 3nm as-dep.

Intensity (a.u.)

108 106 104 102 100 98 96

Binding Energy (eV)

(b) Zr *3d*

Zr 3nm as-dep.

Zr 3nm+Anneal

Zr $3d_{5/2}$ in ZrO_2

Zr $3d_{3/2}$ in ZrO_2

Zr $3d_{5/2}$ in Zr-silicide

Intensity (a.u.)

188 186 184 182 180 178 176

Binding Energy (eV)

- **Initial SiO_2 passivation layer dissociate forming Silicate or suboxide even at as-dep. Sample and this reaction is enhanced by *in-situ* anneal**
- **Vacuum anneal promote Zr-slilcide bond formation through partial decomposition of initial SiO_2 layer**

XPS results after UV-oxidation

(a) Si *2p*

Si sub.

Si in Zr-silicate

Si in SiO_2

~2.9eV

~4.0eV

(3)

(2)

(1)

Intensity (a.u.)

108 106 104 102 100 98 96

Binding Energy (eV)

(b) O *1s*

O in Zr-silicate

O in ZrO_2

O in SiO_2

~1.7eV

(3)

(2)

(1)

Intensity (a.u.)

538 536 534 532 530 528 526

Binding Energy (eV)

(c) Zr *3d*

Zr $3d_{5/2}$ in ZrO_2

Zr $3d_{5/2}$ in Z-silicate

(3)

(2)

(upper-lower) x 5

Intensity (a.u.)

188 186 184 182 180

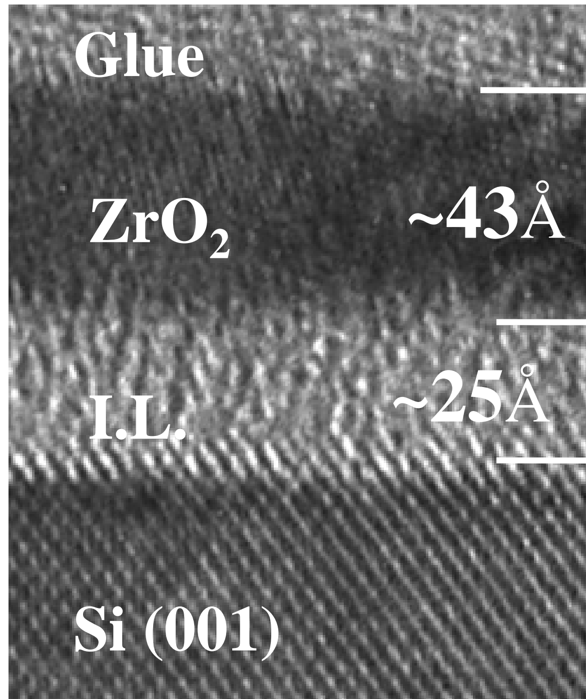
Binding Energy (eV)

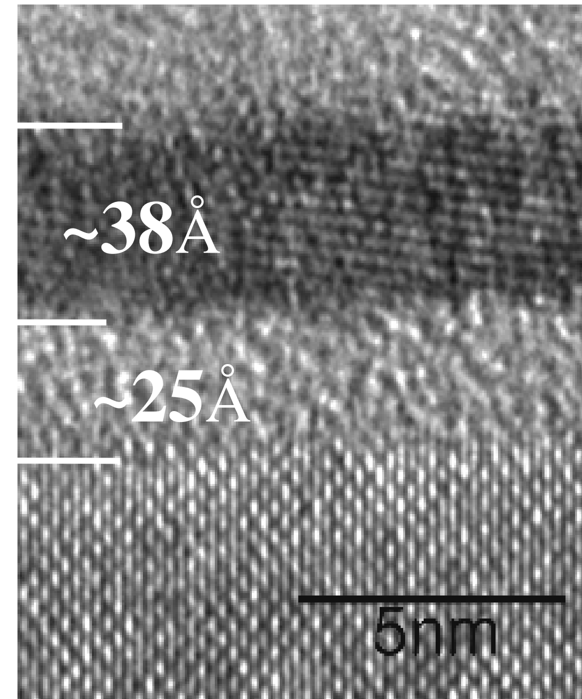
(1) Si with chemical SiO2, (2) Zr 3nm + UVO, (3) Zr 3nm + Anneal + UVO

- **Zr-silicide formed after vacuum annealing was oxidized to form a Zr-silicate phase in the subsequent UV-ozone oxidation treatment in the interfacial layer between ZrO2 / Si(001)**

XTEM (with vs. without Vacuum Anneal)

w/o Vacuum Anneal | **with Vacuum Anneal**



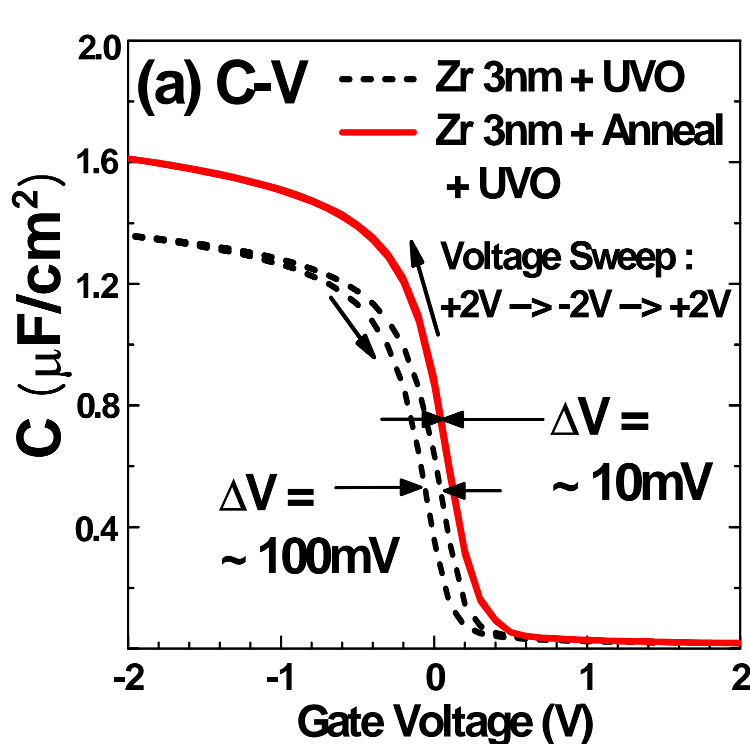


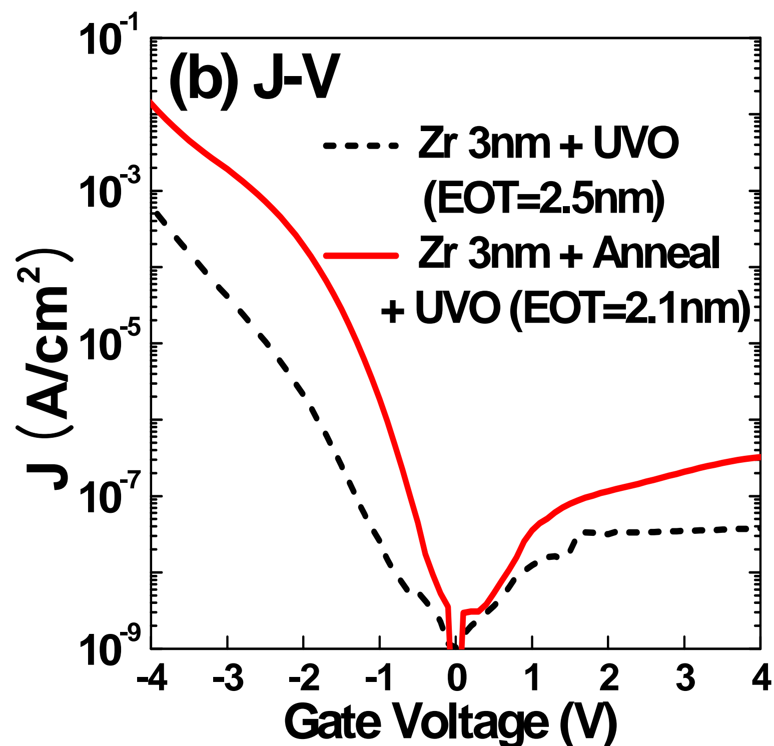
EOT (from C-V) =25.4Å
Assume k (ZrO_2) = 20
k_{eff} (I.L.) = 5.8

EOT (from C-V) =21.3Å
Assume k (ZrO_2) = 20
k_{eff} (I.L.) = 7.2

→ Higher-*k* Zr-silicate I.L. formed in the vacuum annealed sample

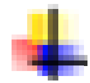
C-V and J-V (with vs. without Vacuum Anneal)





➔ Vacuum annealed samples containing the silicate interface layer exhibited excellent dielectric characteristics, such as negligible capacitance-voltage hysteresis (~ 10mV), lower fixed charge density as well as reduced EOT (~4Å) compared to un-annealed samples.

Outline

 Motivation

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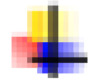 Interfacial layer Engineering of high-*k* (ZrO_2) / Si(001) by Solid State Reaction

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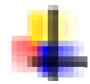
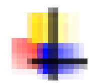
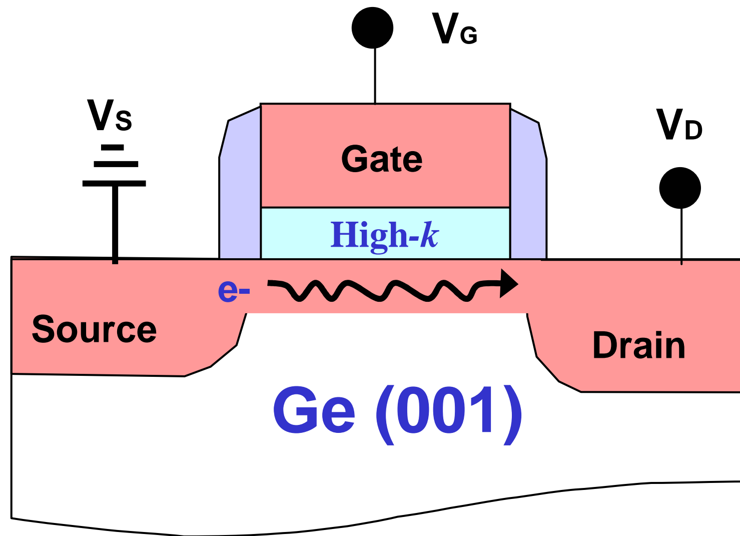
 **Chemical structures and Band alignment at HfO_2 / Ge(001) interface**

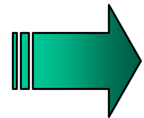
- **SR-PES, Electrical Results**

 Conclusions

Benefit of High-*k* on Ge channel



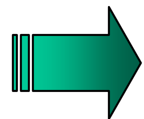
- High-κ Gate Dielectrics → Avoid poor quality GeO_2 & Improve C_{ox}
- Ge channel → Intrinsic Mobility enhancement ; electron (2x) and hole (4x) compared to Si (001)



$$I_{channel} \propto \text{charge} \bullet \text{source injection velocity}$$

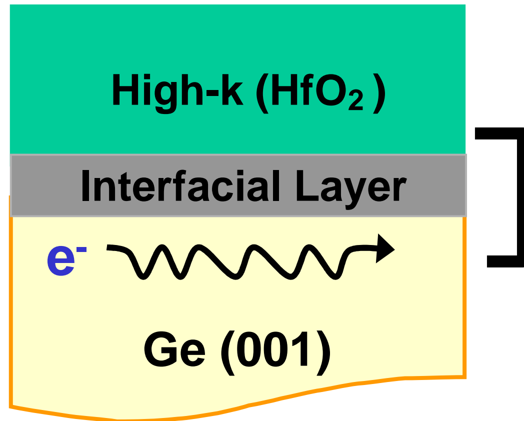
$$\propto (\varepsilon_r \, \varepsilon_o A / t_{ox}) \bullet (V_{GS} - V_{th}) \bullet (E_{source} \times \mu_{inj})$$

Better performance can be achieved by combining high-*k* gate dielectric and high mobility Ge channel



GeO_xN_y, Al_2O_3, ZrO_2, and HfO_2 have recently been studied as a high-*k* gate insulators on Ge,

Why does interface matter ?

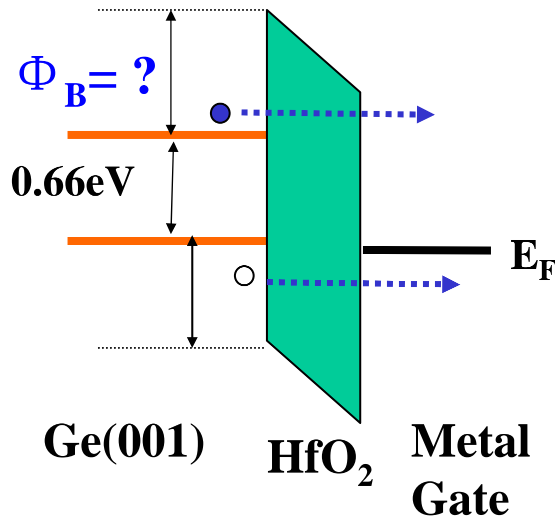


- Physical and electrical structure at the interface is critical

- Chemical bonding nature → C-V, charge trapping, carrier scattering, etc...

- Energy band alignment → I-V, conduction mechanism through dielectric

$$I_{tunneling} \propto \exp\left(-\frac{\Phi_B}{t_{ox}}\right)$$



→ Photoemission study can provide both chemical bonding structure and valence band alignment at the interface

Synchrotron Radiation Photoemission Spectroscopy (SR-PES) Features @ SSRL

1. **Spectroscopy Characteristics ;**
   - Tunable (20~1500eV) Synchrotron Photon energy
   - Analyzer of PHI model 10-360 : Energy resolution of ~0.05 eV
   - Analyzer chamber base pressure : ~5×10^{-11} Torr

2. ***hv*= 80eV is chosen,**
   - **Core-level Binding Energy**

     Ge : *$3d_{3/2}$* (29.8eV), $3d_{5/2}$ (29.2eV)

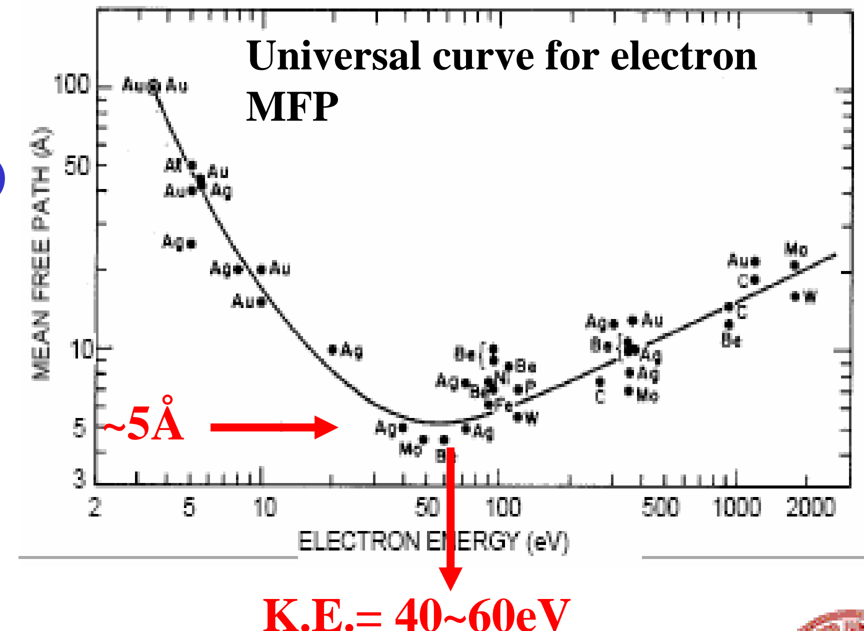
     Hf : *$4f_{5/2}$* (15.9eV), *$4f_{7/2}$* (14.2eV)

     → K.E = *hv* – B.E. - Φ

     = 40 ~60eV

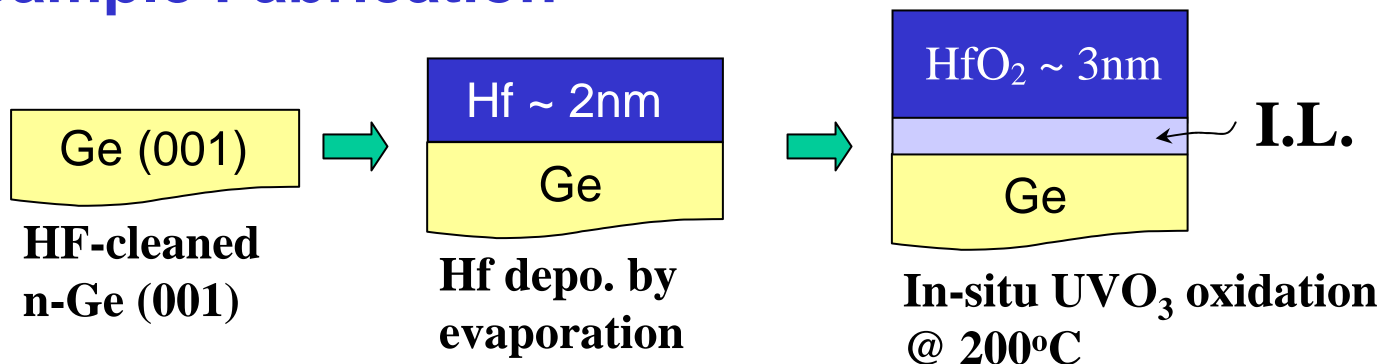
Mean escape depth = ~5Å

(Very surface sensitive)



Sample Structure & Depth Profiling by HF-etching

1. Sample Fabrication



2. Depth Profiling Procedures

hv

e⁻

Signal

λ

$I \sim \exp(-z/\lambda)$

z

HfO₂

Ge

2% HF-etching

(E/R = ~2Å/sec)

Inelastic Mean Free Path: λ ~5Å

➔ 63% photoelectron from 5Å

SR-PES with HF-etching times

$h\upsilon = 80eV$

Ge *3d* (sub.)

Ge *3d* (I.L.)

HfO_2 (Hf *4f*)

VB

17 sec

15 sec

13 sec

8 sec

as-dep

Intensity normalized by I_o (Arb.)

10 20 30 40 50 60 70 80

Electron Kinetic Energy (eV)

Ge

pure GeO_x

Ge

Ge

HF-etching time

hv e^-

HfO_2

I.L.

Ge

Chemical Bonding of I.L. (Ge *3d* core level)

$Ge^{1+,2+,3+}$

Ge^{0}

GeO_x

Ge

Ge^{0} $3d_{5/2}$

Ge^{0} $3d_{3/2}$

Ge^{1+} Ge^{4+} Ge^{2+} Ge^{3+}

No HfO_2

17s

15s

13s

8s

as-dep

HfO_2 exists

1.1eV

1.8eV

2.6eV

3.4eV

39 40 41 42 43 44 45 46 47

K.E. (eV)

No Ge^{4+} feature associated with stoichiometric GeO_2.

→ Re-oxidation of Ge substrate following upper Hf metal oxidation leads to a very non-stoichiometric GeO_x layer at HfO_2/Ge interface

VB Offset Determination from VB spectrum

n-Ge (001)

HfO_2

$h\nu$

e^-

Spectrometer

CBM (Ge)

$E_{g,\,Ge}$

VBM (Ge)

CBM (HfO_2)

$E_{g,\,HfO2}$

VBM (HfO_2)

Valence band

Hf *4f*

Ge *3d*

electrons

$E_{kinetic}$

E_F

VBM (Ge)

VBM (HfO_2)

VB

Hf *4f*

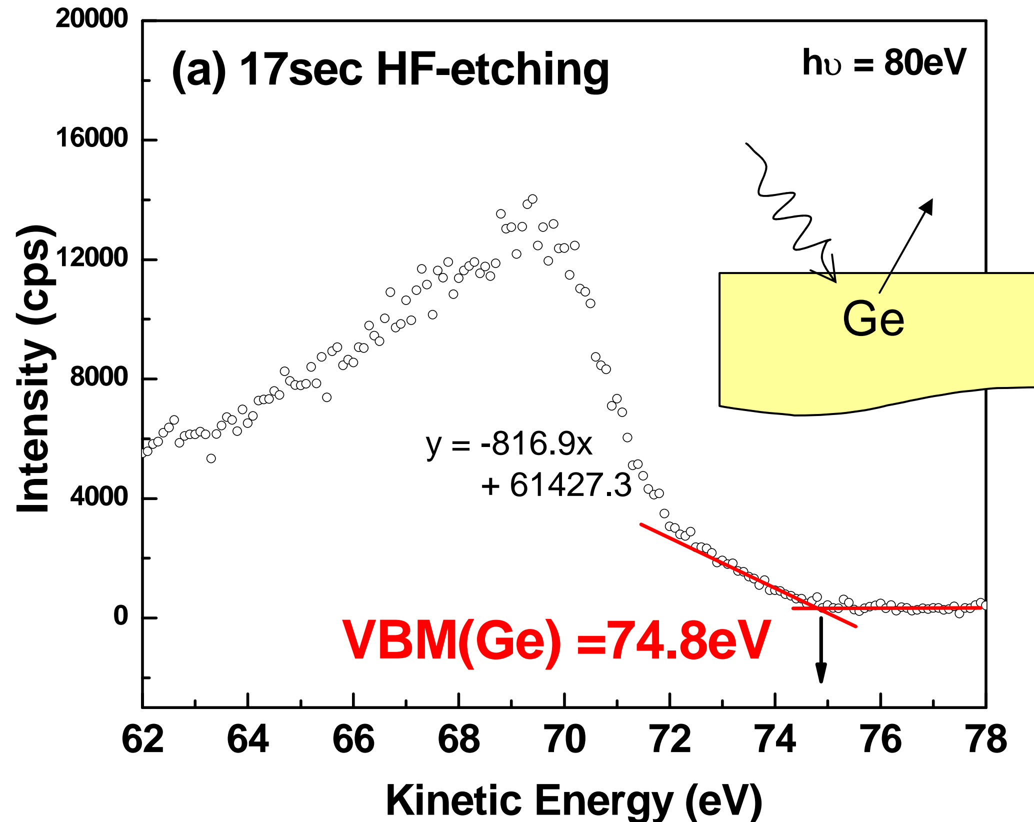
Ge *3d*

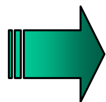
Intensity

VB Spectrum

➔ ΔE_v (Ge-HfO_2)

VB from Ge (100) (17sec HF-etching)



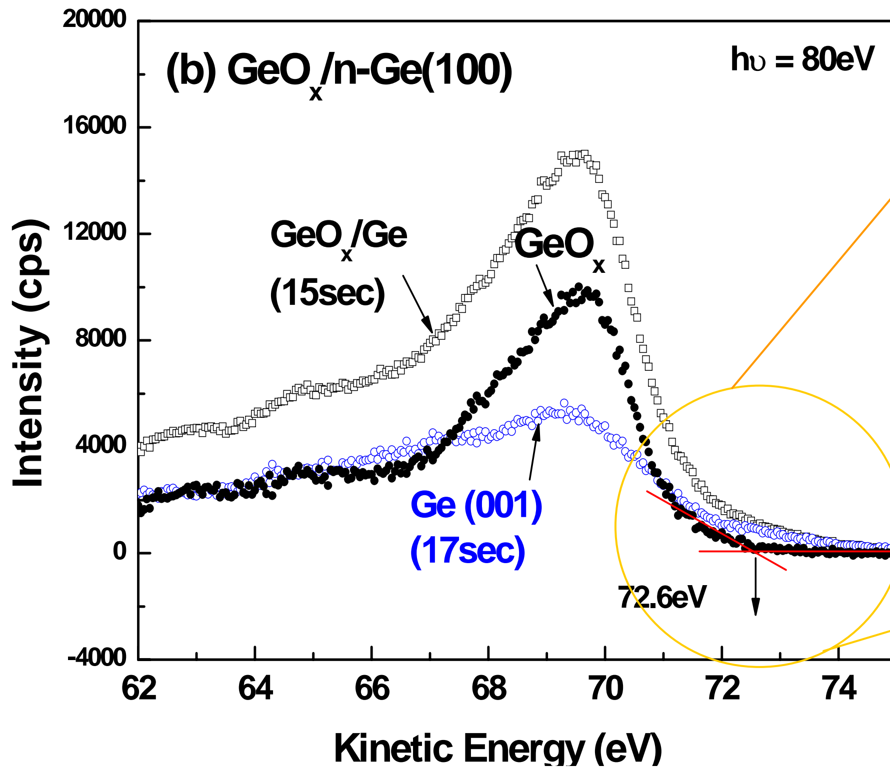


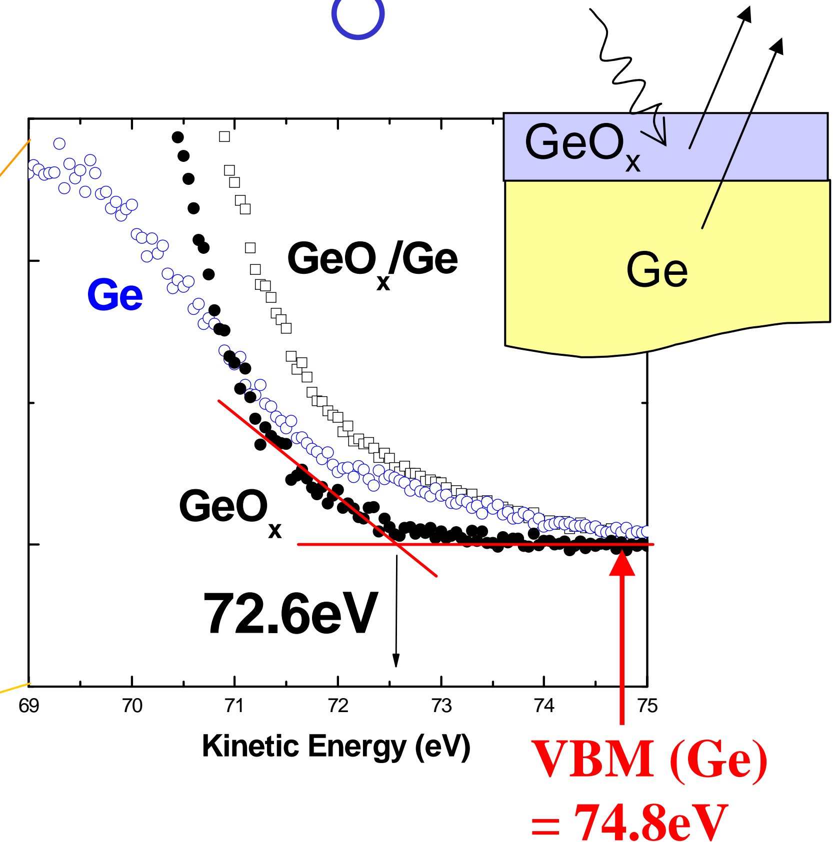
Valence Band Maxima (VBM) of Ge(001) is determined by "Best straight line fitting method"

➔ VBM (Ge(001))= 74.8eV

VB from GeO_x / n-Ge (100) (15sec HF-etching)

VB (GeO_x) = VB(GeO_x/Ge) – (attenuation factor)•VB(Ge)



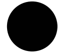


VBM (Ge) = 74.8eV

➡ VBM (GeO_x) = 72.6eV ➔ ΔE_v (Ge-GeO_x) = 2.2eV

VB from HfO_2 / GeO_x / Ge (8sec HF-etching)

$$VB(HfO_2) = VB(HfO_2/GeO_x/Ge) - (attenuation) \cdot VB(GeO_x/Ge)$$



(c) HfO_2 /GeO_x / n-Ge(100)

hυ = 80eV

Intensity (cps)

32000, 24000, 16000, 8000, 0

HfO_2/GeO_x/Ge (8sec)

HfO_2

GeO_x/Ge (15sec)

72.1eV

62, 64, 66, 68, 70, 72, 74

Kinetic Energy (eV)

HfO_2

GeO_x

Ge

HfO_2/GeO_x/Ge

HfO_2

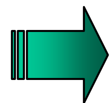
GeO_x/Ge

72.1eV

69, 70, 71, 72, 73, 74, 75

Kinetic Energy (eV)

VBM (Ge) = 74.8eV



VBM (HfO_2) = 72.6eV ➔ ΔE_v (Ge-HfO_2) = 2.7eV

Band Alignment of HfO_2/I.L.(GeO_x)/Ge(100) System

Ge(001) GeO_x HfO_2

E_c

Calculated → ΔE_C = 1.8~2.6eV

E_c

0.66eV

?

5.2~6.0eV [from 1,2,3]

E_v

This work — ΔE_V = ~2.7eV

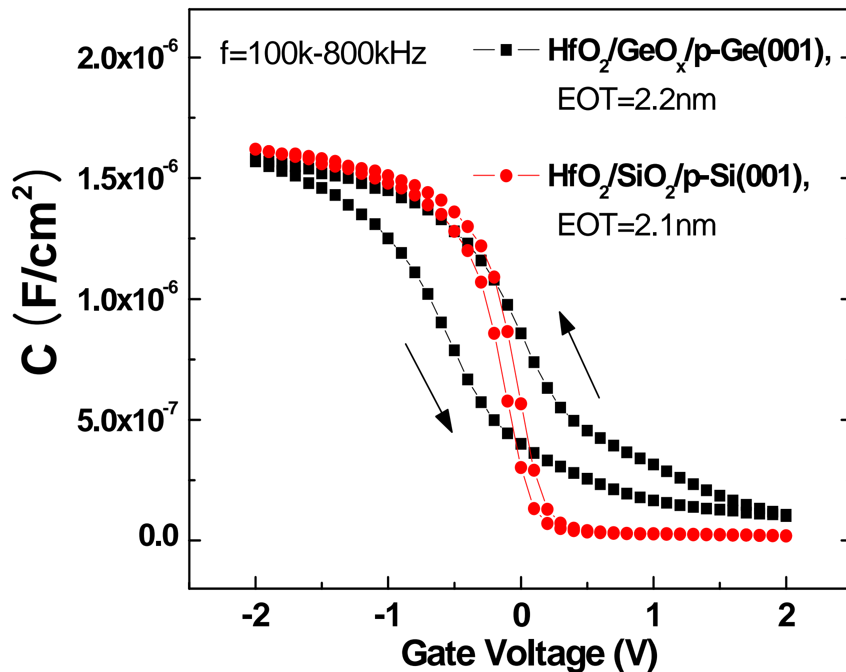
~2.2eV

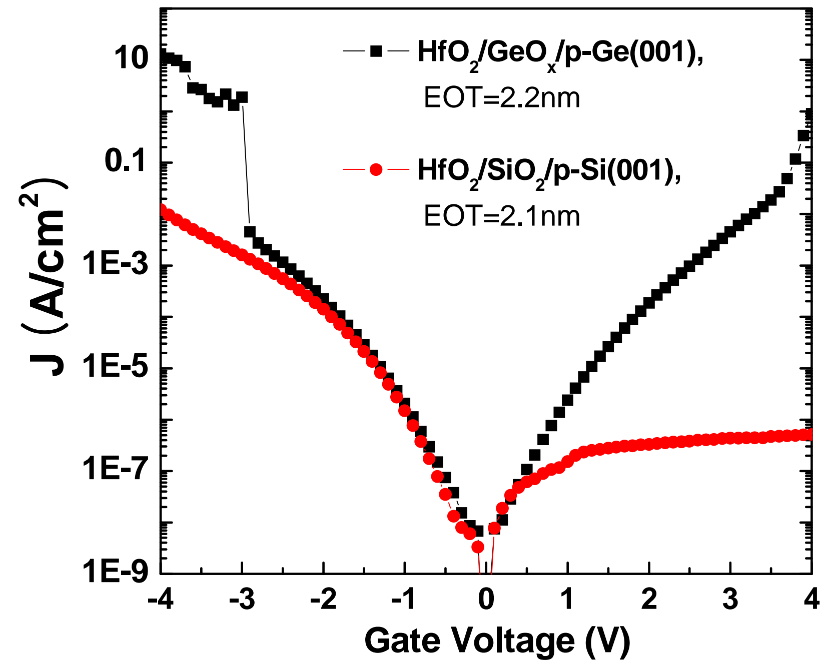
E_v

1 M. Oshima,et. al., Appl. Phys. Lett. **83**, 2172 (2003)
2 J. Robertson, J. Vac. Sci. Tech. B, **18**, 1785, (2000)
3 V. V. Afannas'ev, et. al., Appl. Phys. Lett. **81**, 1053 (2002)

ΔE_v and ΔE_c at HfO_2/Ge(001) is comparable to those of HfO_2/Si(001) → Promising in terms of leakage current

C-V & J-V of $Pt/HfO_2/GeO_x/p\text{-}Ge(100)$ MOSCAP





- **Huge charge trapping (hysterisys) and interface states (curve stretched out) due to poor GeO_x →Need Ge passivation layer (GeON ?)**
- **Gate leakage current is comparable to HfO_2 on Si as expected in band alignment results**

Conclusions

✓**High-k(ZrO_2) /I.L / Si(001)** : Demonstrate formation of a Zr-silicate interfacial layer between ZrO_2 and Si substrate can be controlled by the solid state reaction between Zr and an underlying SiO_2/Si substrate through *in-situ* vacuum anneals → excellent dielectric characteristics, such as negligible capacitance-voltage hysteresis (~ 10mV), lower fixed charge density, and reduced equivalent oxide thickness (~4Å) compared to un-annealed samples.

✓**High-k (HfO_2) /I.L / Ge(001)** : By analyzing Ge *3d* core levels systematically, we found that a very thin non-stoichiometric chemical nature exists at the HfO_2/Ge interface. From the VB spectra, the VB offset between Ge(001) and HfO_2, ΔE_v (Ge-HfO_2) = ~2.7 eV and resulting CB offset, ΔE_c (Ge-HfO_2) = 1.8~2.6 eV. → Need better surface passivation layer, but promising in terms of gate leakage current

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