# A Method to Grow Heteroepitaxial-Ge on Si: Multiple Hydrogen Annealing for Heteroepitaxy *(MHAH)**


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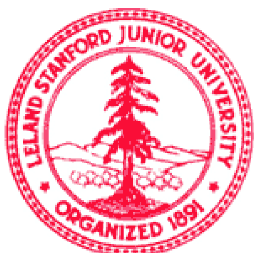



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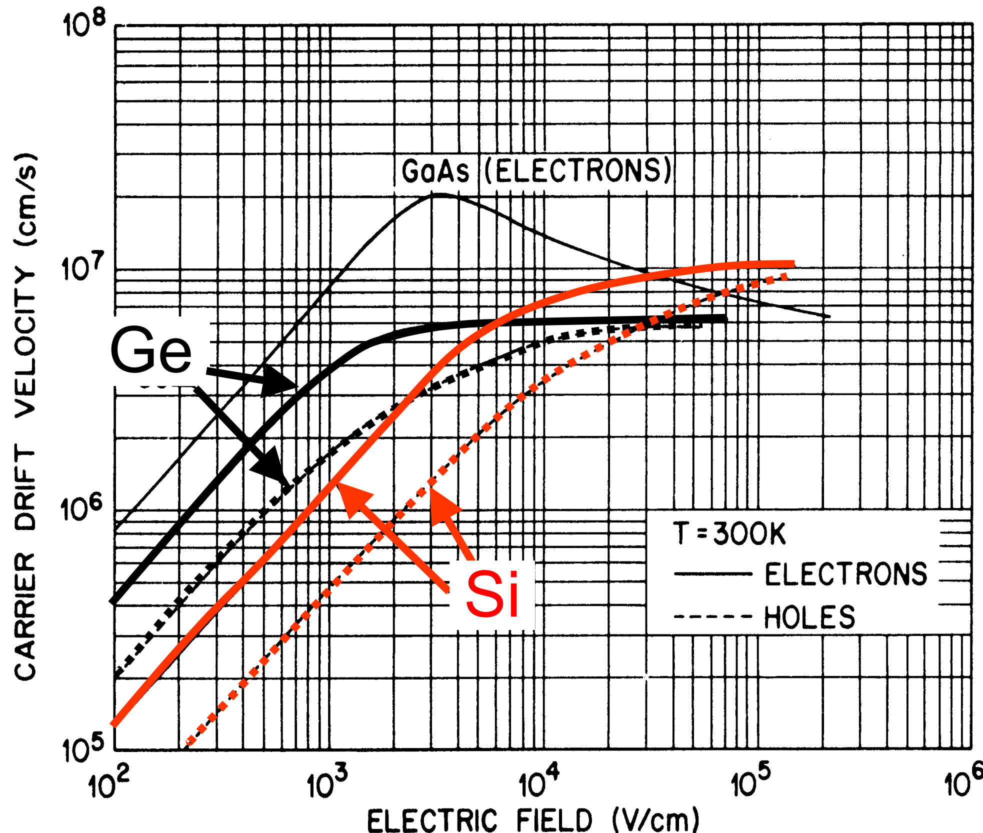
***Center for Integrated Systems (CIS), FMA Program: Canon***

# Why Germanium MOS Transistors?

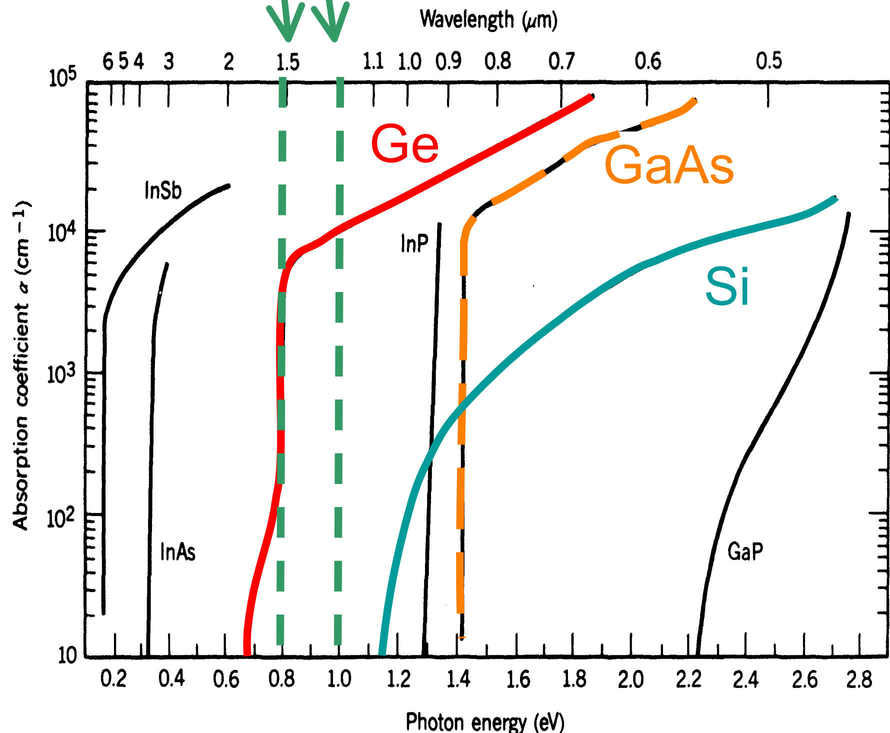
- More symmetric and higher carrier mobilities (low-field)
  - $\Rightarrow$ More efficient source injection
  - $\Rightarrow \downarrow$ CMOS gate delay
- Smaller energy bandgap
  - $\Rightarrow$ Survives $V_{DD}$ scaling
  - $\Rightarrow \downarrow R$ with $\downarrow$ barrier height
- Lower temperature processing
  - $\Rightarrow$ 3-D compatible
- Lattice match with GaAs
  - $\Rightarrow$ GaAs/Ge integration




S. Sze, *Phys. of Semicond. Devs.*

# Ge – A Prospective Optical Material

- Ease of integration with Si
- Smaller optical bandgap ideal for 1.3-1.5 μm wavelength
- High carrier mobilities
  ⇒ Short detector transit time




(Stillman *et al.*, *IEEE TED*, 31, p.1643, 1984)

# Problems With Ge

## Problems #1: Ge Surface Passivation

- The native oxide passivation on Ge surface is not stable enough either during fabrication or in the end-product

## Solution:

- **Oxynitride: Stable**
- **High-κ** dielectrics are deposited on Si, why not on Ge?

## Problem #2: Ge Wafers as a Substrate?

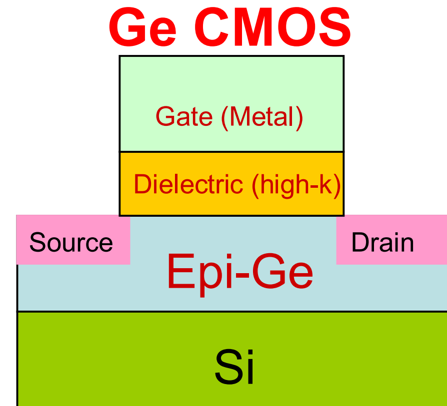
- Ge substrate not easy to handle and not easily available
- Expensive and Low Quality
- Si will continue to be the main substrate due to its overall excellent properties

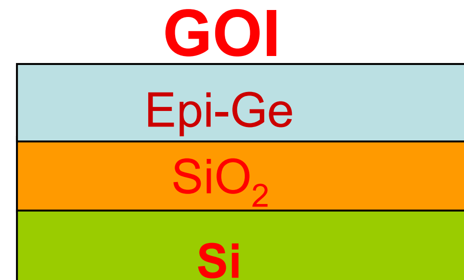
## Solution:

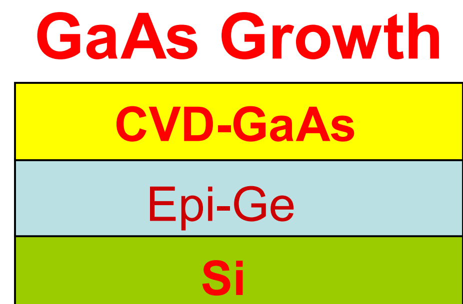
- Heterogeneous integration of Ge on Si.

# Applications heteroepitaxial-Ge?

- ***Ge CMOS***
  - Higher Mobility for High Performance
  - Low Temperature Processing for 3D applications
- ***Germanium on Insulator (GOI)***
  - Alleviate high junction leakage
  - Higher Performance
- ***Ge Photodetector (MSM)***
  - Optical Interconnects
- ***Integration of Ge/Si/GaAs***
  - CMOS: Ge pMOS and Si nMOS
  - GaAs Growth on Ge for Laser's and LED's
- ***GaAs CMOS***
  - Very High Mobility
- ***Nanotechnology:***
  - ***Ge nano-wire growth***
  - ***Ge nano-particle fabrication***

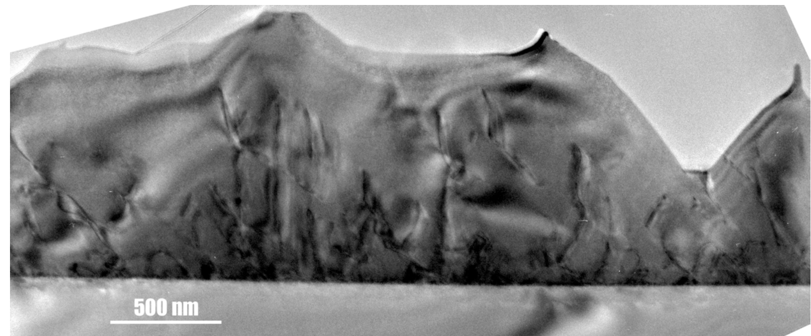




# Challenges to Ge/Si heteroepitxay

- **4% Lattice Mismatch**
  - **MISFIT/Threading Dislocations**
  - **Islanding Morphology**
- **There exists a Critical Thickness($t_c$)**
  - **For 100% Ge on Si: between 4-10nm***




As Grown CVD Ge on Si (at 400 °C)

***The Challenge: Thick Ge Layers on Si with low threading dislocations and reduced surface roughness***

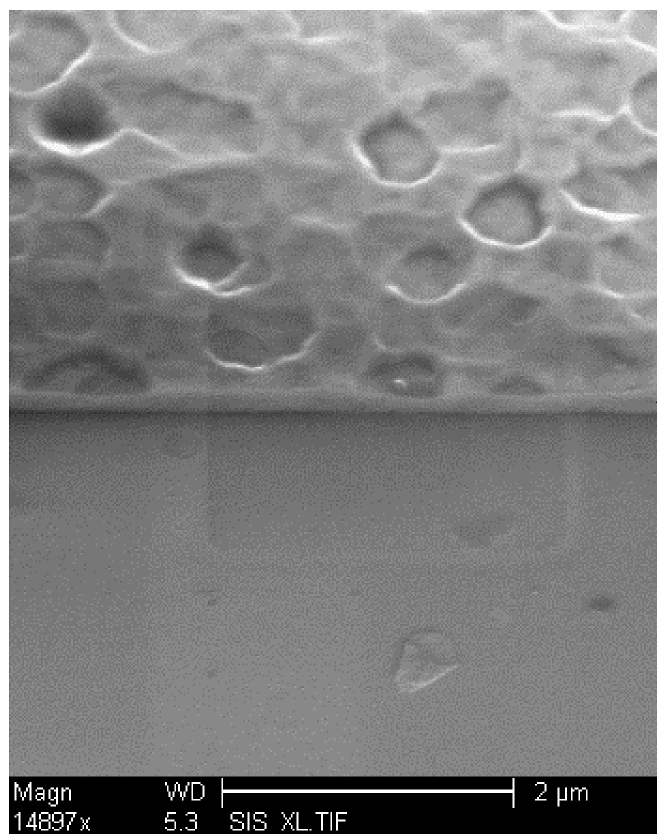
# Surface Roughness: **Hydrogen Annealing**

- Hydrogen Annealing Summary
  - Si-H-> Reduced Si Diffusion Barrier
  - Enhanced Surface Mobility
  - Surface Roughness Reduced
    - N. Sato and T. Yonehara, Appl. Phys. Lett. **65**, 1924 (1994)
    - J. Nara, T. Sazaki, and T Ohno, *Phys. Lett. **79***, 4421 (1997)
- Ge-H Bond attempted
  - In-Situ Hydrogen Anneal After Epi-Growth.

# Experiment #1

- Germanium Growth
  - ASM Epitaxial Reactor at Stanford Nanofabrication Facility (SNF)
  - $H_2$ pre-bake 2-min 950°C
  - Deposition -> Temp = 400°C
  - Germane: Pressure: 10 Torr
  - Time: 15 min
  - 200nm Ge on Si
- Hydrogen Anneal
  - No anneal, 600°C, 700°C,763°C,800°C,825°C
  - 1 hr 80 Torr $H_2$

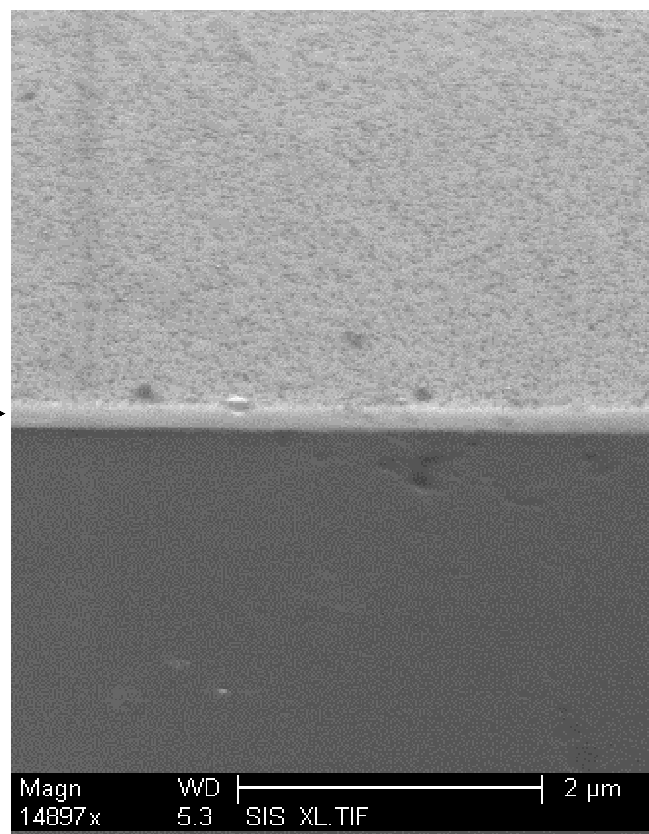
# Scanning Electron Microscopy (SEM)




Ge surface

Ge Cross section

Si substrate




**NO ANNEAL**

**$R_{rms}$: 24.964 nm**

**825°C *Hydrogen* Anneal**

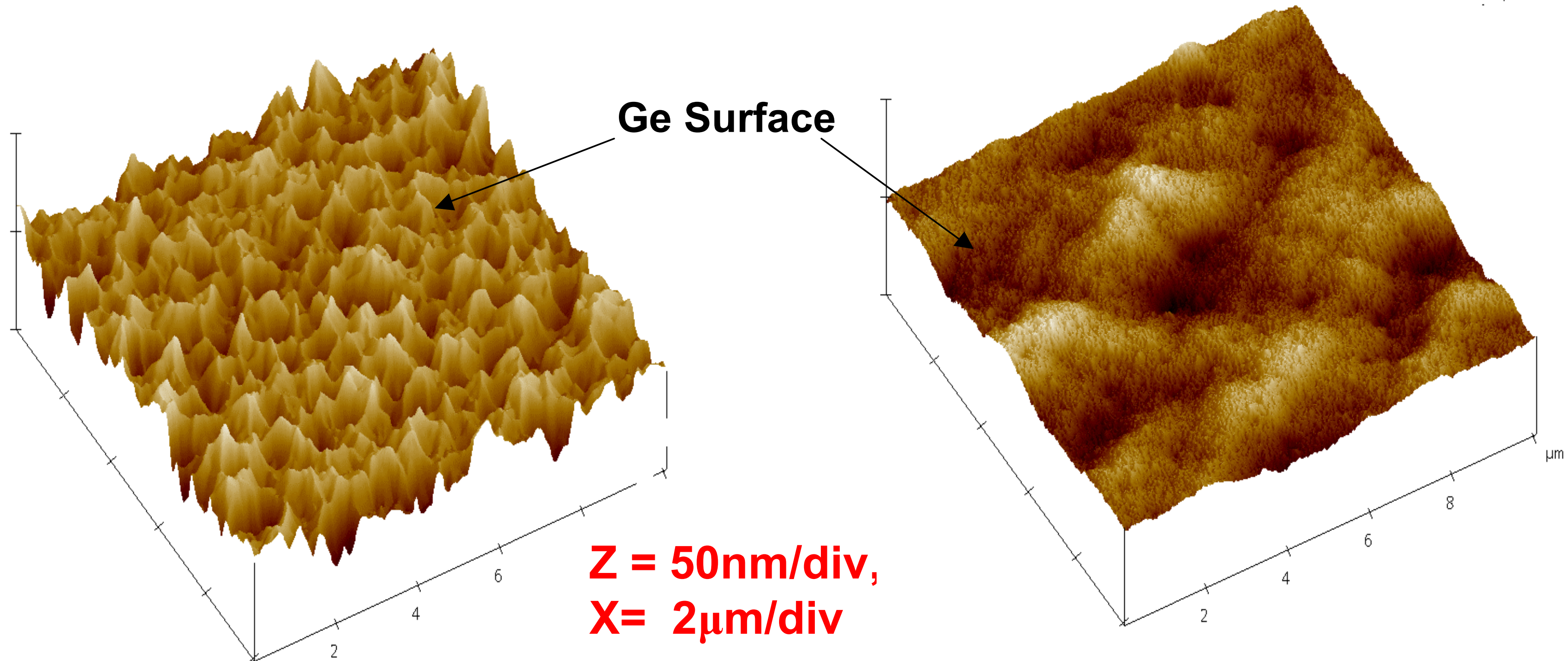
**$R_{rms}$ :2.5nm**

200nm epi-Ge on Si: CVD growth at 400**°C**

45° **Cross Sectional Cut showing Surface Roughness Reduction**

Nayfeh et al, ***APL*** *October 4th* ***85*** 14

# TOPOGRAPHICAL ATOMIC FORCE MICROSCOPY (AFM)

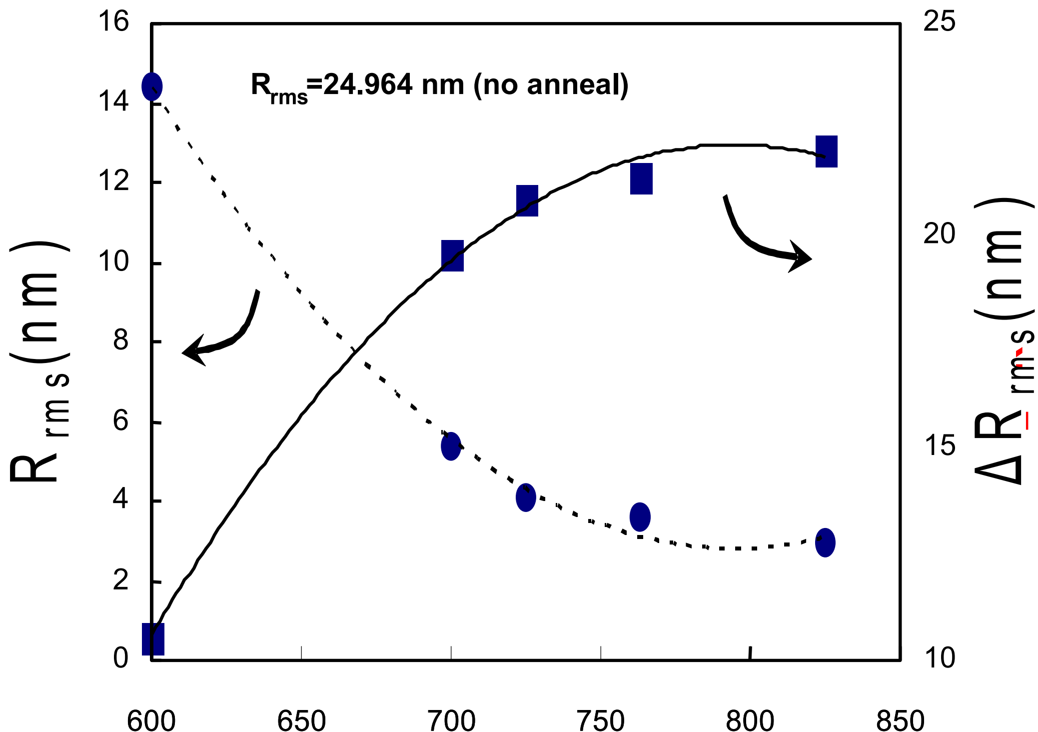


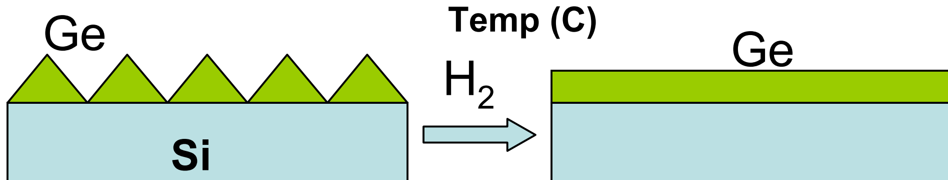

**NO ANNEAL**
**AS GROWN**
**$R_{rms}$ : 24.964 nm**

**825°C *Hydrogen* Anneal**
**$R_{rms}$ :2.5nm**

Nayfeh et al, ***APL*** *October 4th* ***85*** 14

# Ge-H Bond: Reduction in Diffusion Barrier




Reduction in Diffusion barrier, Mobile Ge-H driven by reduced Surface energy

- Ge-H -> barrier for direct path surface diffusion is reduced thus increasing the surface mobility of Ge; Hydrogen remove any surface oxide

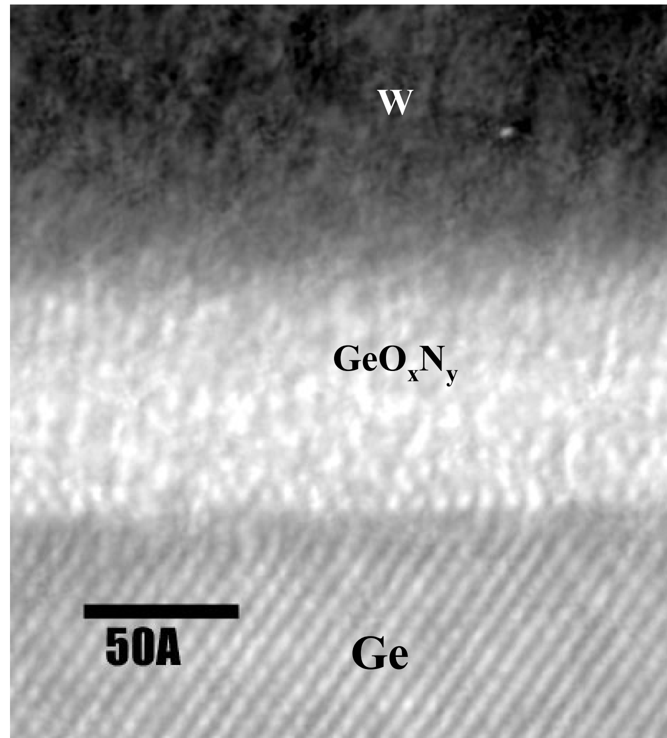
- There appears to be an upper limit to the amount of diffusion barrier reduction.

- ***800°C -> 92 meV reduction in diffusion barrier (~kt/q)***

*Nayfeh et al, **APL** October 4th **85** 14*

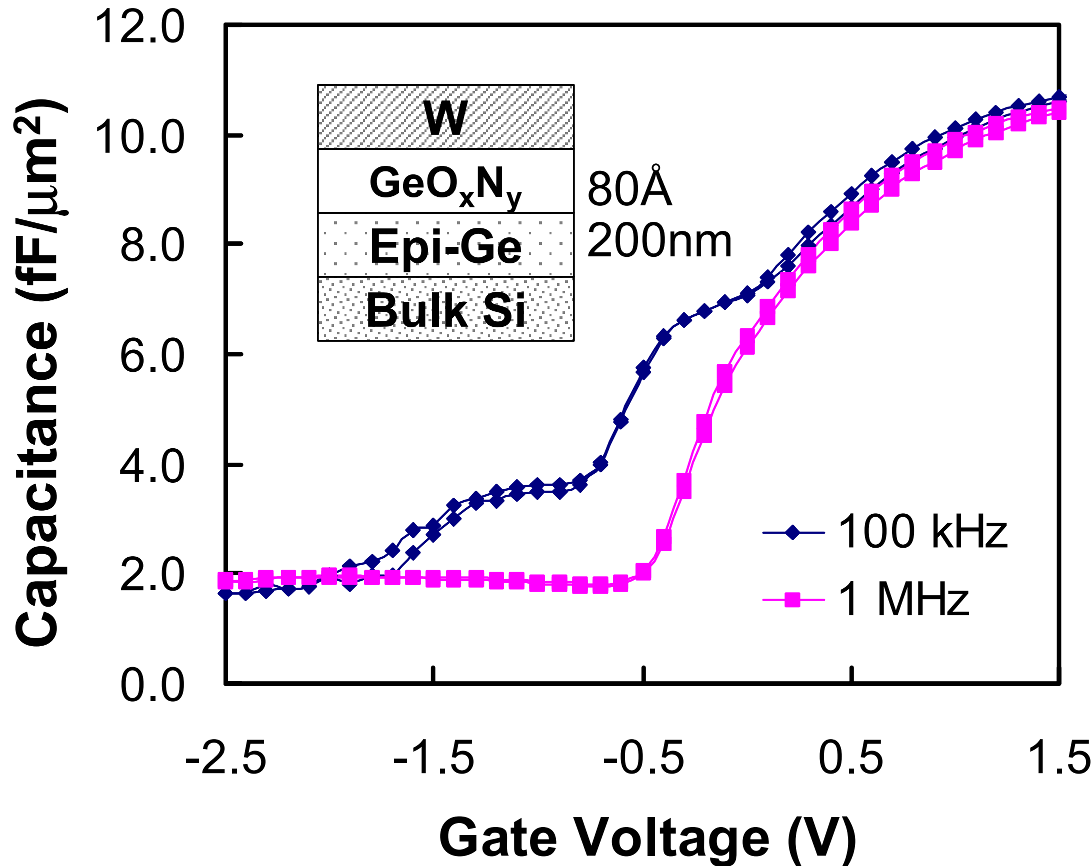
***90% reduction of $R_{rms}$ by hydrogen annealing***

# Epi-Ge MOS CAP




***High Resolution Cross Sectional TEM of Ge/GeOxNy/W stack showing the Ge Single Crystal Lattice with Interface.***

# Electrical Characteristics




- MOS Capacitors were fabricated on smoother Ge surface
- GeOxNy as the gate dielectric with tungsten gate electrode over Ge epi-layer annealed in hydrogen at 825°C.
- From the 100 kHz sweep, two kinks are observed near inversion:  Thin Epi-Ge Layer 200nm, defect region interaction.

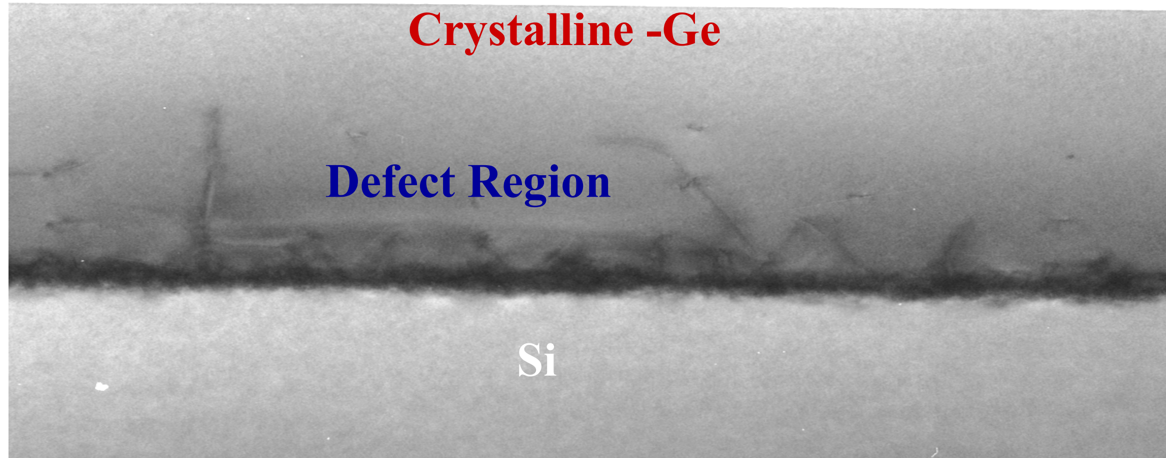
**Bi-directional high frequency CV characteristics measured at 100 kHz and 1 MHz showing negligible hysteresis**

Nayfeh et al, ***APL*** *October 4th* ***85*** 14

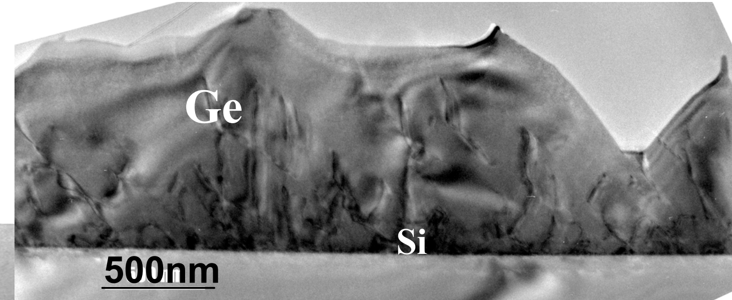
# Experiment #2

- Motivation
  - Grow another layer of Ge-> Hydrogen Bake and ->View by TEM
- 2st growth
  - Same Growth Conditions as before
  - Use lowest $R_{rms}$ Ge wafer
- 2nd Hydrogen Anneal
  - 1 hr 80 Torr 700°C

# Threading Dislocations




Cross Sectional TEM of Heteroepitaxial-Ge on Si using in-situ multiple growth and hydrogen annealing process (MHAH Method)

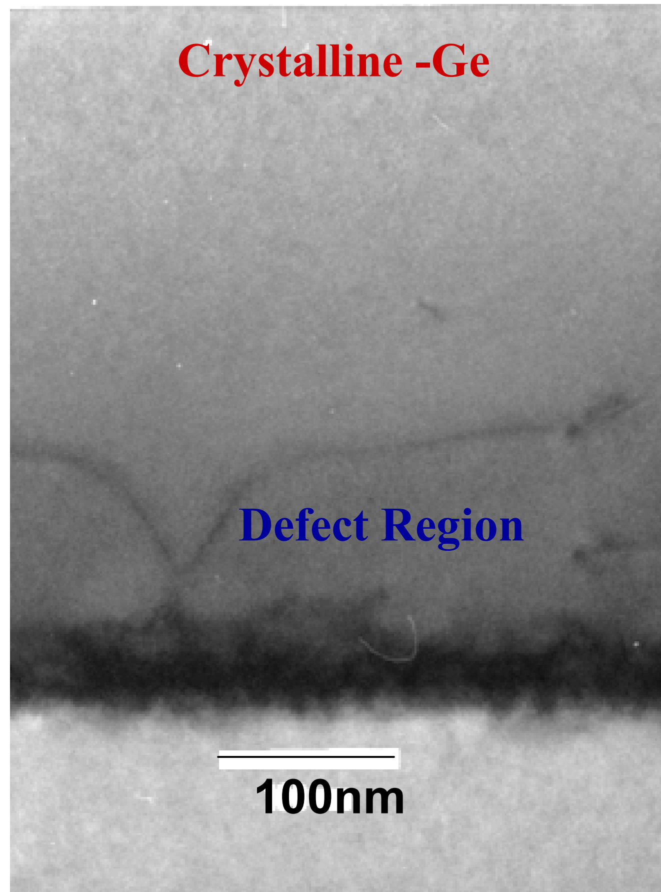



As Grown CVD Ge on Si (at 400 °C and 10 Torr).

**Threading Dislocations are confined to the Si/Ge interface**

Nayfeh et al, ***APL*** *Under Review*

# Misfit Dislocations Cont’d



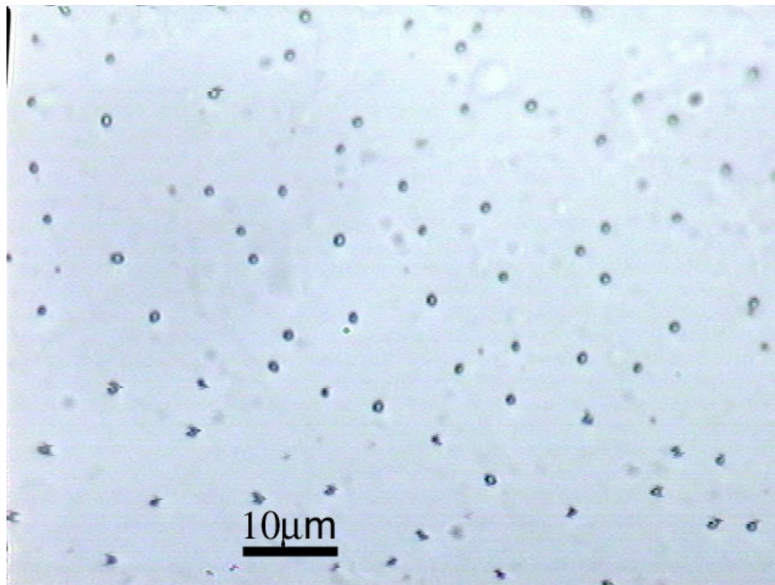

***Threading Dislocations bending parallel to the Si/Ge interface***

# Dislocation Density (Etch Pit Denstiy)

*Iodine Etch:*

*HF, $CH_3COOH$, $HNO_3$, $I_2$*

*EPD Etch on 4.5 μm epi Ge layer (100 x optical microscope)*



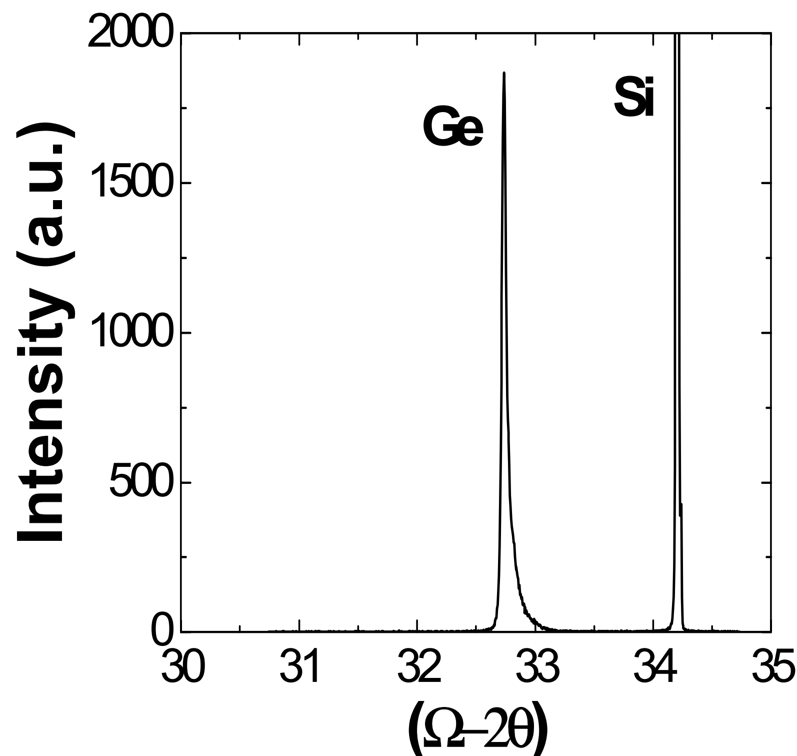

***Threading Dislocation Density Reduced to ~1 x $10^6$ $cm^{-2}$***

# Dislocation Road Map: Ge on Si

| Method | **Dislocation Density /cm$^2$** | Ref. |
|---|---|---|
| Ge on Si Thermal Annealing after growth | $9.5 \times 10^8 – 2.3 \times 10^7$ | Luan et all, APL, ***75***, 2909 |
| Si/Ge Grading | $2.1 \times 10^6$ | Currie et all, APL, ***72***, 1718 |
| Nano-Scale Ge Seeds (ELO) | $2 \times 10^6$ | Li et all, APL, ***85***, 1928 |
| ***MHAH: Multiple Hydrogen Annealing for Heteroepitaxy*** | $\mathbf{1 \times 10^6}$ | This work |

***MHAH method gives the lowest dislocation density published to date***

# MISFIT STRAIN RELIEF



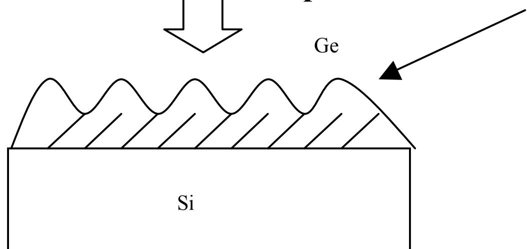

***X-ray Scattering intensity: Ge peak indicates epi-Ge is single crystal and fully-relaxed***

***Hydrogen Annealing relieves the MISFIT Strain Allowing for Homoepitaxial Growth***

# The 4 Roles Of Hydrogen Annealing

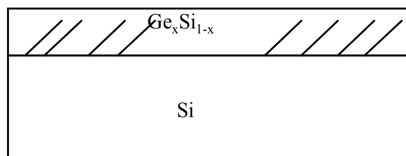
*Bulk Silicon Wafer*

1. **Epitaxial Growth of the 1st Germanium Layer**



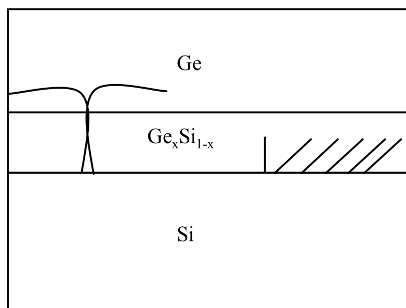

***Ge islanding and Misfit and Threading Dislocation formation***

2. **Hydrogen Anneal**



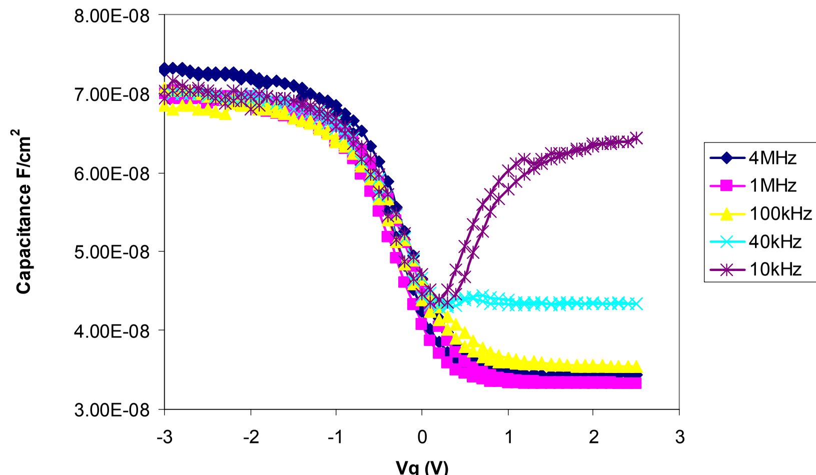

***Threading dislocations glide on inclined slip planes driven by lattice misfit and thermal expansion coefficient mismatch of Ge and Si. Si diffuses in to the Ge epi-layer. These processes relieve the misfit strain.. Hydrogen anneal avoids surface oxide formation. Surface roughness is reduced.***

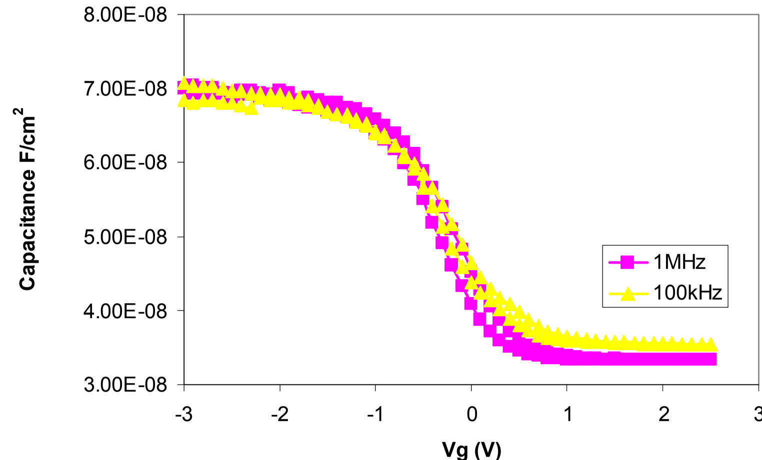
**3. Epitaxial Growth of the 2nd Germanium Layer**
**4. 2nd Hydrogen Anneal**

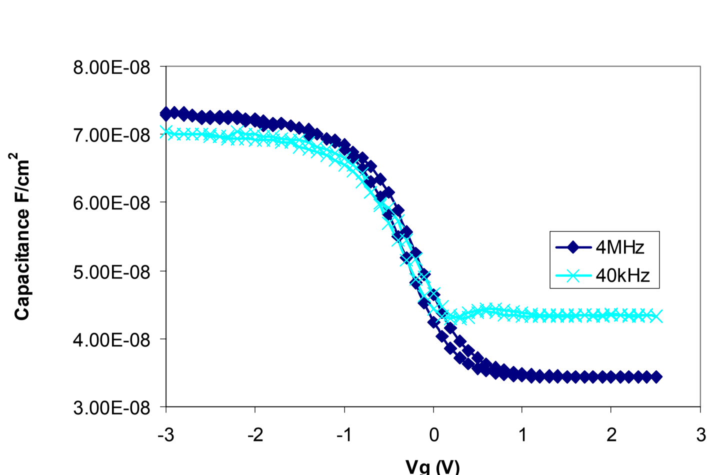


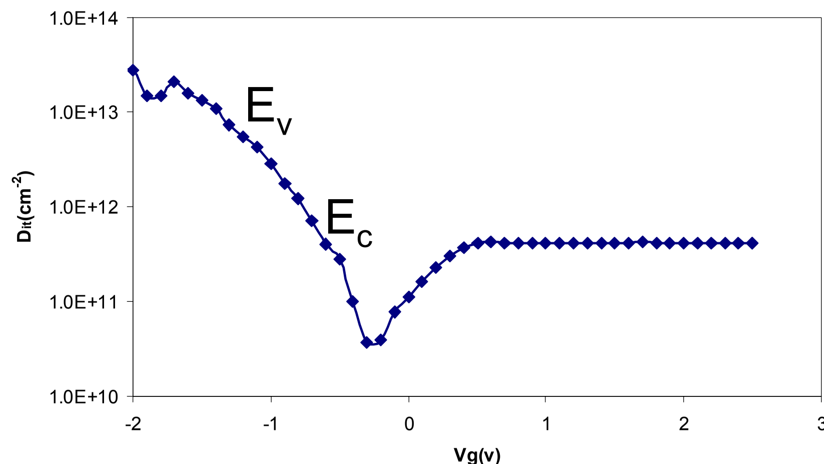

***Homoepitaxy of Ge on relaxed Ge. Defects Remain Near the Ge Si interface. Do not propagate to the surface. Hydrogen Annealing smoothens the final layer.***

# *MHAH* p-Ge MOSCAP



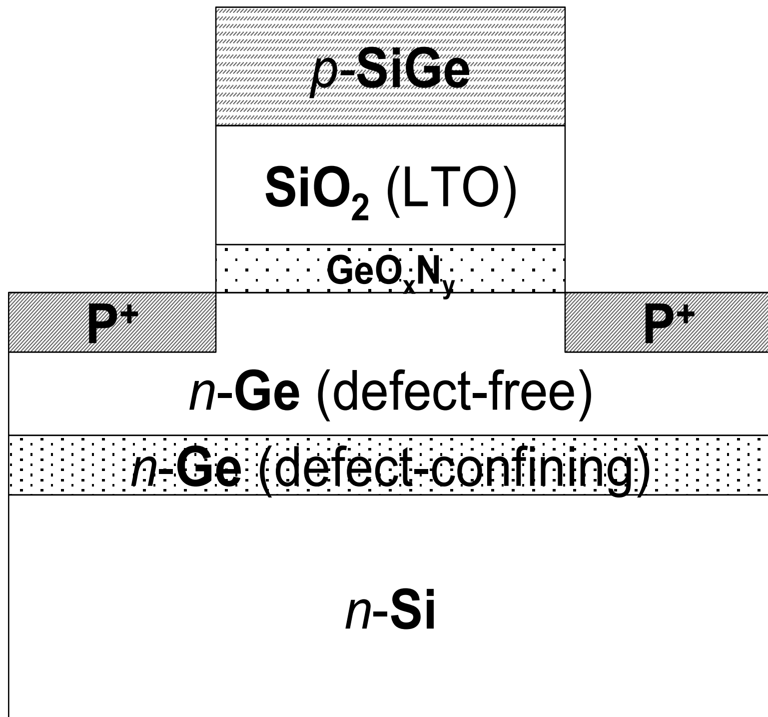



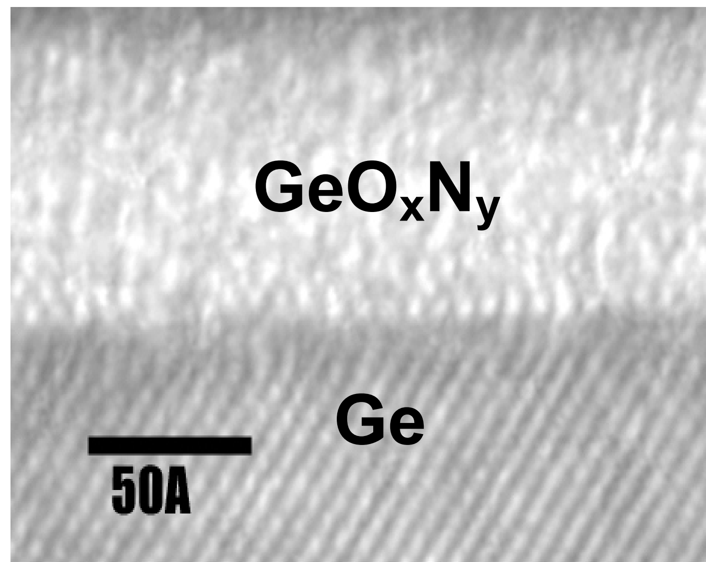




1.5 μm *MHAH* p-Ge: **$GeO_xN_y$ with W gate electrode**

Low Hysteresis; Low $D_{it}$ in strong inversion <1e11 $cm^{-2}$

# PMOS Transistor



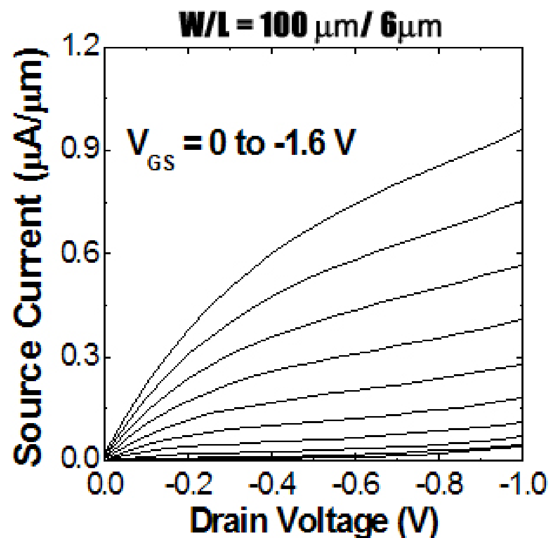



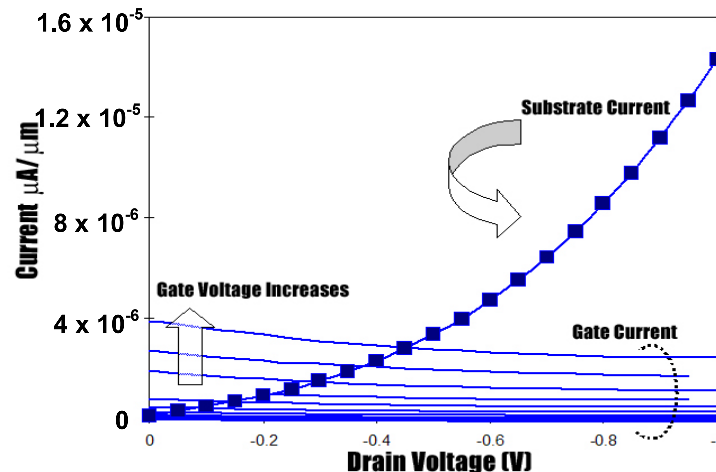

**Sub 500 °C process to fabricate epi-Ge pMOS transistor**

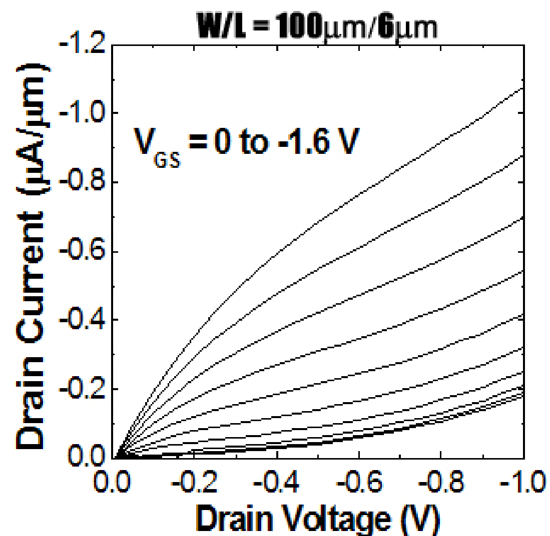
**No Si CAP or SiGe Graded Layer**

Nayfeh et al, ***EDL*** *May 2005 (to be published)*

# Electrical Results




Leakage At Drain Side (2 components)

1. Junction Leakage
2. 400nm Epi-Ge Layer: Electrostatic interaction between drain depletion region and defect region on thin Ge layer.

# Ge Mobility Extraction

## Mobility Derivation

$$\mu_{eff} = \left(\frac{2L}{W}\right) \times I_d \times \frac{1}{C_{ox}\left(V_g - V_t\right)}$$

Threshold voltage, $V_t$ was extracted to be 0.7 V from $I_d$-$V_g$ slope extrapolation. The $V_t$ shift on this p-MOS device is due to the p-type SiGe doped gate electrode

*Note: $Q_i$ is overestimated thus under estimating the mobility*

## Effective Field Derivation

From Gauss's law

$$E_{eff} = \frac{1}{\varepsilon_{Ge}}\left(\left|Q_d\right| + \frac{1}{3}\left|Q_i\right|\right)$$

$$\left|Q_d\right| = C_{ox}\left(V_t - V_{fb} - 2\psi_B\right) \quad \left|Q_i\right| = C_{ox}\left(V_g - V_t\right)$$

$\Psi_B$ is the separation of the fermi level from the midgap in the Ge, and $V_{fb}$ is the flat band voltage

$$\varepsilon_{Ge} \approx 4\varepsilon_{ox}$$

$$E_{eff} = \frac{V_t - V_{fb} - 2\psi_B}{4t_{ox}} + \frac{V_g - V_t}{12t_{ox}}$$

Nayfeh et al, ***EDL*** *May 2005 (to be published)*

# Mobility Enhancement

**Mobility Table**

| | $E_{eff}$ MV/cm | $\mu_{eff_Ge}$ $cm^2/V\text{-}sec$ | $\mu_{eff_Si}$ $cm^2/V\text{-}sec$ |
|---|---|---|---|
| **Vg-Vt = 80mV** | 0.138 | 250 | 125 |
| **Vg-Vt = 0.8V** | 0.213 | 95 | 31 |

**Mobility Enhancement: *2x* at Low field and *3x* at High field compared to Si pMOS Universal Mobility.**

# Epitaxial Nanowire Growth **on *MHAH* grown Ge (001)**

*Hemant Adhikari*, Ammar Nayfeh, Krishna C. Saraswat, and Paul McIntyre**

**Department of Materials Science and Engineering*

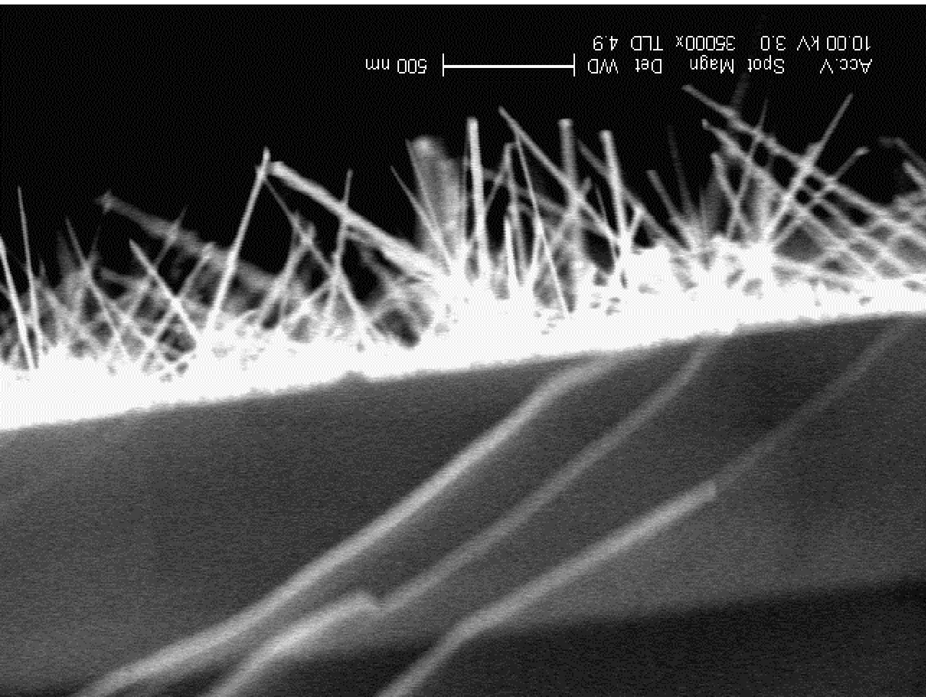
*Stanford University*

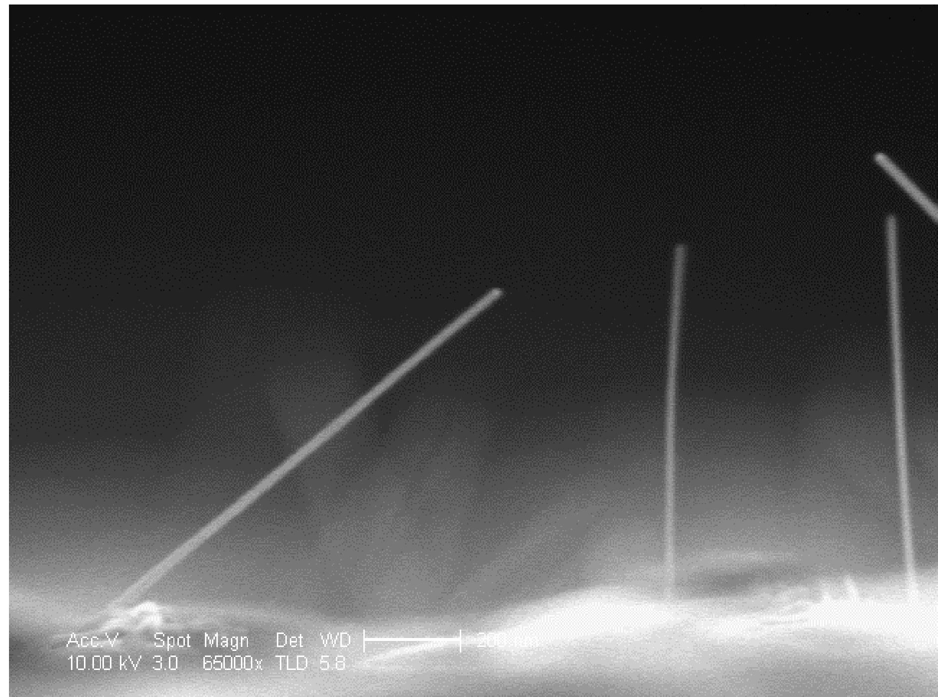
# GeNWs on epi-Ge on Si(001) substrate

Tc =$400^0$ C(2mins), $280^0$ C(28mins), $P_{tot}$= 30 torr, $GeH_4$= 5 sccm, $H_2$= 550 sccm, $p_{GeH4}$=0.273, t=30mins

Sample Prep: Spin APTES, **Dip** Au colloids 10nm dia

Epi-Ge on Si(001) (MHAH) from Ammar Nayfeh (Saraswat Group)




Observation: Wires grown from epi-Ge on Si(001) seem to be similar in growth orientation to the ones grown on Ge (001).



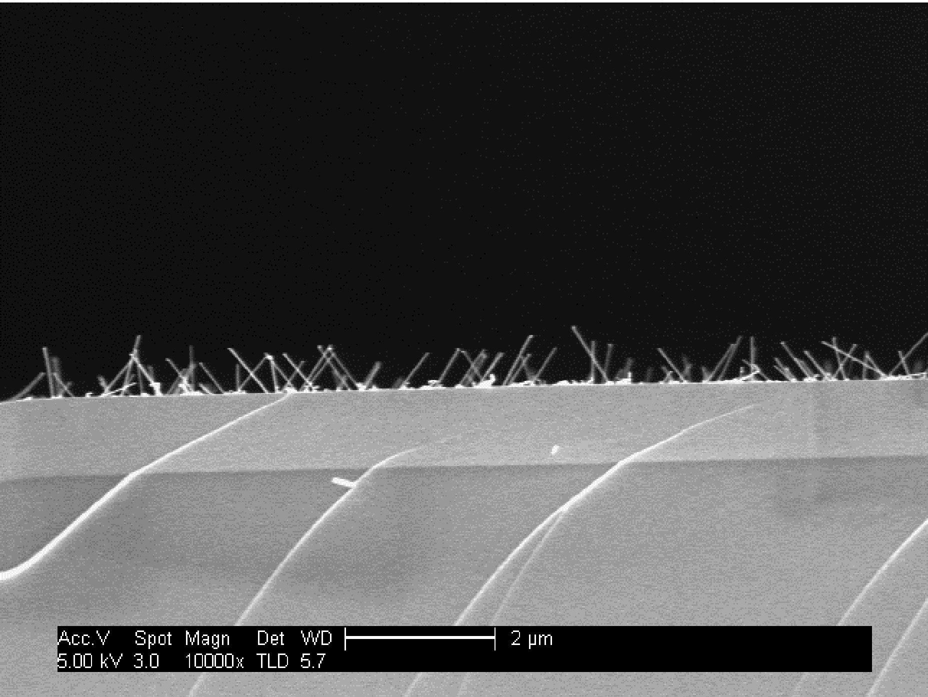
*hemant adhikari*

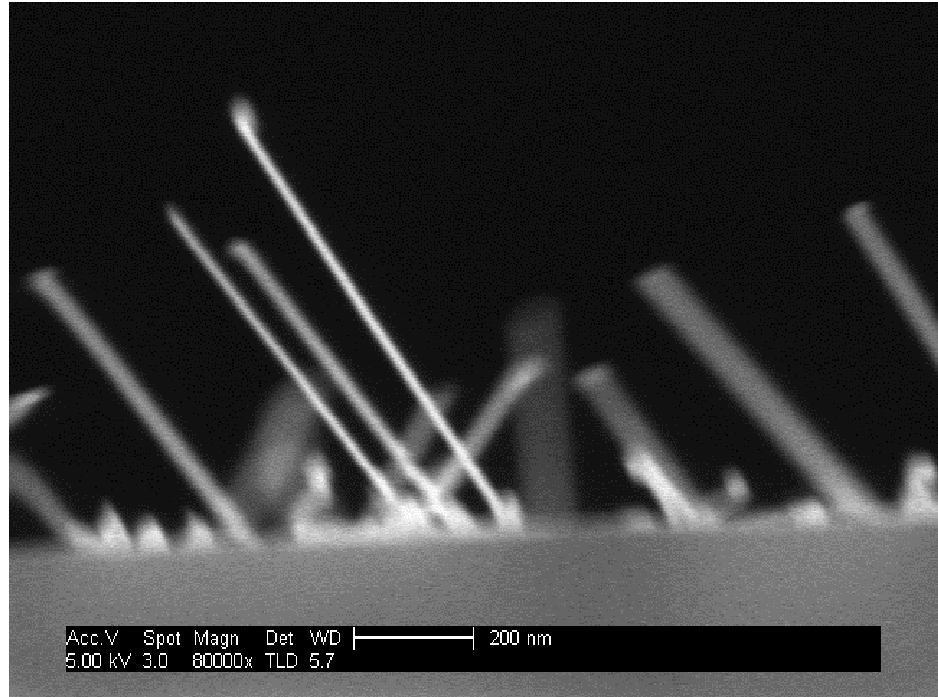
# GeNWs on epi-Ge on Si(001) substrate

Tc =400⁰ C(2mins), 280⁰ C(28mins), $P_{tot}$= 30 torr, $GeH_4$= 5 sccm, $H_2$= 550 sccm, $p_{GeH4}$=0.273, t=30mins

`Sample Prep: Spin APTES, ` **`spin`** ` Au colloids 10nm dia`

Observation: Most wires appear to be growing in ~60 deg from horizontal. Some wires are vertical. Almost none are at ~35 deg orientation from horiz.




Conclusion: Wires growing vertically are epitaxial to (001) orientation of substrate
Wires at 54.7 deg from horiz. are epitaxial to (112) plane of substrate.

# GOI Development Using ***MHAH*** Technology

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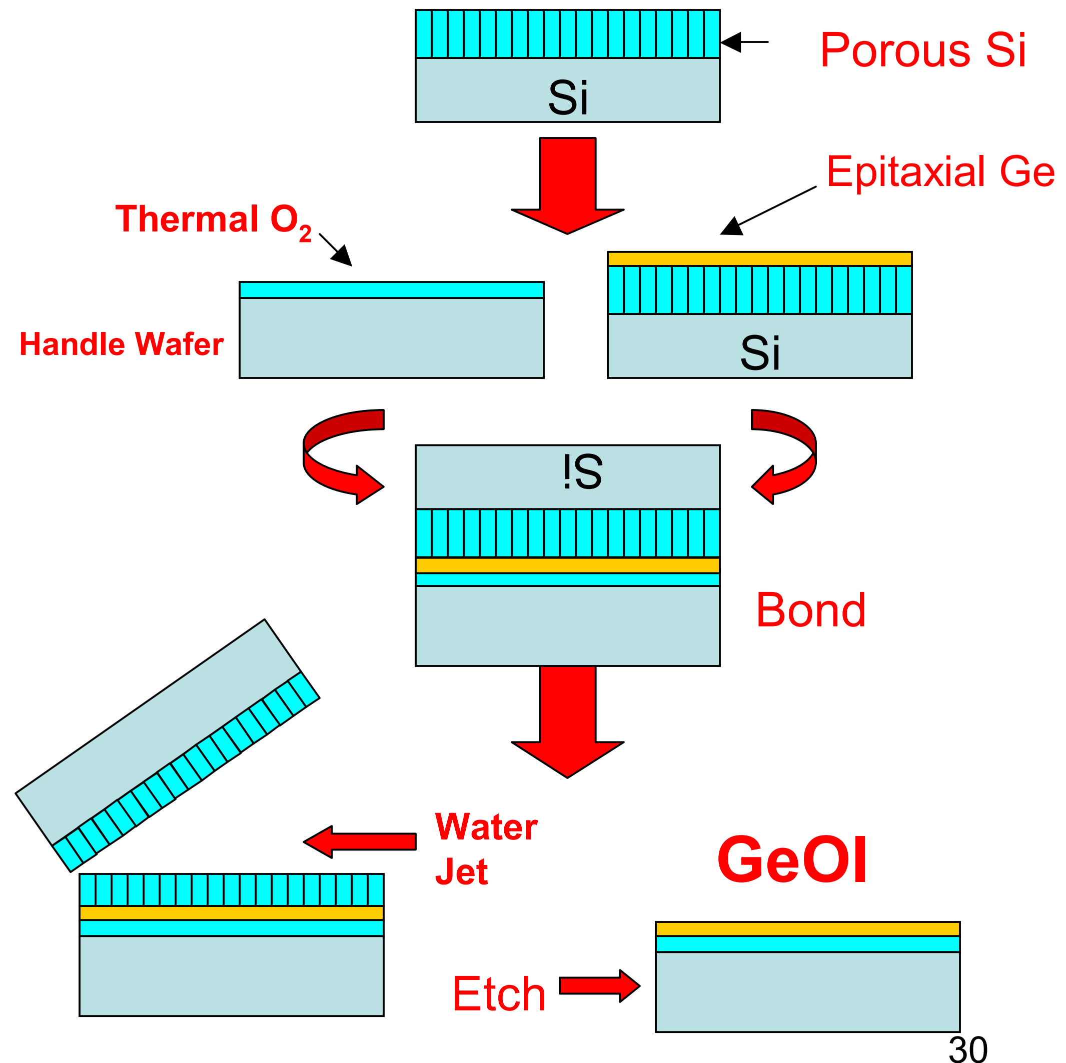
# GOI: Using MHAH Process (I)

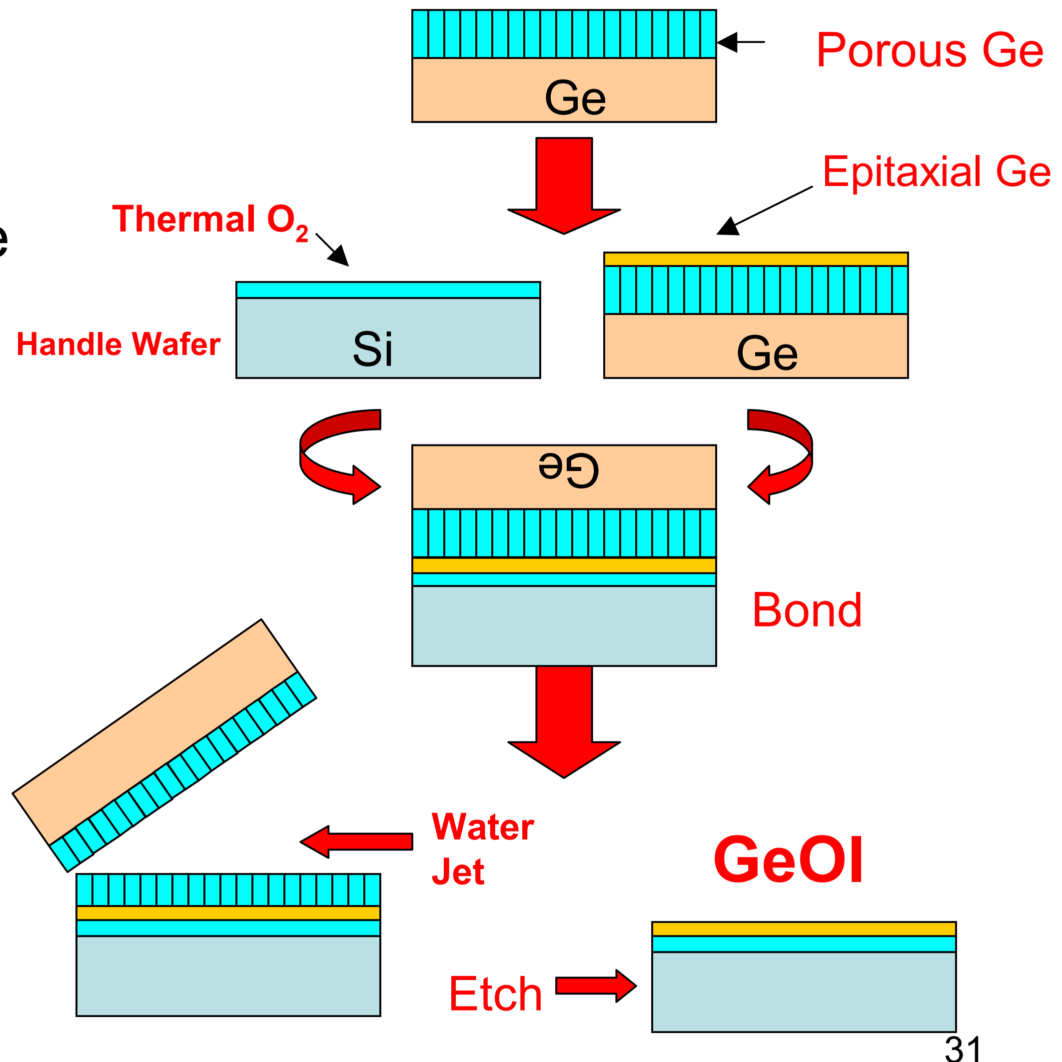
- Begin with Si Wafer, Anodize
- Grow Epi-Ge on Hydrogen Pre-Baked Porous Silicon Layer
- Grow Thermal Oxide on Si Handle Wafer
- Bond Handle Wafer to Epi Germanium Layer.
- Water Jet and Etch porous and defect region for GOI



# GOI: Using MHAH Process (II)

- Begin with *MHAH Ge* Wafer on Si
- Anodize Ge->Porous Ge
- Hydrogen Pre-bake/Epi Ge growth
- Bond Handle Wafer/Epi Germanium Layer.
- Water Jet and Etch

  Porous Si for GOI



# Summary

- Why Ge? Epi versus Bulk
- Challenges of heteroepitaxial-Ge
- ~90% Surface Roughness Reduction in epi-Ge layers on Si by in-situ Hydrogen Annealing
- epi-Ge based MOS capacitors with low hysteresis CV characteristics were fabricated
- Threading Dislocations are confined to the Si/Ge Interface or bend parallel to the interface
- Four roles of Hydrogen Annealing Understood: MISFIT Relief
- Defect Etch showed Ge layers with defect density of $1 \times 10^6$ $cm^{-2}$. The lowest published number to date.
- Epi-Ge pMOS transistors fabricated with high hole mobility
- Applications: Ge Nanowire, GOI fabrication using *MHAH* technology