Methodology for environmental impact evaluation with 2D v. 3D case study

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Outline

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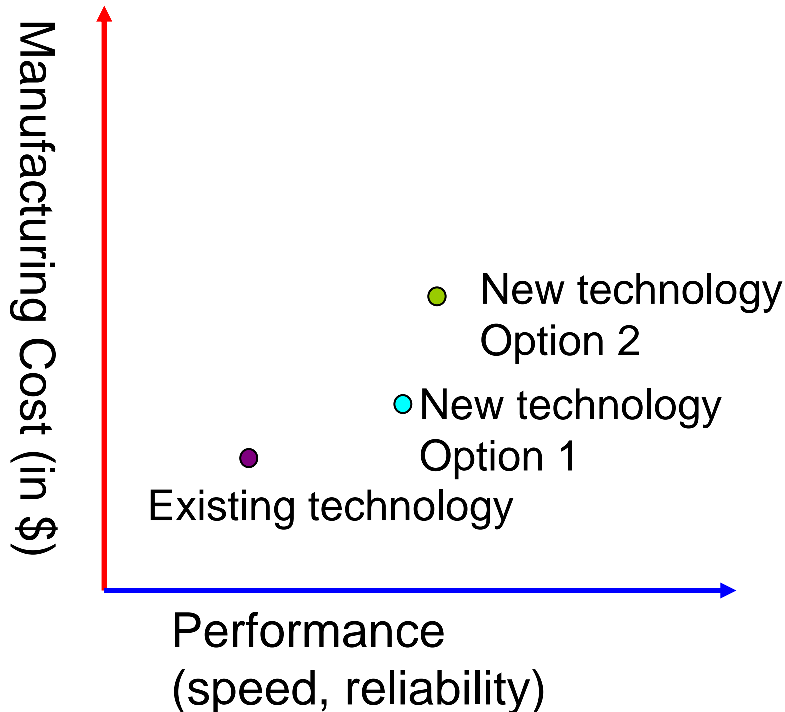
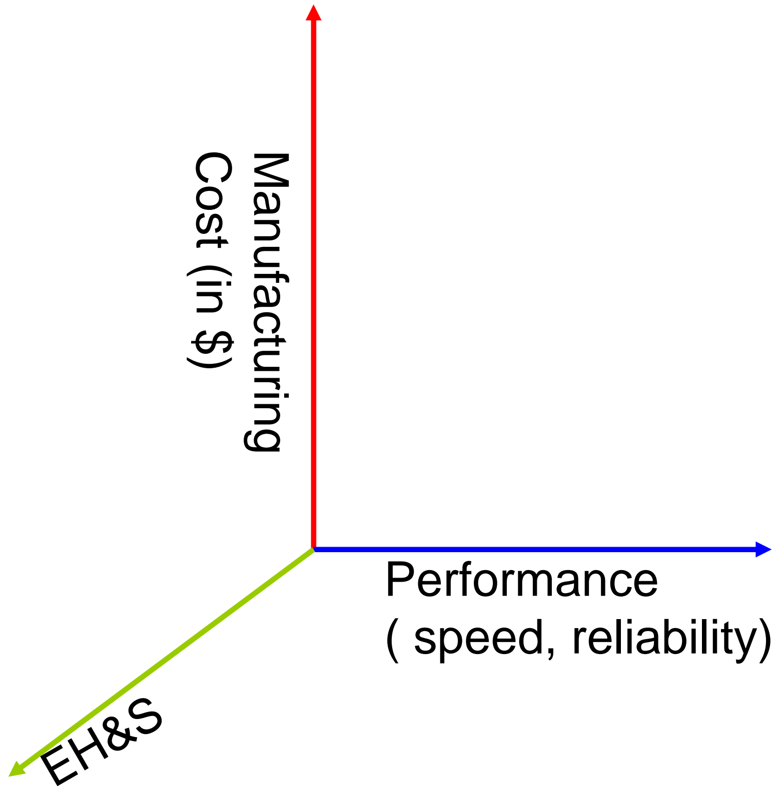
Motivation for Methodology



- Each semiconductor technology can be mapped on manufacturing cost and performance axis
- In reality, performance is not single axis but has multi-parameters such as speed, power, reliability etc.
- All these parameters can be measured and modeled depending upon specific applications
- Performance parameters can also be easily correlated to revenue ($$) depending on market size
- Having models which can model performance like speed, reliability helps in deciding the future course of technology

Motivation for Methodology



- Need for EH&S as 3rd axis, so technology can be mapped on space rather than plane, help in decision making
- EH&S like performance has multi-variables
- Health and Safety are hard to quantify
- So for now, Environmental Impact will be used as 3rd axis
- Even environmental is multi-parameter like energy, water and materials consumption and emissions
- These parameters can be related to cost ($$) through CoO models.
- To put Environment as 3rd axis, we need to have method or approach to quantify

Background of Environmental Impact Assessment –LCA &LCI

- LCA – Life Cycle Analysis - assessment of a product's full environmental costs, from raw material to final disposal, in terms of consumption of resources, energy and waste (product specific)
- LCI – Life Cycle Inventory - accounting of the energy and waste associated with the creation of a new product through use and disposal (process specific and knowledge or data can be extended to other products)

Background of Environmental Impact Assessment –Existing Methods

- CARRI (Computer Aided Relative Risk Impact)
  - Designed to assess relative risk of alternative manufacturing processes based on mass/flow and exposure information
  - Relies on its database to evaluate risks, therefore can not evaluate new chemicals
- DFESH (Design for Environment Safety and Health)- Mass/Energy Balance
  - Designed to evaluate mass and energy consumed, transformed and discharged from fabs
  - Has 57 unit operations with input data as process information and output data as air emissions and chemical wastage discharge
- The Target Method
  - Developed as a method to evaluate the environmental aspects of commercial and industrial activities in relation to earth's "carrying capacity"
- EnV-S (Environmental Value System Analysis)
  - Developed as a "bottom-up" equipment-centric approach to support both the analysis of EH&S and the design of semiconductor manufacturing process
  - Compares the overall environmental footprints of alternative technology

Background of Environmental Impact Assessment -Other Important Works

- Eric Williams – Environ Sci. Tech. 2002, 36, 5504-5510, LCA of 32 MB DRAM
  - Identified fabrication is most energy expensive stage
  - Identified etchants, acids/bases, photolithographic chemicals and chemicals used in processes
- Cynthia Murphy - Environ Sci. Tech. 2003, 37, 5373-5382, Parametric inventories for material, energy and emission
  - Developed parametric unit operation modules to predict changes in inventory as a result of changes in process flow and product design
  - Did a case study for energy in comparing two process flows with different number of metal levels
- Intel's paper – IEEE Symp. on Elec. & Environ. 2004, 97-103
  - Compared two generations of semiconductors
  - Defined major outputs such as PFC emissions, VOC's, HAP's, chemical wastage produced during semiconductor manufacturing

Objective of New Approach/Methodology

- “Fast” - Can help in decision making
- Identify problems/uncommon processes within new process technology
- Need to be quantitative, so can be compared easily (need not to be accurate)
- Will help building on LCI for all common semiconductor manufacturing processes such as Dielectric Etch, PECVD etc.
- For sake of completeness, new or uncommon processes will be estimated using existing knowledge

Description of New Approach/Methodology

- Identify standard or existing process flow and use current database or LCI for unit processes to estimate environmental impact
- For unit steps, where no database exist, need to estimate the environmental issues with process knowledge
- Assume emissions and consumption linearity with design parameters such as deposition thickness, volume etched
- Identify new steps or processes in new technology which needs to be evaluated
- Eventually, new/additional processes environmental footprint is compared with existing technology in order to understand the relative change
- Identified six environmental issues, which will be addressed in this approach – energy, water, emissions (PFC), HAP's, VOC's and chemical wastage
- So far, no packaging is considered, just focused on fabrication unit processes

Example- Strained Silicon technology

- No change in Back end
- Few additional/new steps in Front end
- New step like depositing epitaxial Ge along with Si, is very much like epitaxial deposition of Si (except need to evaluate GeH_4) and also additional annealing steps to relax Si-Ge layers
- Eventually, need to compare additional new steps with environmental footprint of existing standard technology

Case Study 2D v. 3D

- Typical 2D process flow is created for 250 nm process technology (using help of textbook and MTL standard flow)

- All unit processes are tabulated and with help of existing literature and some estimates, extrapolation of data is conducted to come up with basic environmental footprint

- New/additional 3-D processes were identified
  - Grinding has been estimated using oxide CMP
  - Bonding was another new process has been estimated like annealing (with pressure term as another additional energy consumption)
  - Besides all the other process were common

Assumptions in 2D process flow

- Twin-well CMOS process for Logic device with 7 metal layers
- Process flow for this 0.25 μm technology created with help of textbook (Silicon VLSI technology by Plummer)
- Process parameters were either taken from text or from process knowledge gathered from fabrication experience
- Overall process has 63 steps in front end with 1st metal level and 14 dual damascene steps repeated 6 times (84 at back end)
- LOCOS used instead of STI for isolation
- 1μm photoresist is used as standard process for all photo steps and ashing/piranha is done for striping resist
- First metal layer is Al with W plugs
- All other 6 metal layers and vias use Cu (dual damascene via first approach)
- Full RCA is conducted each time for clean i.e. SC1/dump/HF/dump/SC2/dump/dry
- Post CMP clean comprises of SC1 only

Unit Processes for 2D

Unit Processes	**Front End**	**Back End**
Photo	11 times (typical 1μm)	14 times (typical 1μm)
Piranha (removing photo)	11 times (typical)	
Oxide wet etch and	2 times	
TiN metal etch	1 time	
RCA clean (also include pre-metal)	8 times	9 times
Post CMP clean (oxide and Cu)		14 times
CVD W		1 time (750 nm)

Unit Processes for 2D

Unit Processes	Front End	Back End
PECVD oxide/ SiN (hard cap)/ BARC	1 time (Spacer 200 nm)	7 times (1200 nm)/ 6 times (30nm)/ 6 times (30nm)
LPCVD poly-Si/ Si_3N_4	1 time (gate 400 nm)/ 1 time (LOCOS 80nm)	
Sputtering Al/Ti/ Ta-Cu		1 time (500 nm)/ 1 time (200 nm for making contacts)/ 6 times (10-20 nm)
Electrodeposition Cu		6 times (for 1400 nm)
CMP Cu/W		6 times (Cu)/ 1 time(W)
CMP oxide		7 times

Unit Processes for 2D

Unit Processes	Front End	Back End
Ion Implantation	5 times (p-type)/ 4 times (n-type)	
Annealing/ thermal oxidation	1 time (furnace 4-6 hrs @1100C)/ gate oxide (10 nm)/ 2 times screen oxide (20 nm) and LOCOS(400 nm)/ 5 times RTP	
Oxide etch/ SiN (hard cap) and BARC opening	1 time spacer etch for 200 nm/ 1 time dry etch Nitride (LOCOS 80nm)	7 times (Via opening etch for 1000 nm)/ 6 times (line etch 500nm)
Poly-Si etch	1 time (gate etch)	
Al dry etch	1 time (500 nm)	
Ashing	11 times (typical)	14 times (typical)

First-Order Assumptions in Energy Estimation for 2D process flow

- Each unit operation is counted no. of times it appears in process flow and multiplied with average time required to average energy
- Processes like furnace annealing and thermal oxidation, CMP (Cu and oxide), electrodeposition of Cu and metallization (by PVD) are treated similar in energy consumption as a lack of data and similarity in the processes
- Pattern etch for all different materials are treated in similar way
- Clean is approximated as wet etch in terms of energy

Energy Estimation for 2D

Unit Operation	No. of times each operation	Wafers/run	Wafers/hr	Power (KW)
Implant	9	25	20	27
CVD	11	10	15	16
Clean/ Wet etch	31/14 (45 total)	50	150	8
Furnace	2	150	30	21
RTP	5	1	10	48
Oxidation	4	150	30	21
Etch	17	1	30	135
Ashing	25	1	20	1
CMP (Cu and ox)	14	1	25	29
Photo (coater)	25	1	60	90
Stepper	25	1	60	115
Electrodeposition	6	1	20	120
Sputtering	8	1	25	150

Available LCI Data and Sources

- Peter Dahlgren's Sematech Study (LCI)
  - Implanter, PECVD, Wet Spin etcher
- Cynthia Murphy's work
  - Furnace processes such as oxidation and annealing
  - Energy consumption for most of the unit processes for 0.13μm technology acquired with the help from Sematech and some other member companies
- Guess estimates

New/Additional Processes in MIT's Cu-Cu bonding 3D Process Flow

Unit operations	**Description and no. of times**
PECVD oxide	200 nm on handle wafer (Once)
Sputtering Al	20 micron-release layer on handle wafer (Once)
Sputtering Ta/Cu	50/300 nm on Handle wafer+ bond pads
CMP Cu	Twice before bonding
Grinding/ CMP Si	First layer of device wafer
Wet etch	Thrice (After grinding Si etch TMAH, BOX etch, Al release layer by HCl:H2O)
Photo	Once to make bond pads at back side
Dry etch	Si & ILD to make contacts/ etch oxide (twice)
Bonding	Twice (Handle to device & device to device)
Ashing	Once (Strip PR)
Electrodeposition Cu	Once in contacts formed at back side

Comparison b/w 2D and 3D in Terms of Processes

Unit operation	2D process flow (for one wafer)	Additional 3D processes in flow
Photo/stepper/ashing	25	1
Dry Etch	13	2
Wet etch/Clean	31/14	3/4
CVD	11	1
CMP	14	2
Sputtering Al	1 (0.5 μm for metal 1)	1 (20 μm)
Sputtering Ta/Cu	6	1
Electrodeposition Cu	6	1
Bonding	0	2
Grinding	0	1

First-Order Energy Comparison in 2D v. MIT's 3D Process Flow

- Sputtering 20 micron Al for release layer seems outrageously huge number and largely energy consuming
- Bonding and Grinding are new processes which needs to be estimated
- Besides these all processes are small in percentage as compared to full process flow, so can be easily ignored
- Grinding can be estimated using CMP, just that it takes a bit longer to thin wafer but energy usage must be similar
- Bonding can be estimated using vacuum process with temperature budget of 300 degrees centigrade for half an hour

Conclusion and Future Work

- Methodology for environmental evaluation has been established
  - Establish environmental footprint or impact for standard flow
  - Compare it with new/additional significant processes
- MIT 3D technology has been studied as case study from energy standpoint
- Other 3D technology such as RPI, IBM, Intel needs to be compared from environmental standpoint
- Needs to complete LCI data for other unit operations by literature survey or by experimentation
- Similar comparisons like energy for other environmental axis such as air emissions like VOC's, HAP's and GWP gases

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