Wafer Cleaning in Semiconductor Manufacturing: The Single-Wafer Inflection Point

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Outline

- Trends in the Semiconductor Industry
- Wafer Cleaning Challenges
- Migration to Single Wafer Processing
- New Wafer Cleaning Technologies
- Summary

Applied Materials Corporate Profile

Applied Materials is the global leader in nanomanufacturing technology™ solutions for the electronics industry with a broad portfolio of innovative equipment, service and software products

Providing:

- Wafer Fabrication Systems
- Flat Panel Display PECVD and Test Systems
- Environmental Solutions
- Manufacturing Execution System (MES) Software
- Global Service Products

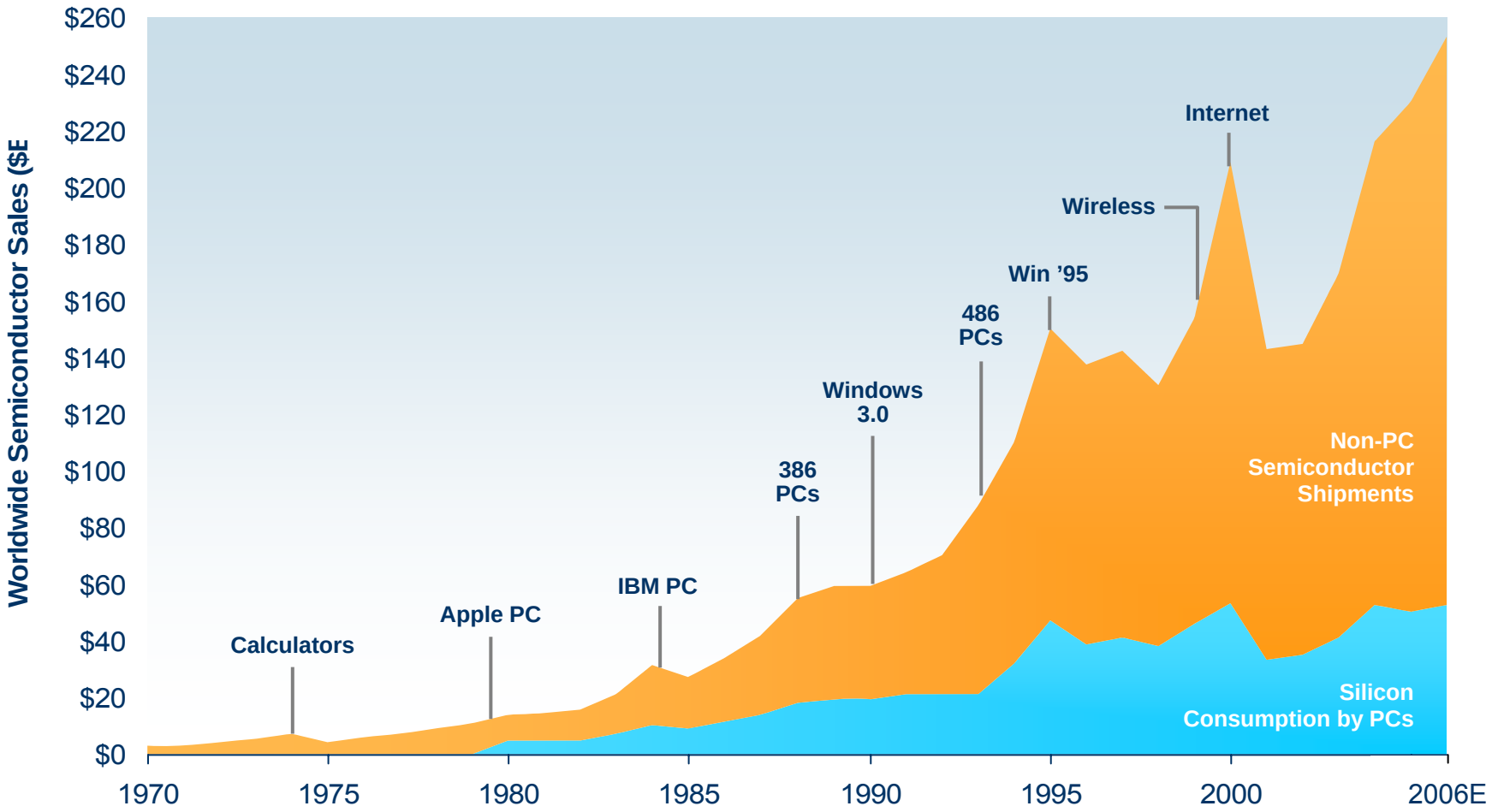
Top 15 Worldwide Semiconductor Equipment Manufacturers

2005 Rank	CY2005 Sales ($M)*	Company
1	**7,043.2**	**Applied Materials**
2	5,211.3	Tokyo Electron Ltd.
3	3,159.6	ASML
4	2,213.0	Nikon Corporation
5	2,167.0	Canon Inc.
6	2,005.4	KLA-Tencor
7	1,959.9	Advantest Corporation
8	1,916.2	Hitachi High-Technologies Corp.
9	1,537.7	Dainippon Screen Mfg. Co., Ltd.
10	1,382.3	Lam Research Corporation
11	1,302.4	Novellus Systems, Inc.
12	1,180.0	Ulvac, Inc.
13	814.2	Teradyne, Inc.
14	811.7	ASM International N.V.
15	605.6	Varian Semiconductor Equipment

* Includes service and spares. Source: VLSI Research 5/06

Worldwide Semiconductor Shipments

Industry Transformation



Sources: WSTS, Gartner Dataquest, IDC, Applied Materials

Semiconductor Devices – 2006 Outlook

- 2006 semiconductor revenue estimated to be $253.2B (10% growth)

- Semiconductor device expectations:
  - NAND flash memory to grow 53% to $16.2B
  - DSPs to grow 17% to $8.9B
  - DRAM sales to grow 8% to $27.6B
    - Bit shipment growth at 55-60%

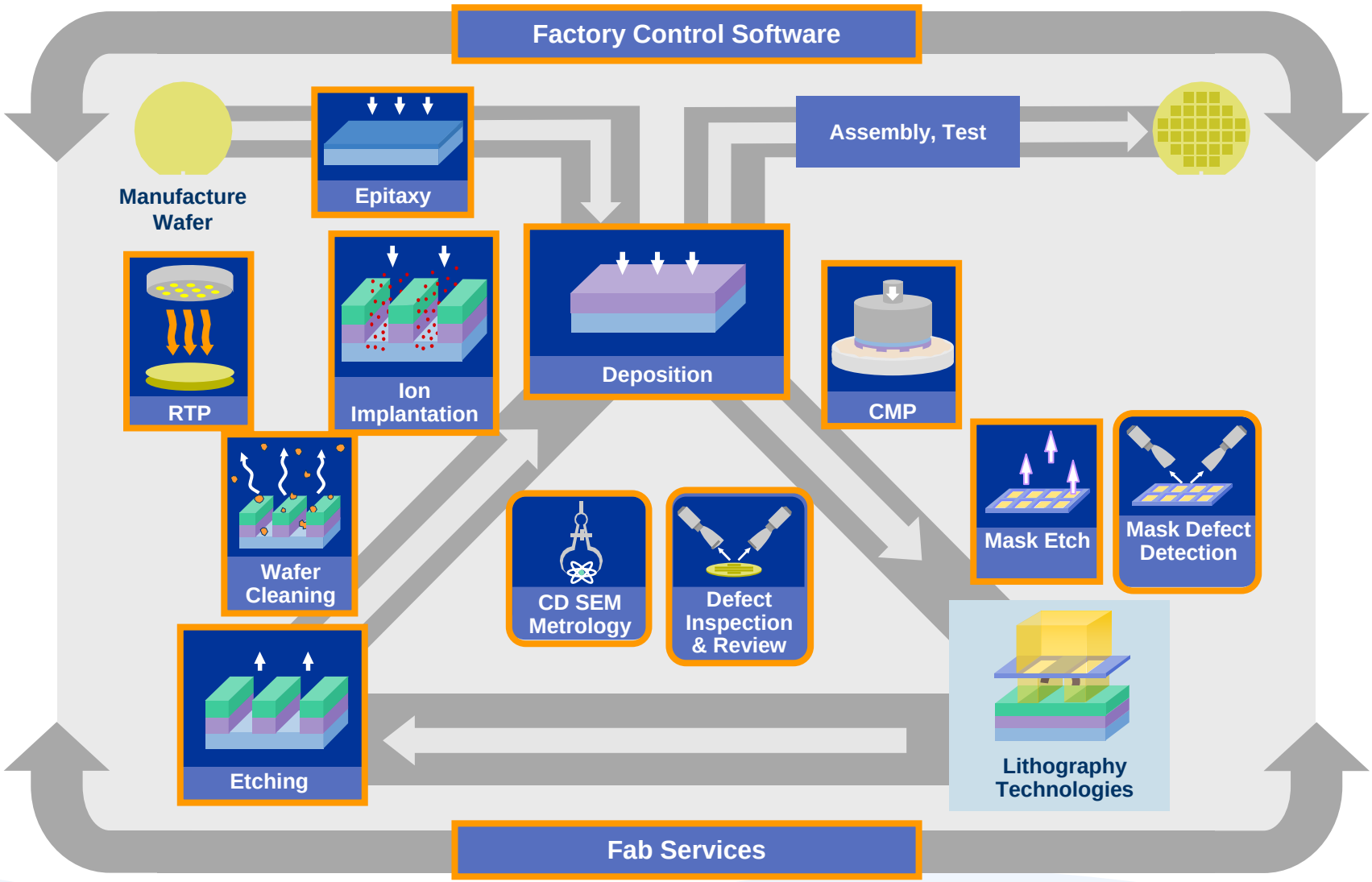



Sources: SIA, Applied Materials

2006 Wafer Fabrication Equipment Drivers

- Production capabilities down to 65nm
- 300mm capacity investments
- Memory and foundry-related equipment spending
- Wafer Cleaning Drivers
  - Conversion of FEOL to single-wafer
  - Lower geometries requiring more advanced technologies
  - Conversion to lower K drives need for watermark-free hydrophobic surface drying

Semiconductor Wafer Processing



Complexity of Surface Preparation Tools

- →Chemistry
- →Concentration
- →Temperature
- →Residence Time
- →Flow Dynamics
- →Robot Dynamics
- →Software and control
- →Exhaust Flow
- →Cross contamination
- →Rinsing Efficiency
- →Chem/DIW Dispense
- →Spin Variables
- →Material Compatibility
- →Wafer Support Features
- →Several Hundred Other Inputs

- →Particles (<65nm)
- →Metals (ppt - ppq)
- →Surface Organics (1.0E12 C atoms/cm^2)
- →Surface Anions (<ppb)
- →Etch Rates (1 A to several thousand A/min)
- →Etch Uniformity (<1%, 1σ for a 10 A removal)
- →Surface Haze
- →Surface State Control
- →Residue Removal
- →CD Control

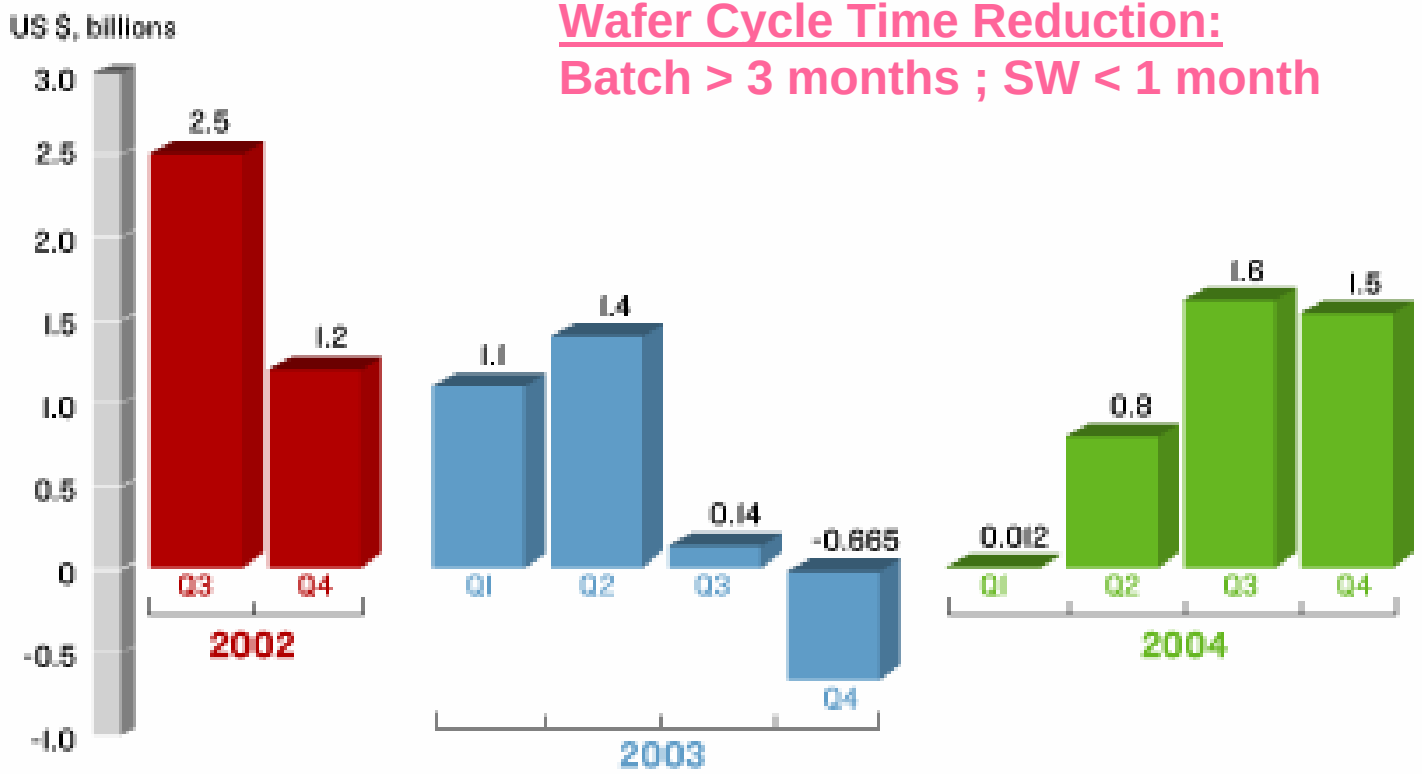
Surface Preparation Challenges for 45nm and Below

- Removal of sub-50nm particles
- Cleaning without pattern damage and film loss
- Surface state control
  - HF-last processing
  - Interfacial layer formation for pre high-κ deposition
- Drying philic/phobic structures and high aspect ratio features
- Process control and uniformity

Why Single Wafer Processing ?

- Benefits
  - Improved process control and much reduced defectivity
  - Reduced cycle times
    - Typical batch process times of ~1 hr reduced to about 3 min single wafer
  - Greatly improved process uniformity
  - Edge/bevel cleaning
  - Damage-free cleaning
  - Interface control for new materials
- Challenges
  - Throughput vs. batch
  - IPA drying

Single Wafer Justification: Reducing Excess Chip Inventory

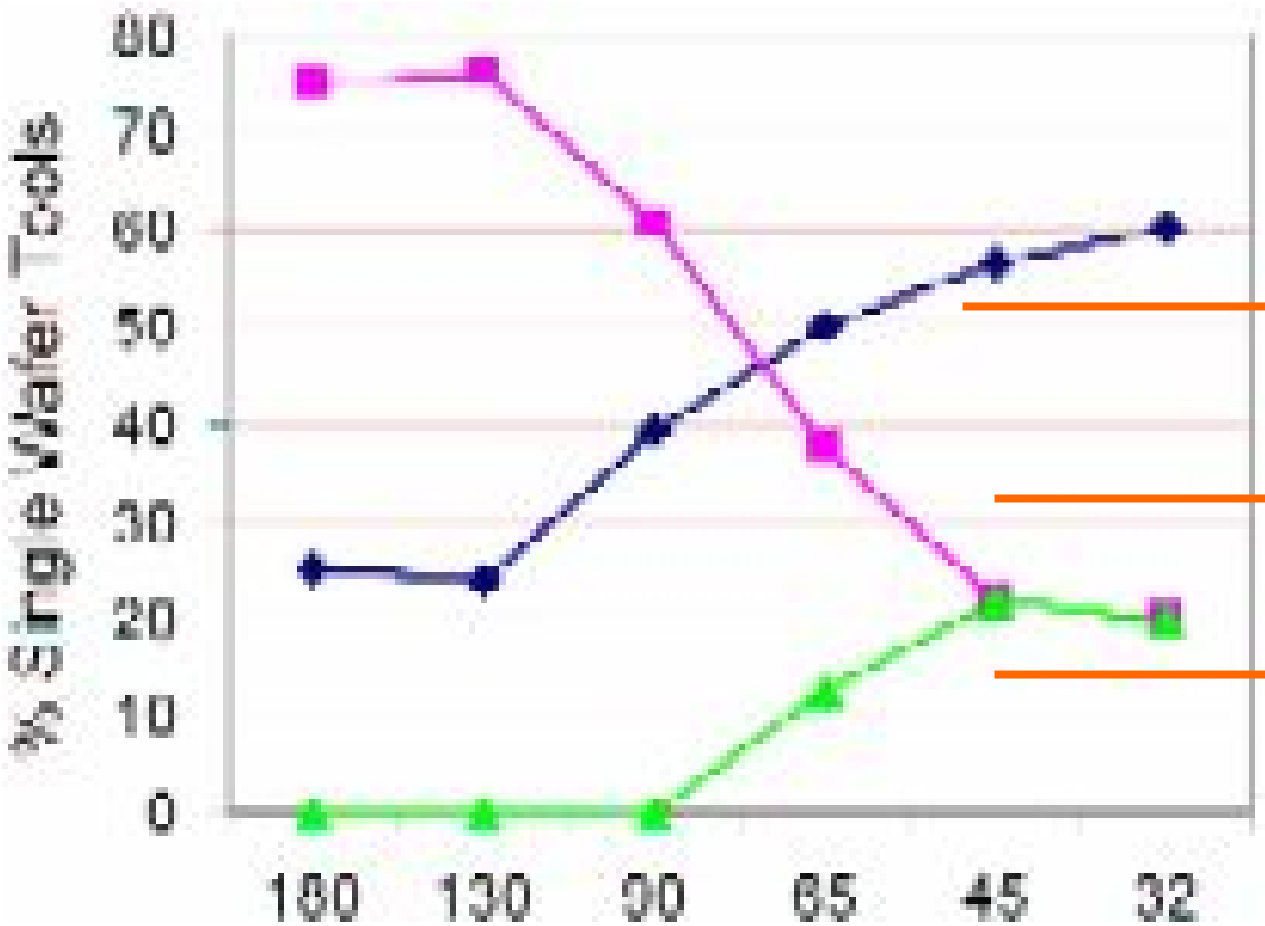


Wafer Cycle Time Reduction:
Batch > 3 months ; SW < 1 month

$1.5 Billion Excess Inventory in Q4/2004 due to Batch Processing

R. Singh (Clemson U) and R. Thakur (AMAT), IEEE Spectrum, Feb. 05

Single Wafer vs. Technology Node



Source: AMD Presentation at the 2005 ConFab Meeting

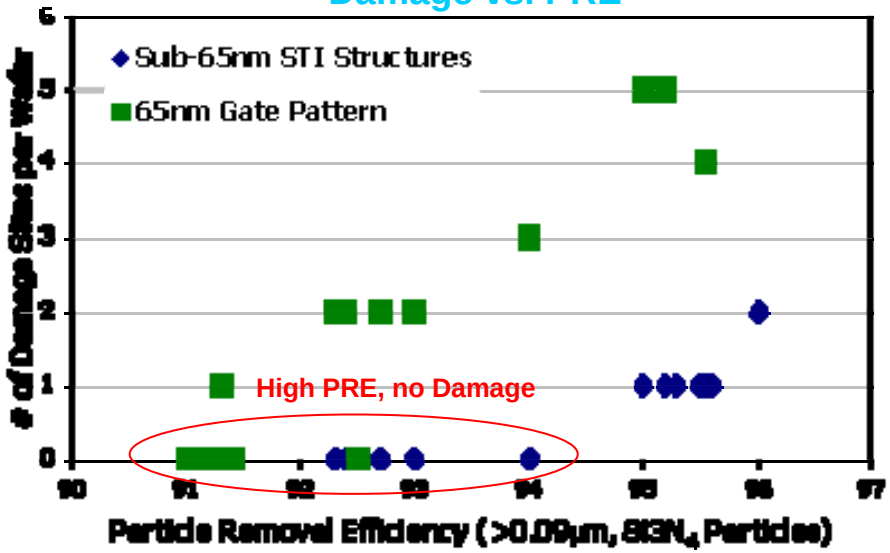
New Single Wafer Technologies from AMAT

- Immersion single wafer processing
  - Directed triple-megasonics for damage-free cleaning with min film loss
  - Fast fill and drain chamber design
    - Etch uniformity control for <10 A removal
    - Thin interfacial layer formation through oxide growth and controlled etchback
  - Enhanced Marangoni Dry
    - Watermark-free drying of high aspect ratio features
    - HF-last processing
- Spin single wafer processing with integrated Marangoni drying
  - Mixed-fluid jet cleaning for damage-free cleaning
  - Full face megasonics for backside-cleaning
  - Marangoni dry
    - No ESD (non-spin dry)
    - Improved defect performance at small particle sizes
    - Watermark-free drying

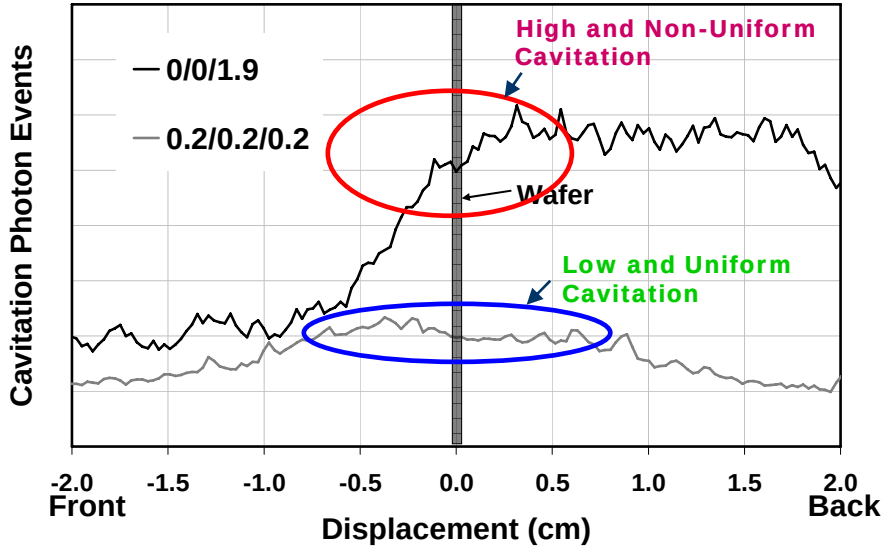
Immersion Single Wafer Processing:

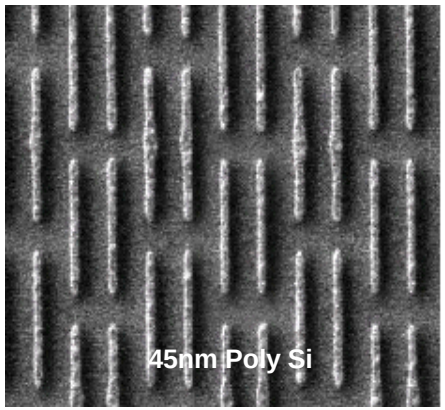
Triple Megasonics: Cavitation control for High PRE, no Damage

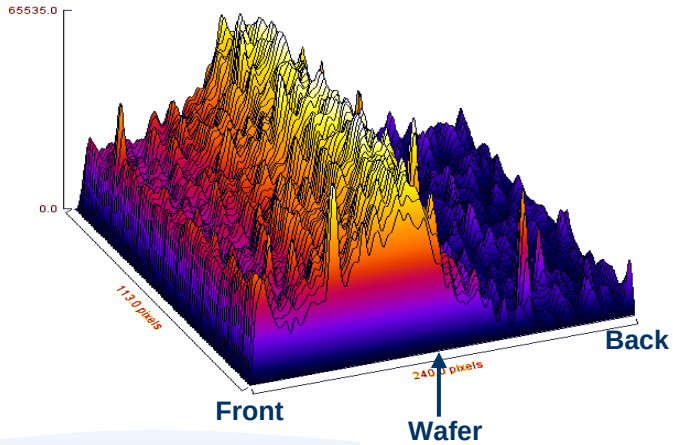
Damage vs. PRE



Tunable Cavitation Control



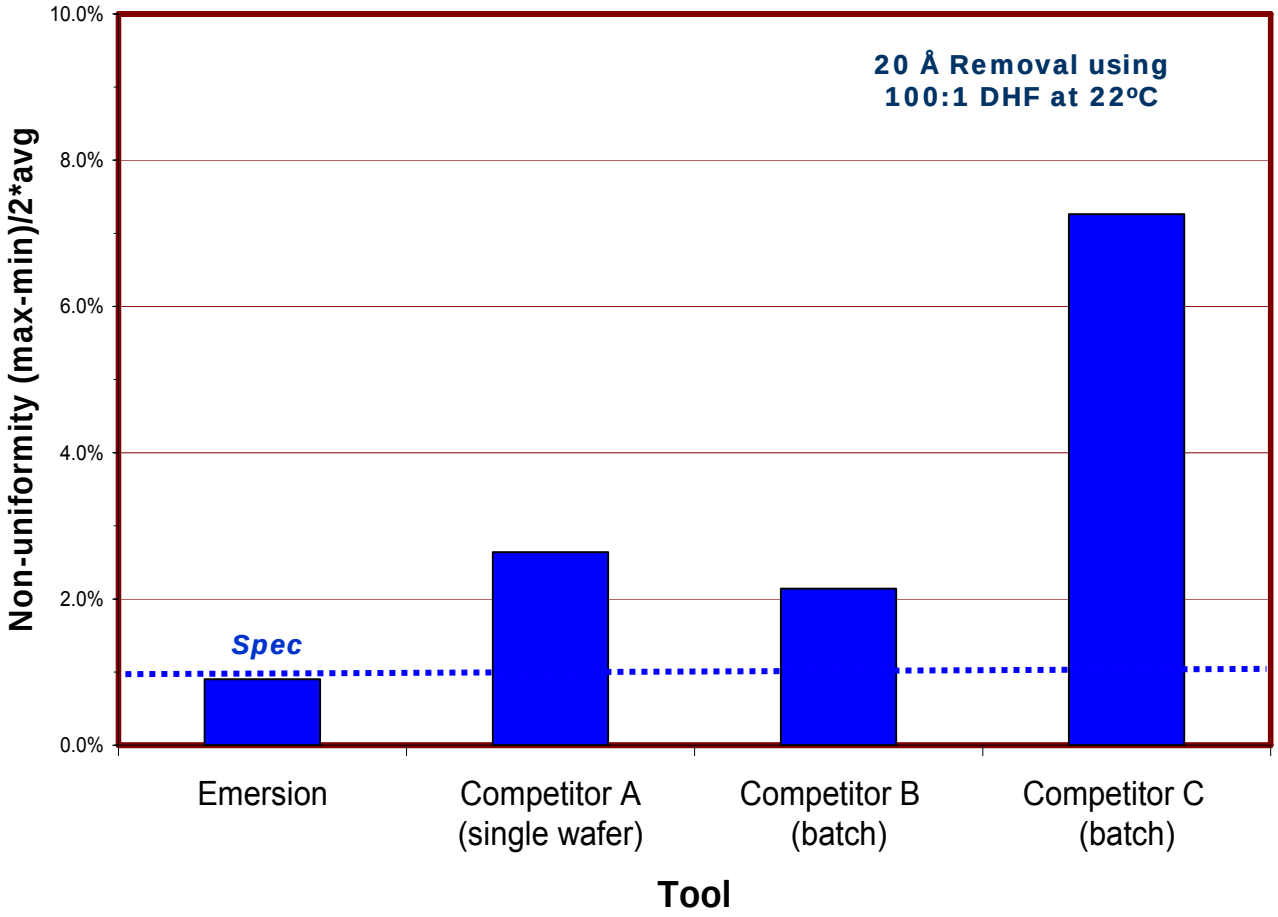




Immersion Single Wafer Processing:
Short Process Times: Low Film Loss

	Wet Bench		Immersion Single Wafer
	High Temp RCA (70°C, 5min)	Low Temp RCA (25°C, 10min)	SC1 Clean (50°C, 30sec)
Oxide Loss	~20 Å	~2-5Å	<0.3 Å
Silicon Loss	~20 Å	~2-5Å	<0.6 Å
PRE % (0.09µm Si_3N_4)	>95%	~70-85%	>95%

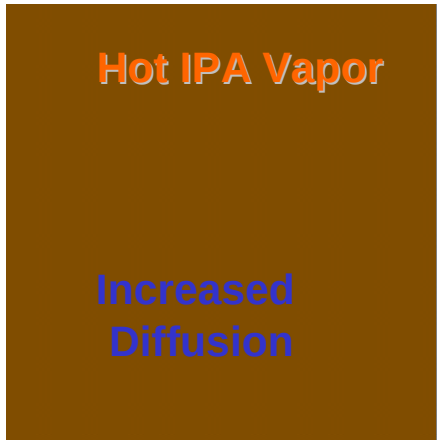
Immersion Single Wafer Processing:
Fast Fill/Drain Design: Controlled Film loss and Uniform Etch

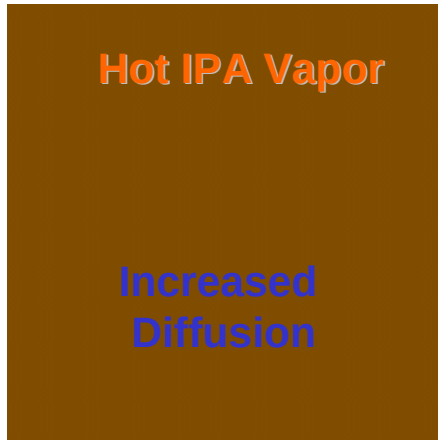


Immersion Single Wafer Processing:

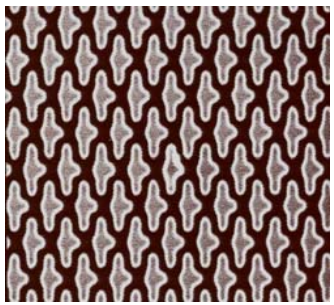
Enhanced Marangoni Drying with Megasonics for Watermark-free Drying

Wafer Motion



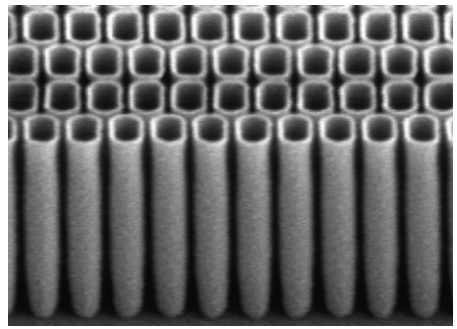


Bulk Fluid



65nm STI

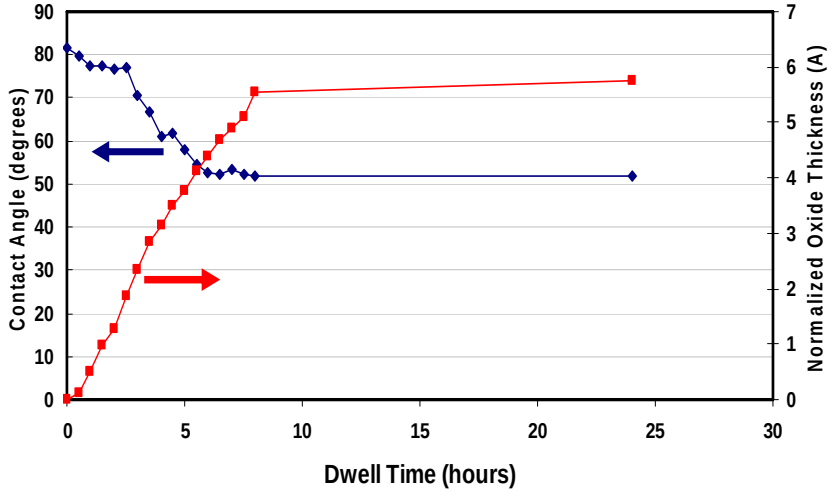
Soft Megasonics
Thinner Capillary layer
Larger Marangoni force



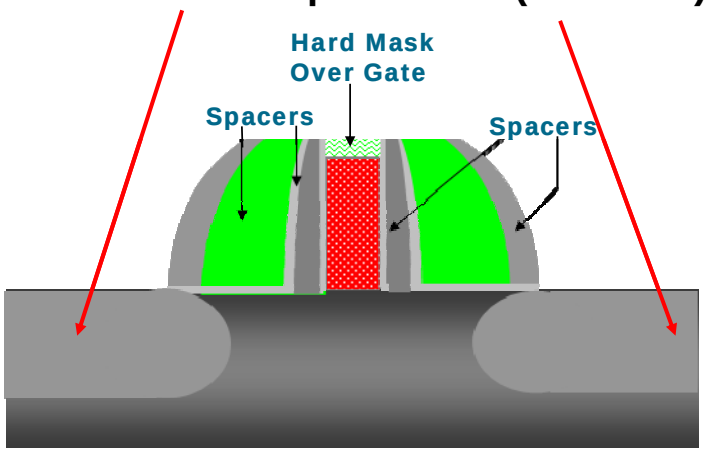
>60:1 Gap AR Cap Structure

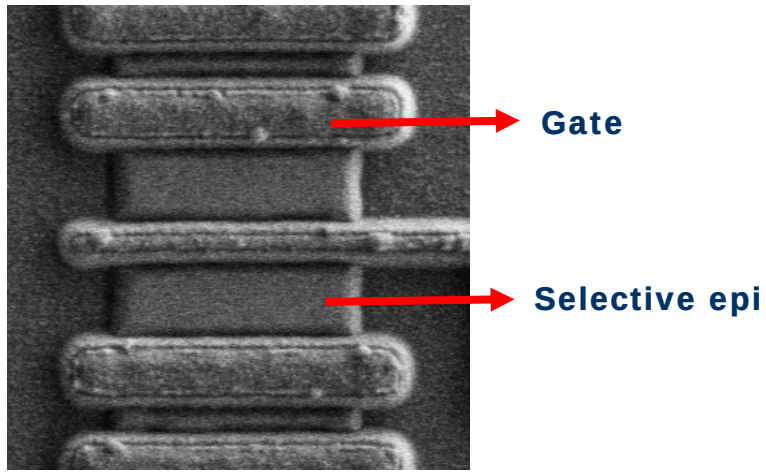
Immersion Single Wafer Processing:
Surface State Control for Pre SiGe Cleans

- **HF-Last pre-epi clean for selective epitaxial growth**
  - Surface stability vs. Queue time
- **Process Results**
  - Selective epi for raised S/D
  - No negative effect for ~5 hr Q-time

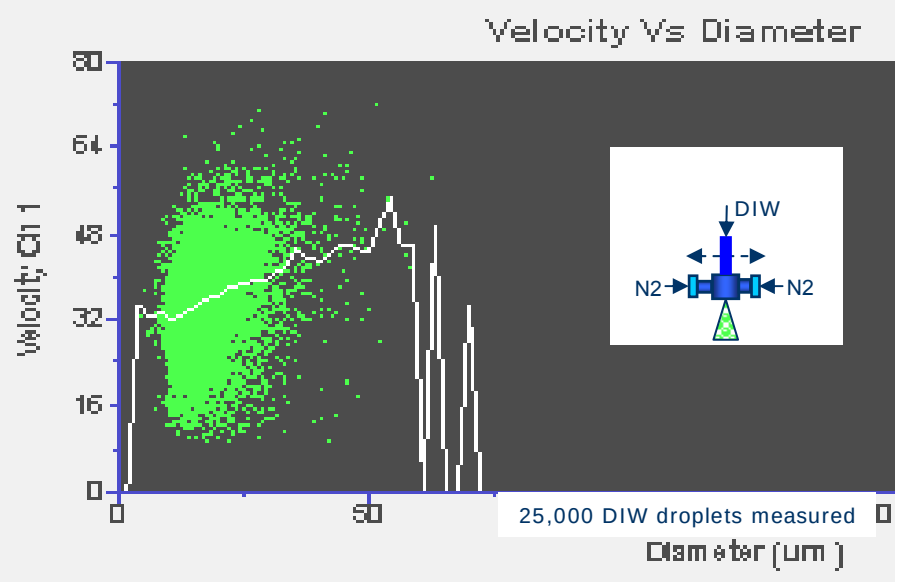


S/D Recess: depth ~ 1kÅ (~3:1 AR)





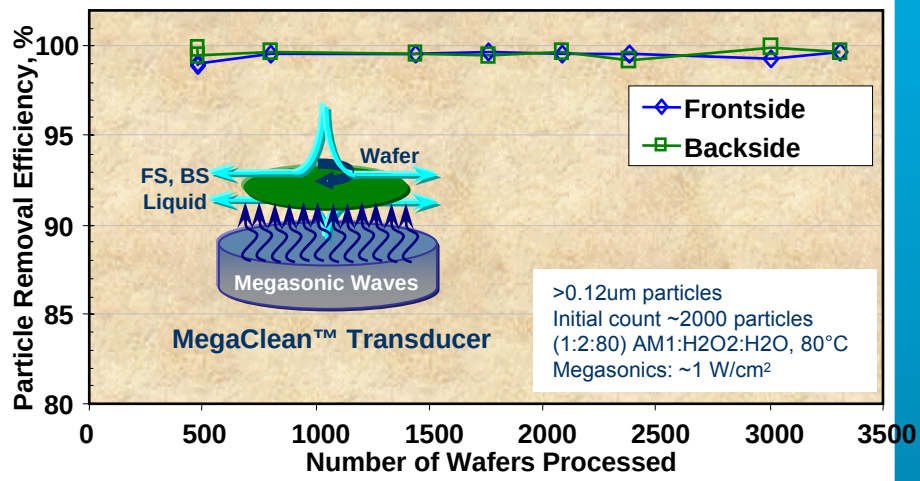
Spin Single Wafer Processing with Integrated Marangoni Drying:
Mixed Jet Fluid for Damage-free Cleaning and Megasonics for Backside Cleaning

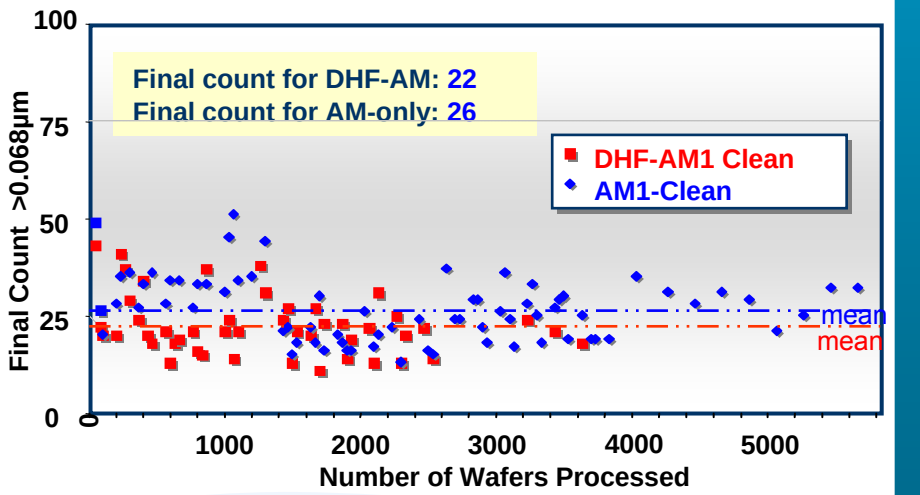


$D_{v0.5}$ = 22.1um
DIW droplet average velocity=34m/s
CIP on-going to 10um droplet size

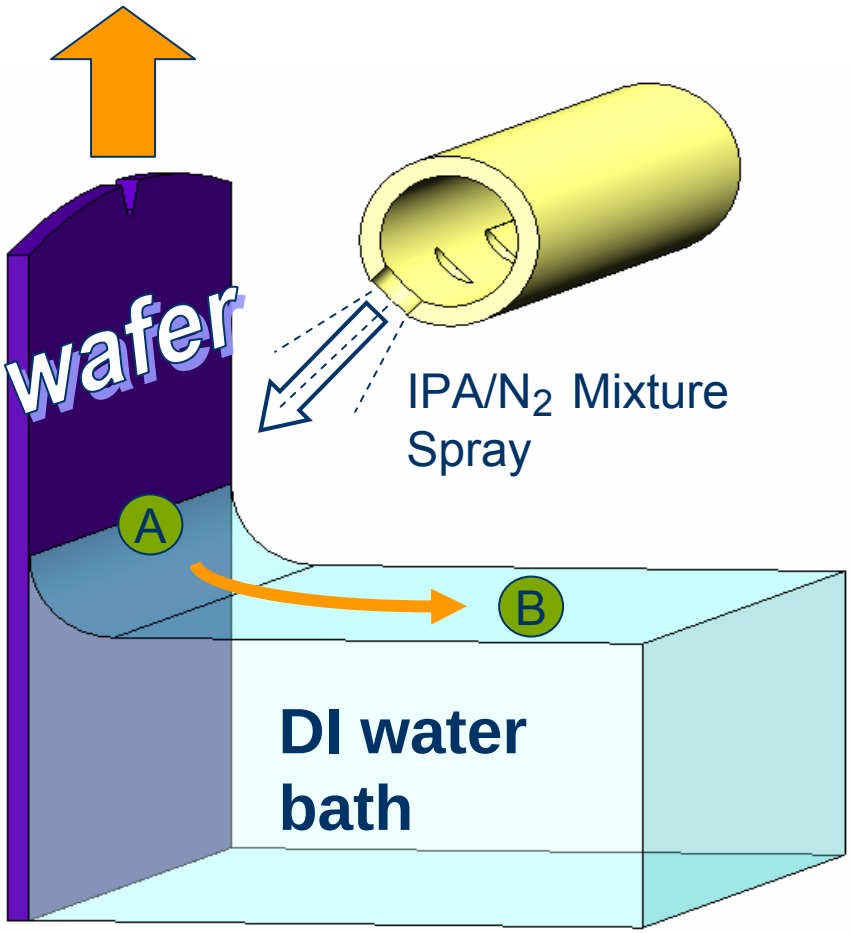
Test structures	Chemistry Only (PRE %)	Chemistry + OS (PRE %)	Damage sites
65nm Poly lines	75%	99%	0
80:1 Capacitors	41%	95%	0

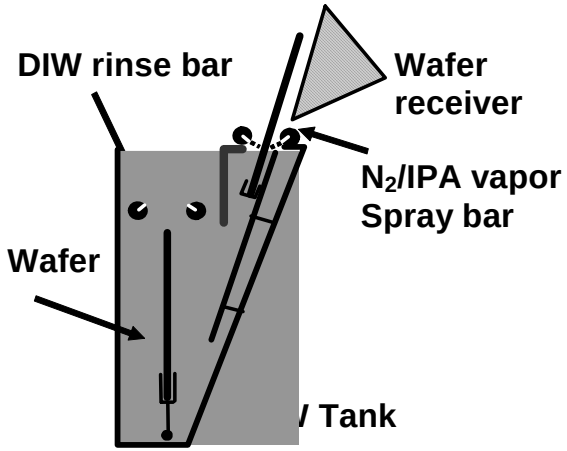
Megasonics - Full Plate

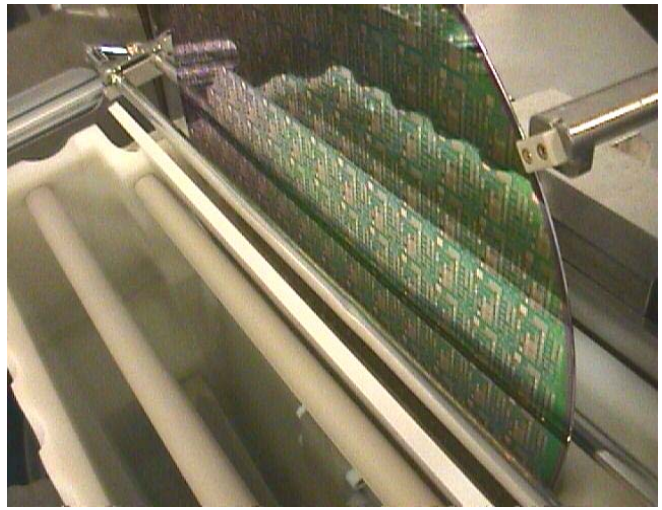




Spin Single Wafer Processing with Integrated Marangoni Drying:
Single Wafer Marangoni® Dryer Design





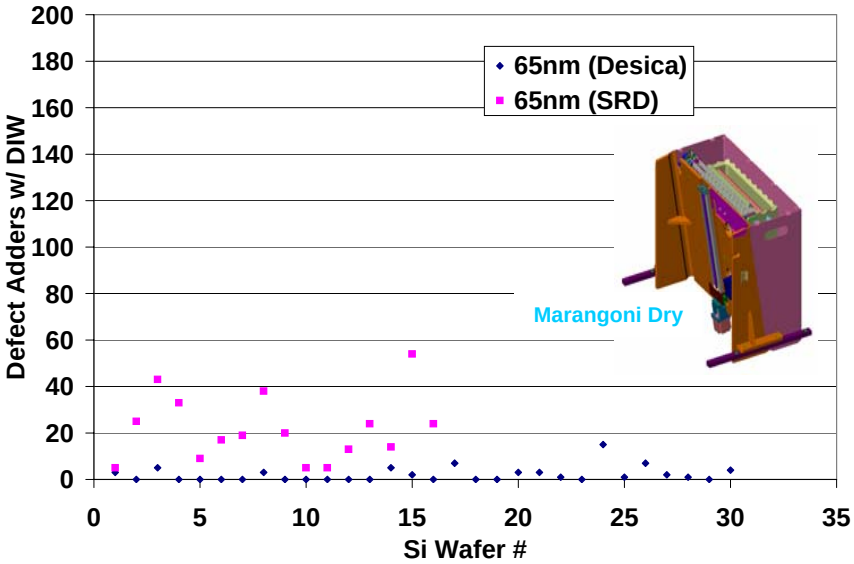


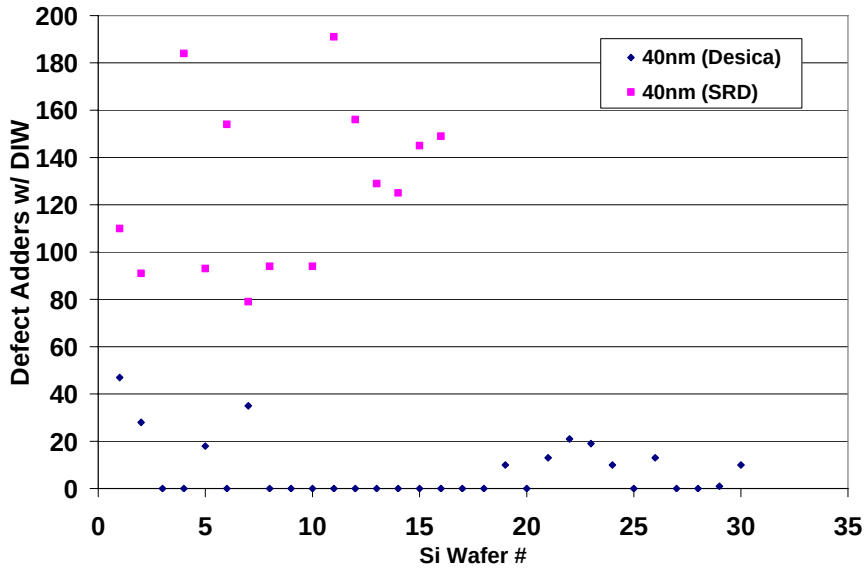
Surface tension gradient draws water away from surface

DIW/Vapor Interface is STABLE & REPRODUCEABLE

Spin Single Wafer Processing with Integrated Marangoni Drying

Particle performance at small particle sizes (Marangoni vs. SRD)





Can Single Wafer meet the Throughput Requirements?

- Single wafer processing with new and innovative technologies show advantages and promise over batch processing to meet 45nm and below technology requirements
- Traditional batch wet cleaning systems can achieve higher throughputs (~200 wph for critical cleans)
- AMAT's new platform has unique hardware and architecture which makes it the first single-wafer tool to achieve 200 wph throughput for both FeOL and BeOL cleans.

Summary

- **Trends in the Semiconductor Industry:** Semiconductor shipments to exceed $250B in 2006 (10% growth) driven by Consumer Products. Memory becoming a much larger component of the product mix.

- **Wafer Cleaning Challenges:** The most commonly used step in semiconductor manufacturing now requires unprecedented chemical, uniformity, and defect control.

- **New Wafer Cleaning Technologies:** New chemical combinations and hardware innovations allow faster processing times, thus enabling single wafer approaches for many applications.

- **The Future of Wafer Cleaning:** Multi-chamber platforms based on single wafer processing will dominate future high productivity fabs.

APPLIED MATERIALS®