Modeling of Pattern Dependencies in the Fabrication of Multilevel Copper Metallization

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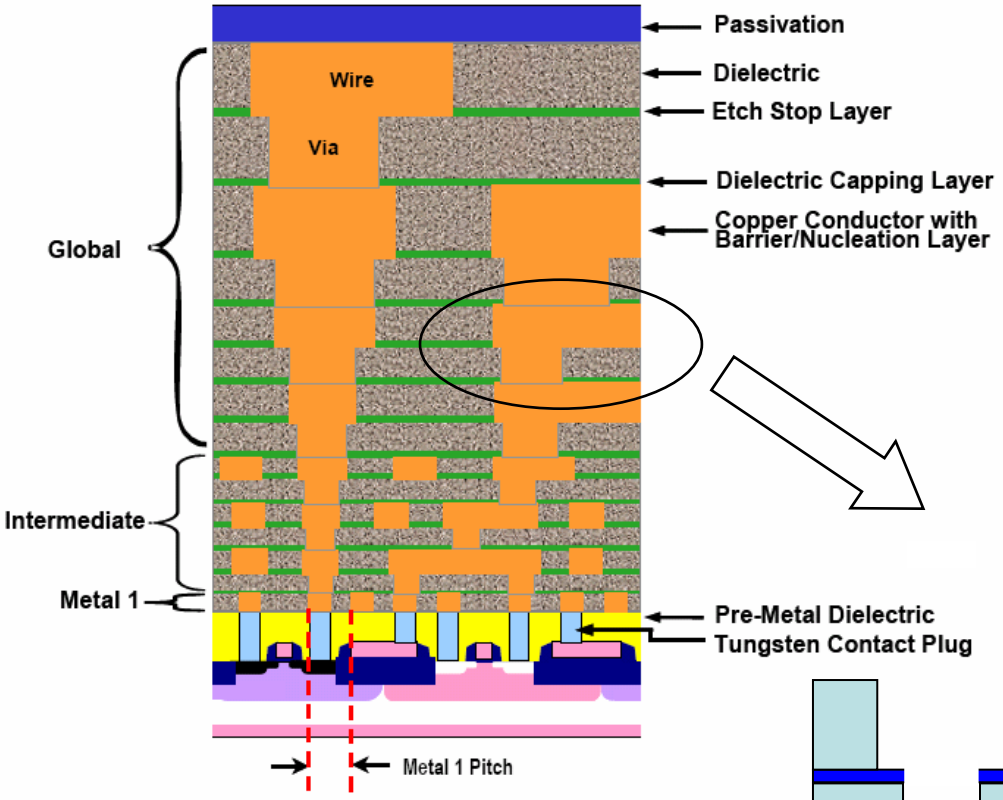
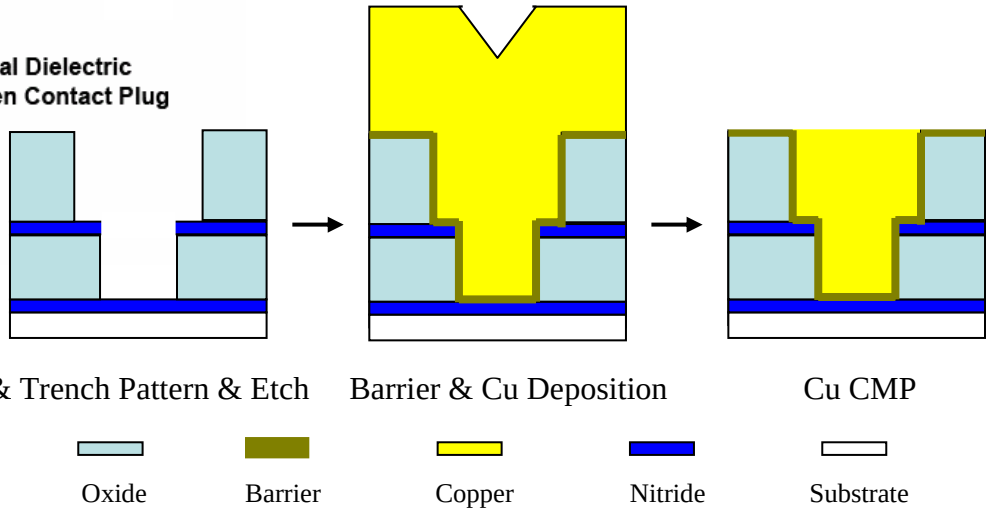
Multilevel Copper Metallization

Cross-section of Hierarchical Scaling



From ITRS 2005

Dual Damascene Process Flow



R. H. Havemann et al., Proceedings of the IEEE, 2001

OUTLINE

- Motivation for Research
- ECD Chip-Scale Model
  - Model Review
  - New Model Framework
  - Calibration and Verification
  - Summary
- CMP Chip-Scale Model
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- Application
  - In-Pattern Dummy
  - Sensitivity Analysis
- Conclusion and Future Work

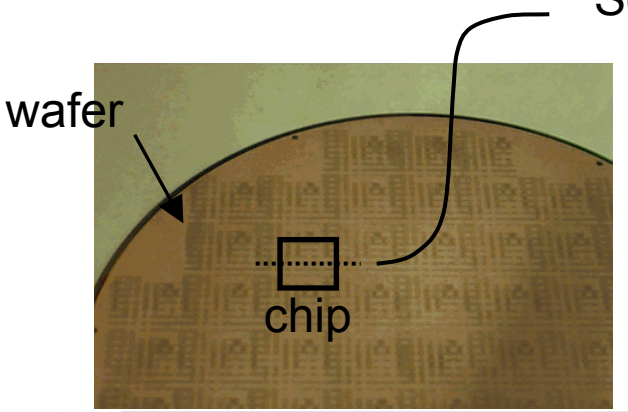
Motivation: Pattern Induced Thickness Variation

- Significant copper thickness variation
- Performance and yield loss

Question:

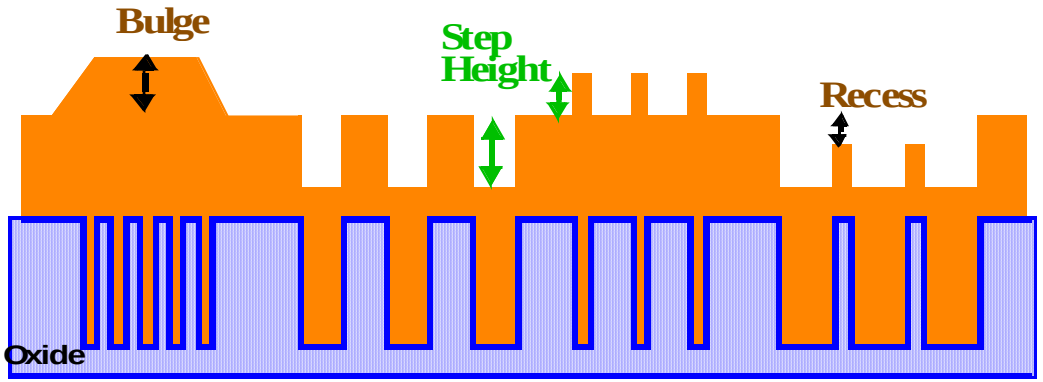
How can we model and predict the topography variation?

How to optimize process, layout and dummy design

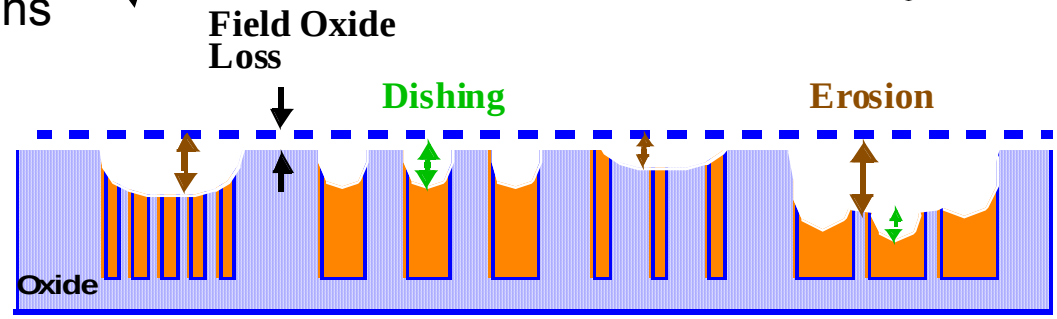


Cross Sections

Electroplating Problems

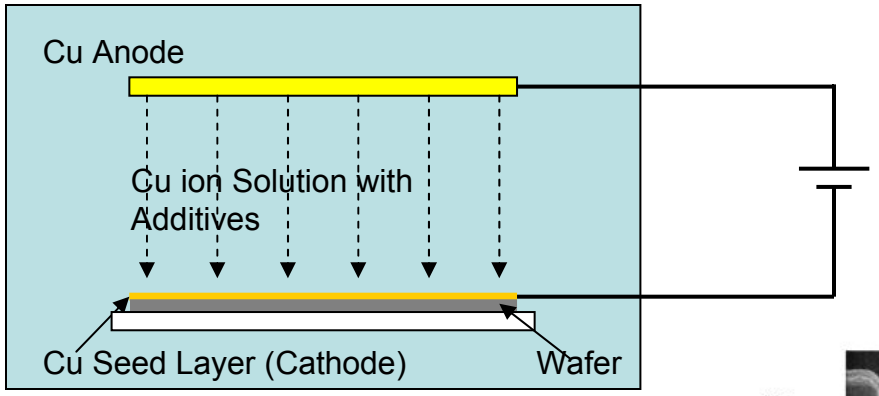


CMP Problems

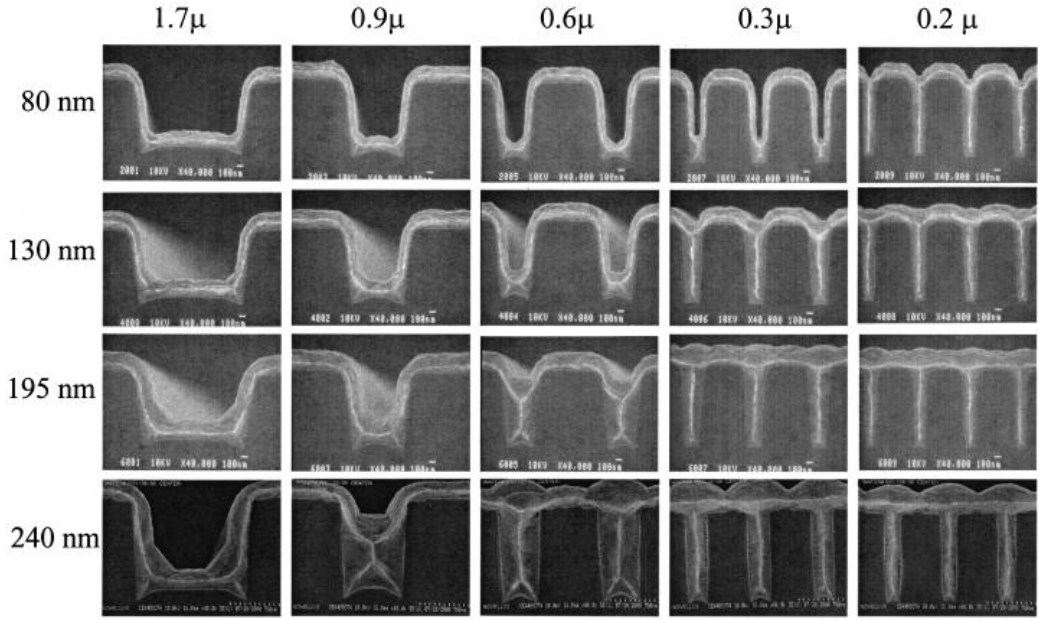


T. Park, Ph.D. Thesis, EECS, MIT, May 2002.

Copper Electrochemical Deposition



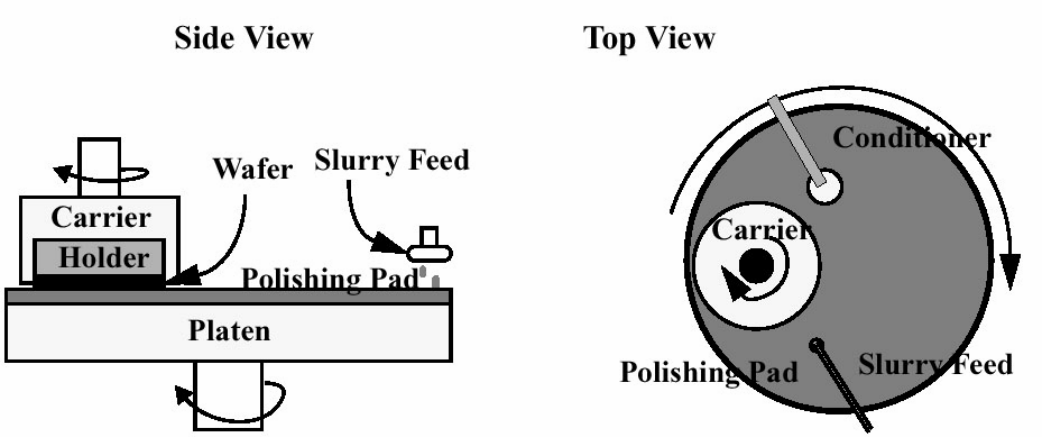
Principle of Copper ECD



Results of Copper Fill Experiments.
X: feature size, Y: Nominal field Cu thickness.

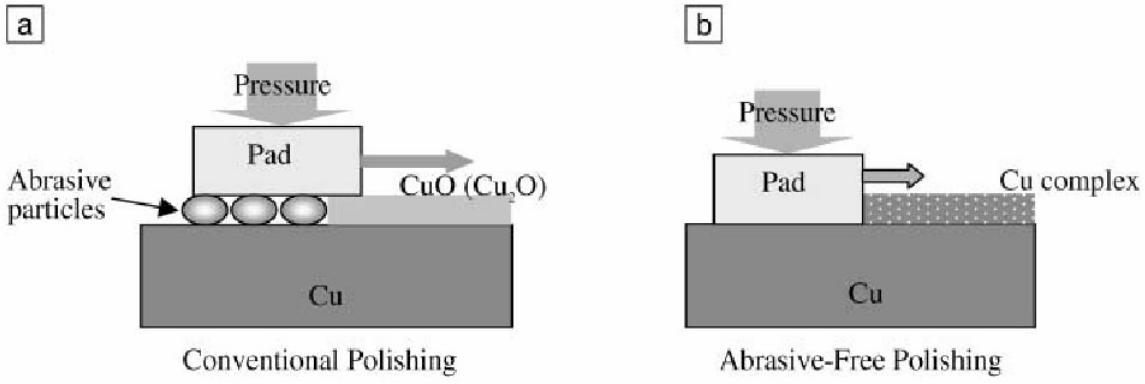
T. P. Moffat et al., Electrochemical and Solid-State Letters, 2001.

Chemical-Mechanical Planarization



Rotary CMP Tool

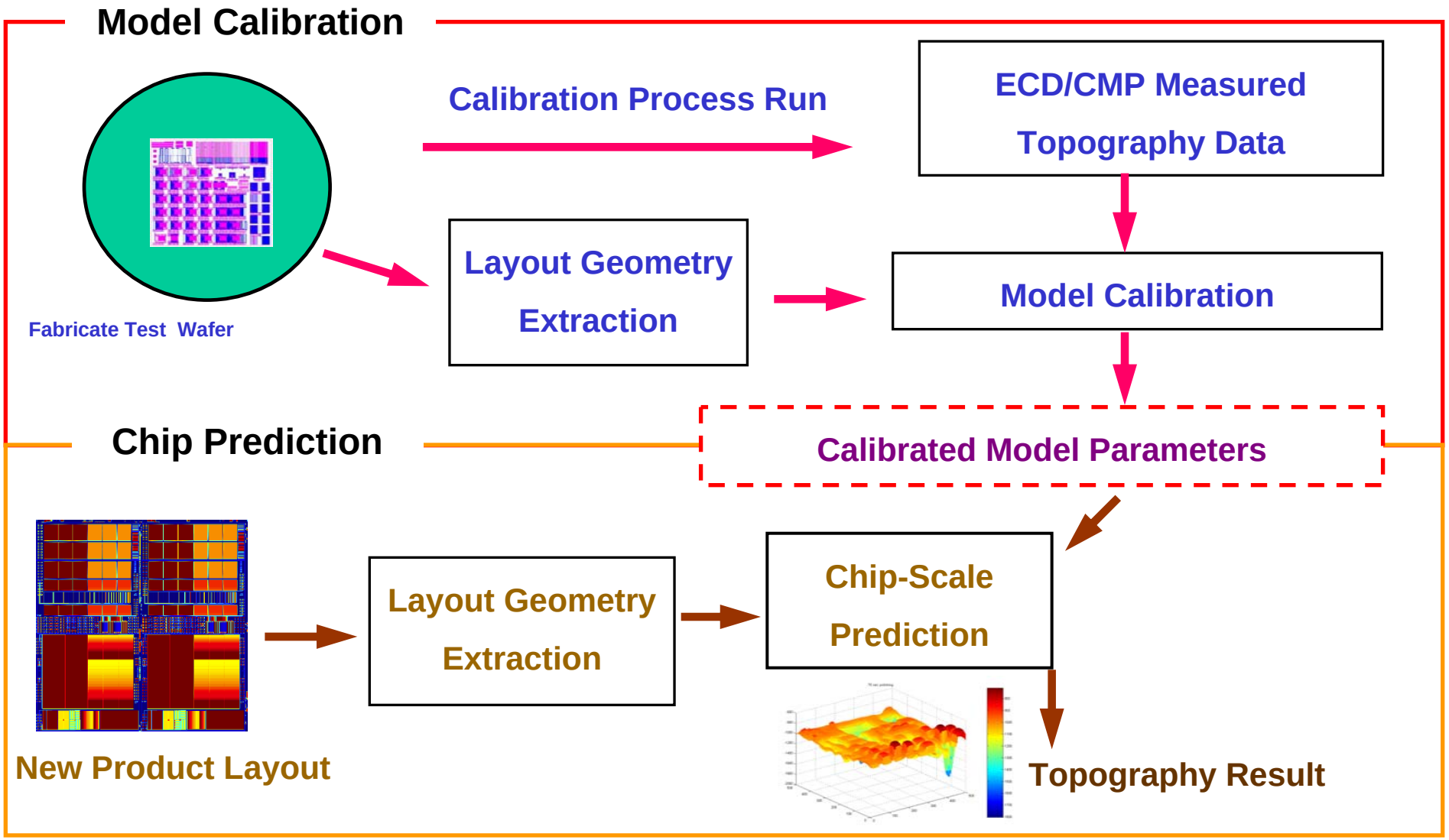
T. Park, Ph.D. Thesis, EECS, MIT, May 2002.



Schematic Illustration of Cu CMP Mechanisms
(a) Conventional Slurry (b) Abrasive-Free Polishing Solution

M. Hanazono et al., MRS Bulletin, 2002.

Overall Methodology



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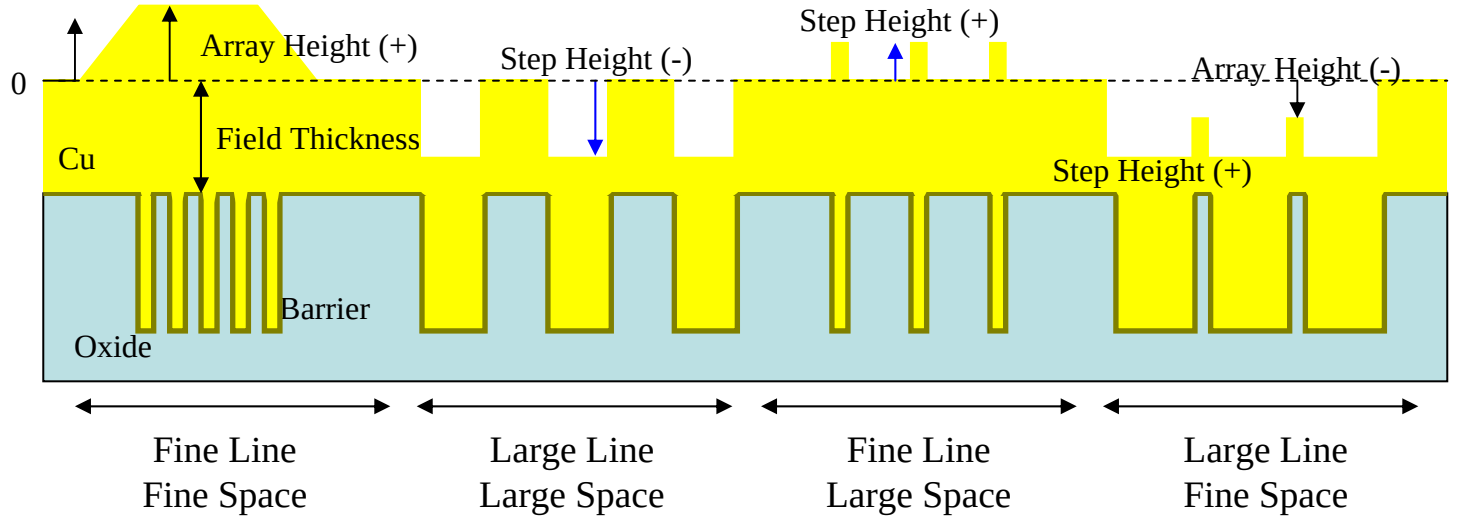
ECD Chip-Scale Model: Chip-Scale Model Review



Step Height and Array Height Definitions in ECD

Park's Response Model to Capture *AH* , *SH* and *Field Thickness* Variations:

$$AH = a_A W + b_A W^{-1} + c_A W^{-2} + d_A S + e_A (WS) + Const_A$$

$$SH = a_S W + b_S W^{-1} + c_S W^{-2} + d_S S + e_S (WS) + Const_S$$

$$FT_g = \alpha \left\langle \overline{SA_g} - C_o \right\rangle + F_o$$

T. Park, Ph.D. Thesis, EECS, MIT, May 2002.

ECD Chip-Scale Model : Feature-Scale Model Review

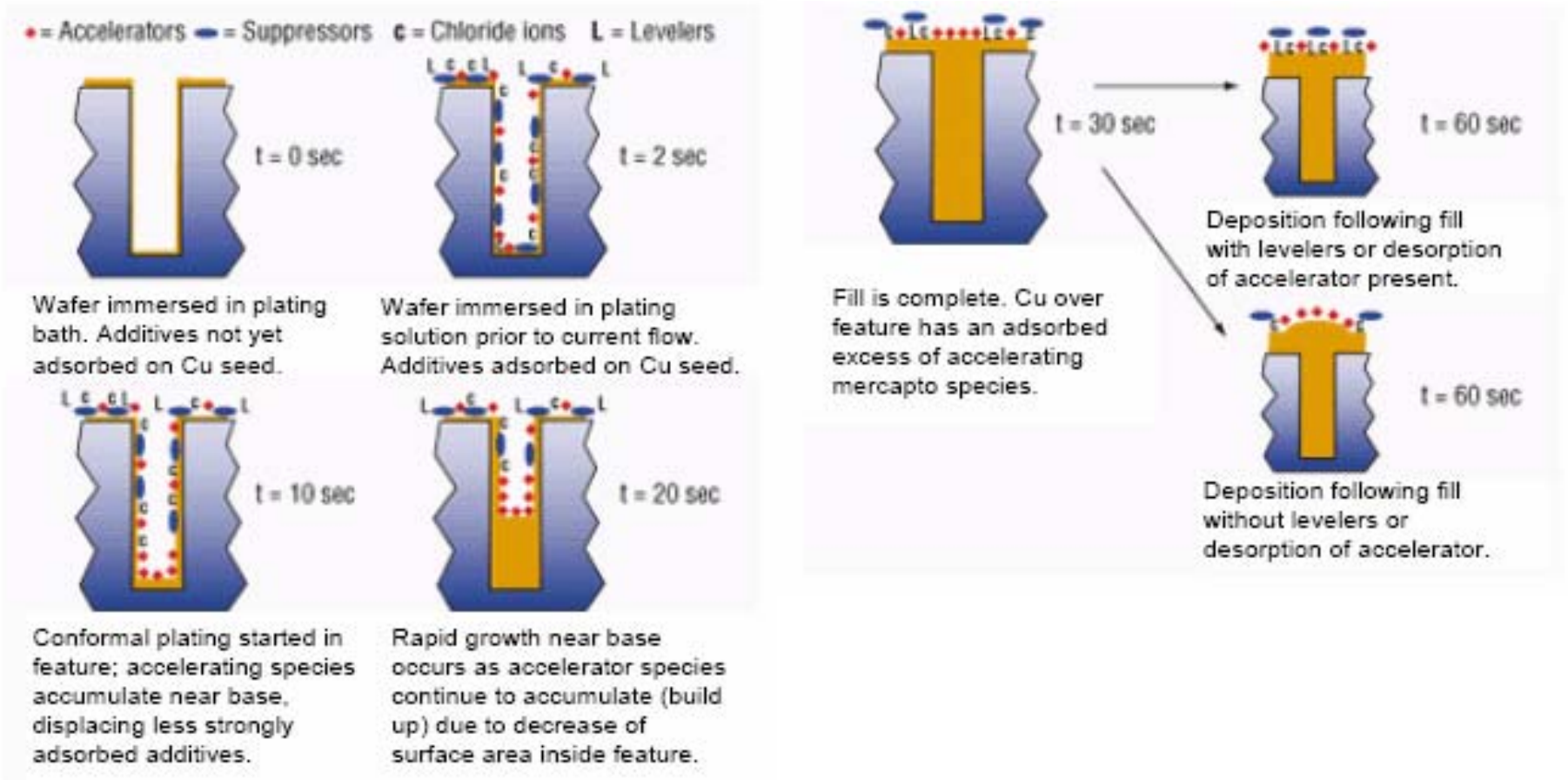


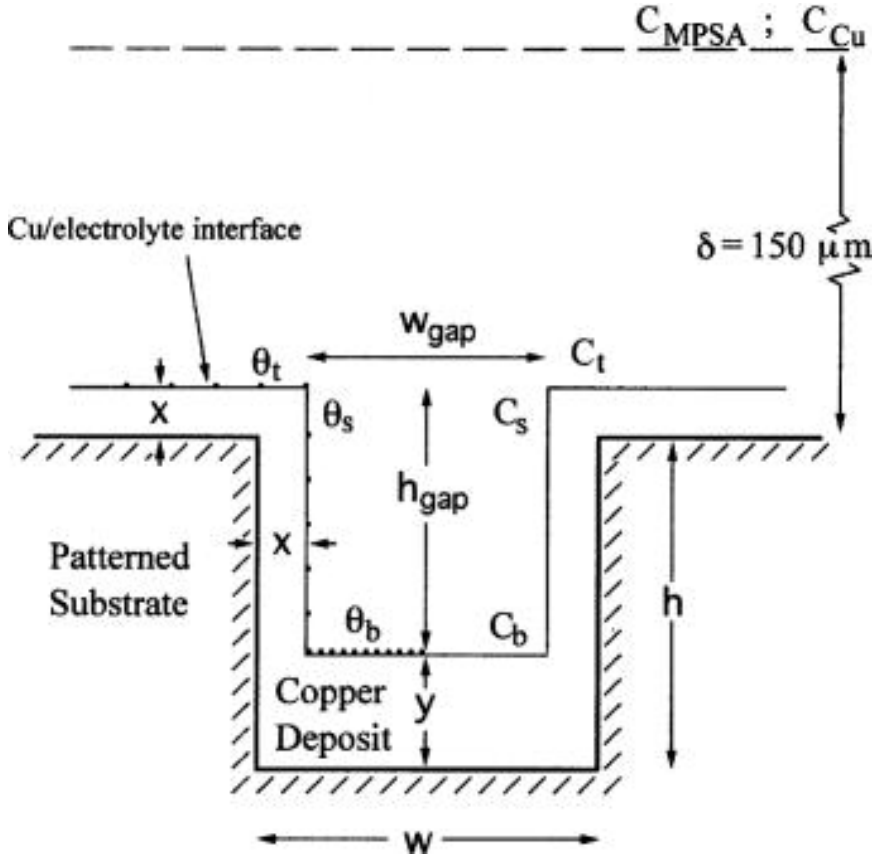
Illustration of additive adsorption behavior during plating fill.
A mechanism for the establishment and propagation of bottom-up fill is suggested.

J. Reid et al., Solid State Technology, July 2000.

Chip-Scale ECD Model

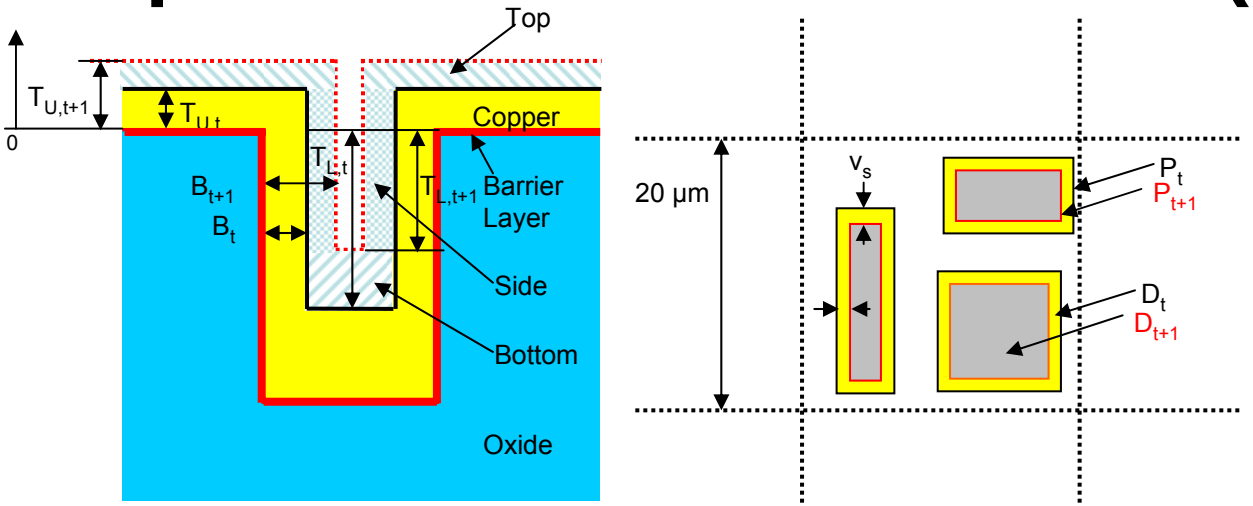
- Chip-scale ECD model
  - Based on feature-level ECD model
  - Dynamically tracks evolutions of additives concentration and topography
  - Requires small number of model parameters

Schematic of the Approximate Geometry for the Simple Model

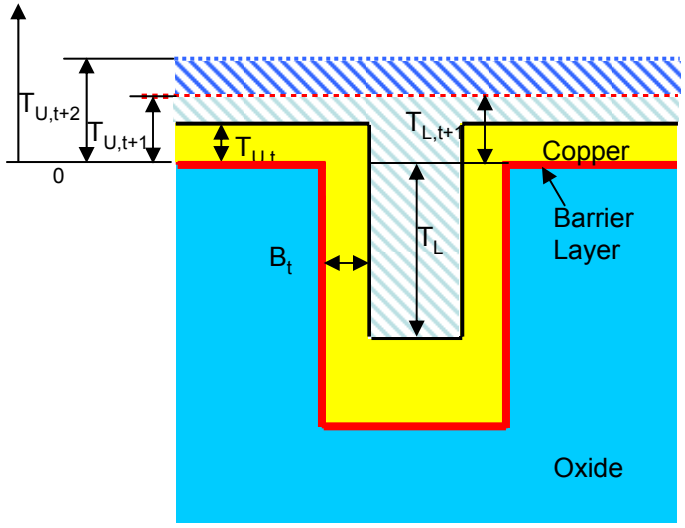


D. Josell et al., Journal of the Electrochemical Society, vol. 148, no. 12, pp. 767-773, 2001.

ECD Chip-Scale Model : New Chip-Scale Model Framework (1)



Profile Evolution before Trench Overfill at Feature Level



Profile Evolution after Trench Overfill at Feature Level

ECD Chip-Scale Model : New Chip-Scale Model Framework (2)

Equations before trenches are filled:

Growth rate: $$\upsilon(\theta, C) = \frac{C}{C_{Cu}} R_0 \left(1 + k\theta_{ACC} - \theta_{SUP}\right)$$

$$\theta_{ACC,t}^{t+1} = \theta_{ACC,t}^{t} \frac{\left(1 - D^{t}\right)}{\left(1 - D^{t+1}\right) + P^{t+1} v_t^t / l^2} - k_1 \left(\theta_{ACC,t}^{t} - \theta_{ACC,eq}\right)\Delta t$$

$$\theta_{ACC,b}^{t+1} = \theta_{ACC,b}^{t} \frac{D^t}{D^{t+1}} + \theta_{ACC,s}^{t} \frac{P^t v_b^t}{D^{t+1} l^2} - k_1 \left(\theta_{ACC,b}^{t} - \theta_{ACC,eq}\right)\Delta t$$

Surface Area Change

$$\theta_{ACC,s}^{t+1} = \theta_{ACC,s}^{t} - k_1 \left(\theta_{ACC,s}^{t} - \theta_{ACC,eq}\right)\Delta t$$

Absorption/ Desorption

$$\theta_{SUP,t}^{t+1} = \theta_{SUP,t}^{t} - k_2 \left(\theta_{SUP,t}^{t} - K(1 - \theta_{SUP,t}^{t} - \theta_{ACC,t}^{t})\right)\Delta t$$

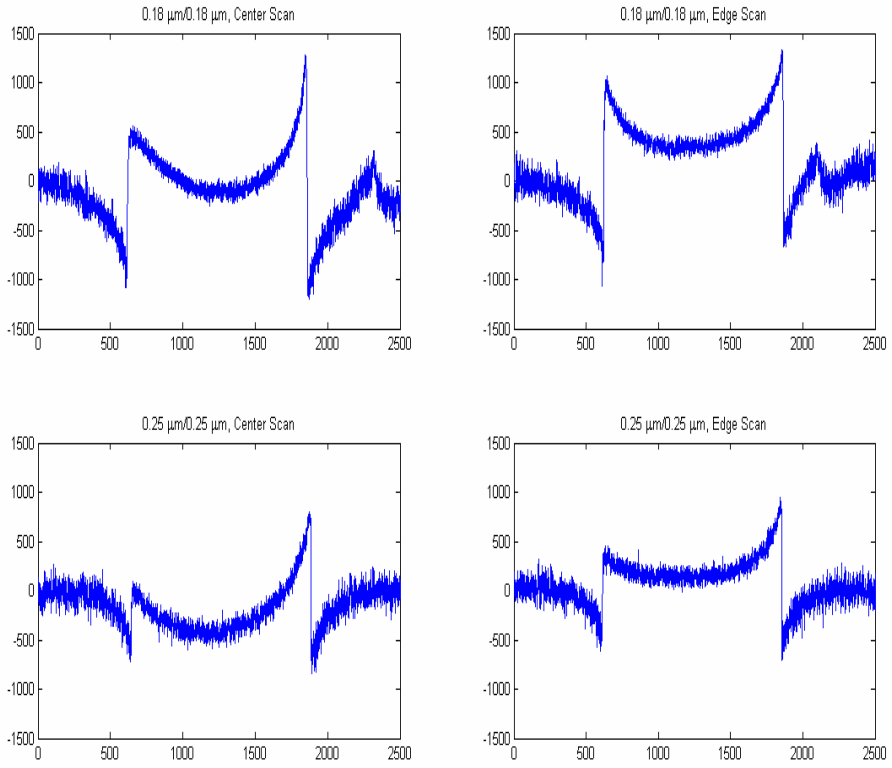
$$\theta_{SUP,s}^{t+1} = \theta_{SUP,s}^{t} - k_2 \left(\theta_{SUP,s}^{t} - K(1 - \theta_{SUP,s}^{t} - \theta_{ACC,s}^{t})\right)\Delta t$$

$$\theta_{SUP,b}^{t+1} = \theta_{SUP,b}^{t} - k_2 \left(\theta_{SUP,b}^{t} - K(1 - \theta_{SUP,b}^{t} - \theta_{ACC,b}^{t})\right)\Delta t$$

Additive Competition

ECD Chip-Scale Model : New Chip-Scale Model Framework (3)

Long-range (mm scale) Pattern Effect

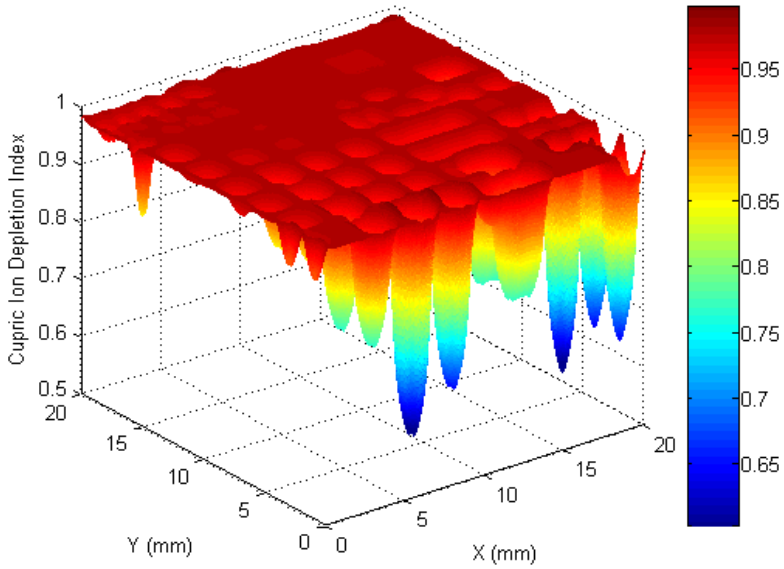


Center and Edge HRP Scans for CPT 104-01

Inter-feature cupric ion depletion:
– Spatial averaging approach

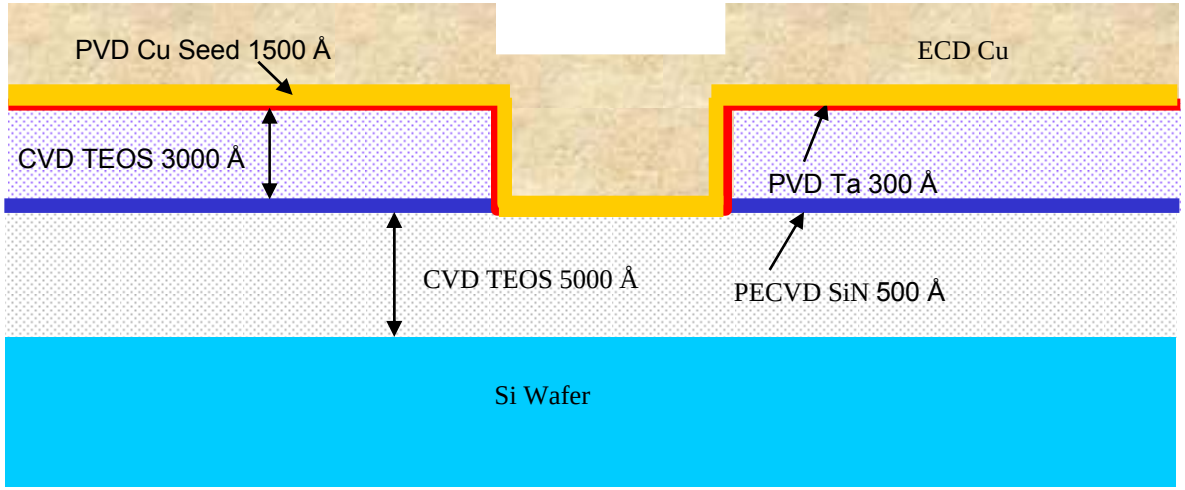
$$M'_{R^t} = \left[F_{filter}(M_{R_N},\ L_{ECD})\right]^{-\alpha}$$

$$M_{R^t} = M'_{R^t} / Max(M'_{R^t})$$

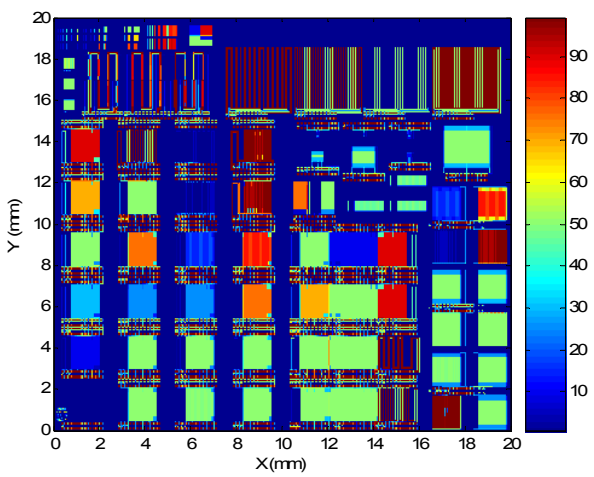


Cupric ion depletion ratio

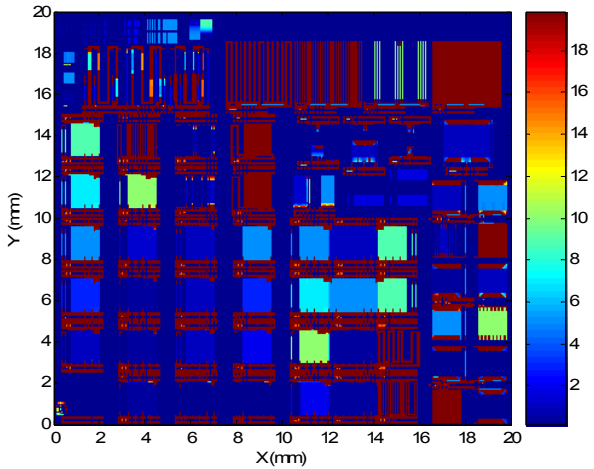
ECD Chip-Scale Model: Calibration (1)



Stack Information for MIT/SEMATECH 854 M1 Wafers

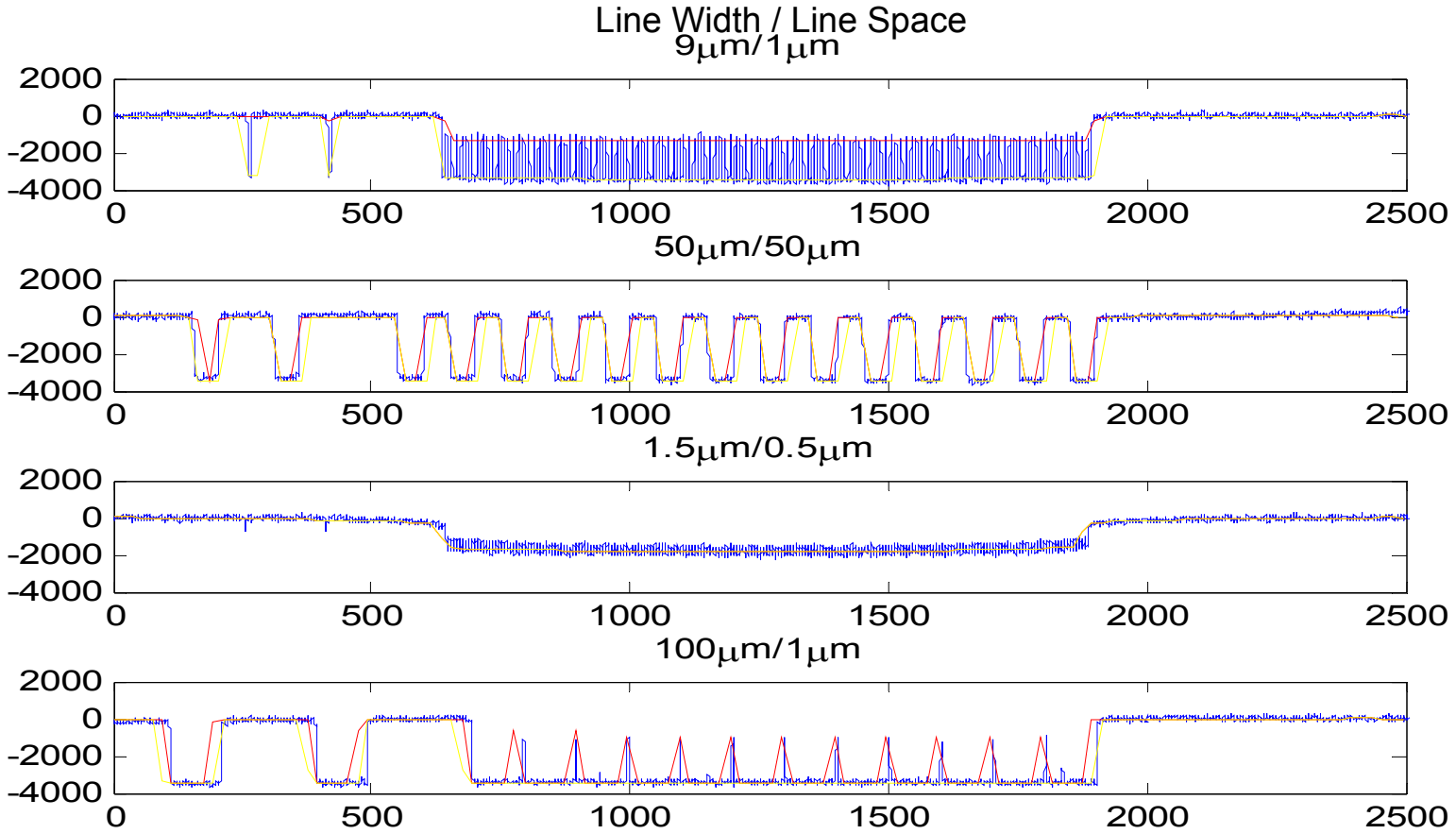


Pattern Density Map (%)



Line Width Map (μm)

ECD Chip-Scale Model: Calibration (2)



Experiment: HRP Scan Data (Blue)
Model: Grid Top (Red)
Model: Grid Bottom (Yellow)

ECD Chip-Scale Model: Calibration Summary

ECD Chip-Scale Modeling for MIT SEMATECH 854 M1

Wafer	Electroplated Cu Thickness (Å)	Array Height Error (Å)	Effective Step Height Error (Å)	Field Copper Thickness Error (Å)
CPT104-01	6938	**157**	**148**	**83**
CPT115-04	8611	**252**	**285**	**86**
CPT105-01	9855	**243**	**291**	**98**
CPT115-07	12668	**250**	**378**	**89**

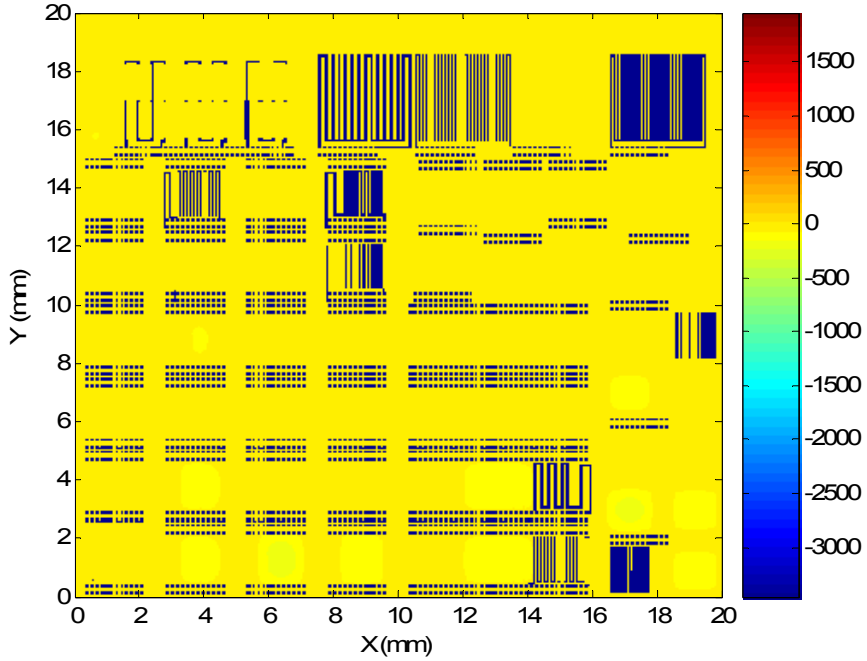
Previous model (Park):

- Semi-physics Model
- Surface Response Model
  - Over-fitting
  - Fixed Copper Thickness
  - Weak in Random Layout
- RMS Error: 200 – 400 Å

New model:

- Physics-based Model
- Time-stepped Model
  - Limited Fitted Parameters
  - Various Copper Thickness
  - Good in Random Layout
- RMS Error: 80 – 150 Å

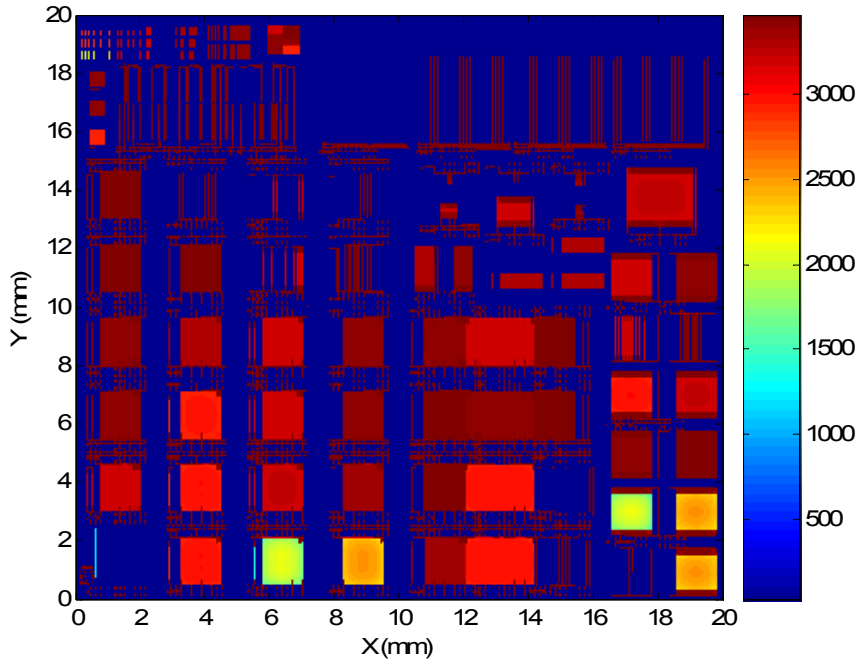
ECD Chip-Scale Model: Simulation (1)



(Relative) Envelope map (Å)

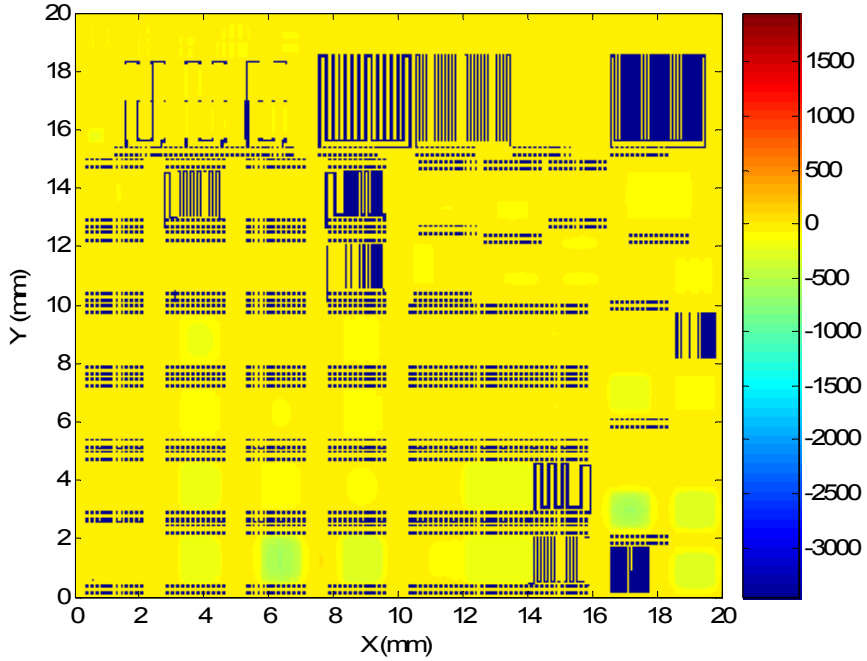
- Based on model fit, we can simulate and visualize the time evolution for the full chip layout

Effective step-height map (Å)



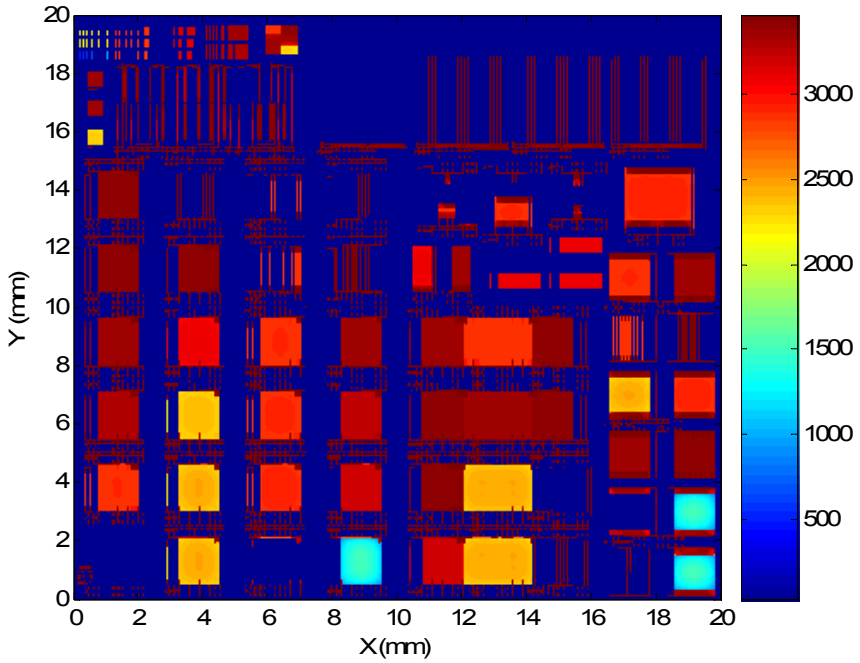
Chip-Scale ECD Modeling at t=10 sec

ECD Chip-Scale Model: Simulation (2)



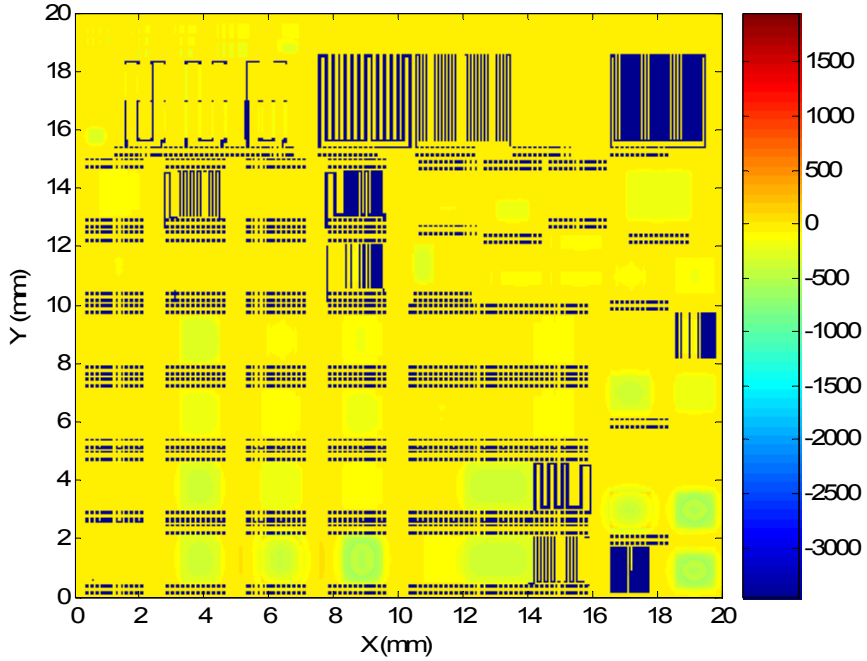
(Relative) Envelope map (Å)

Effective step-height map (Å)



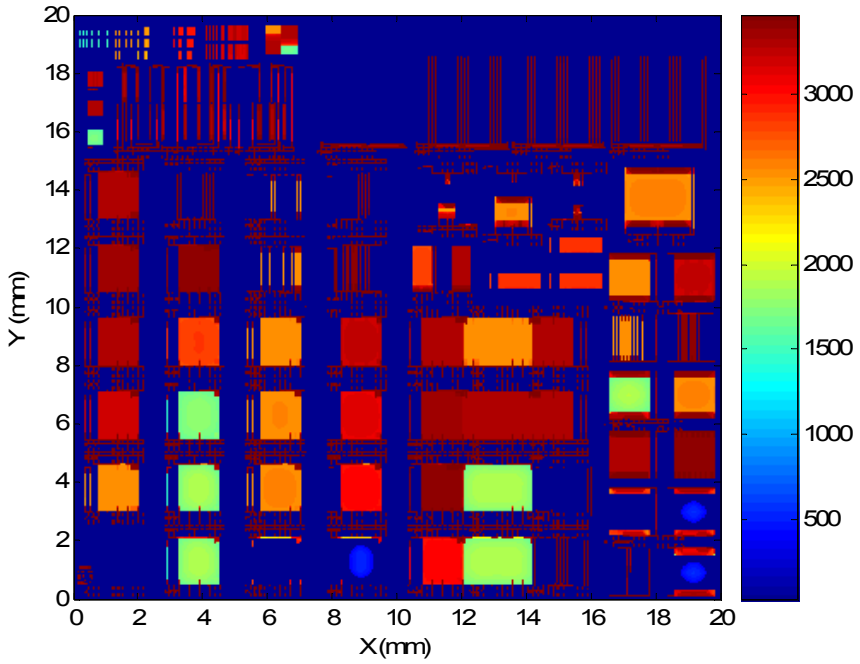
Chip-Scale ECD Modeling at t=20 sec

ECD Chip-Scale Model: Simulation (3)



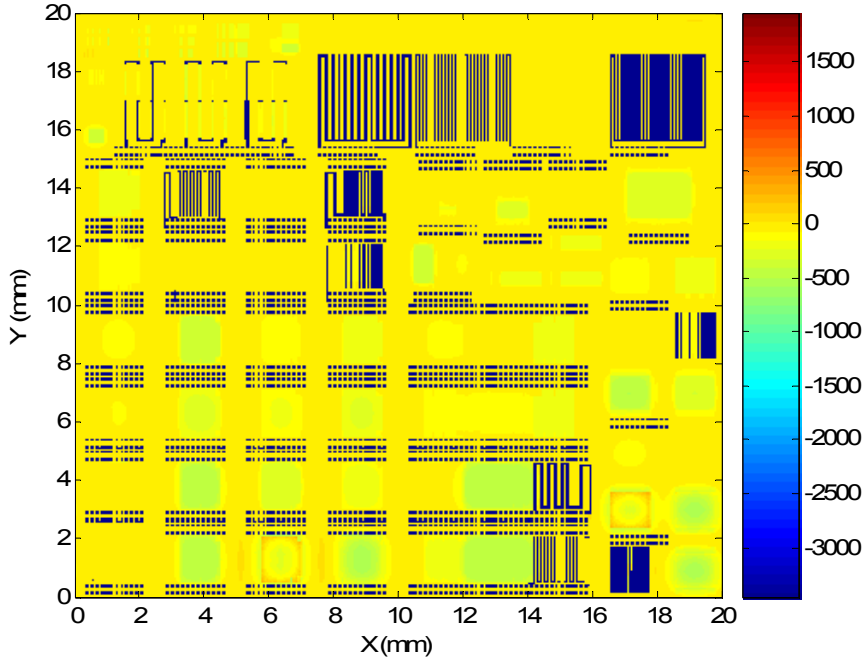
(Relative) Envelope map (Å)

Effective step-height map (Å)



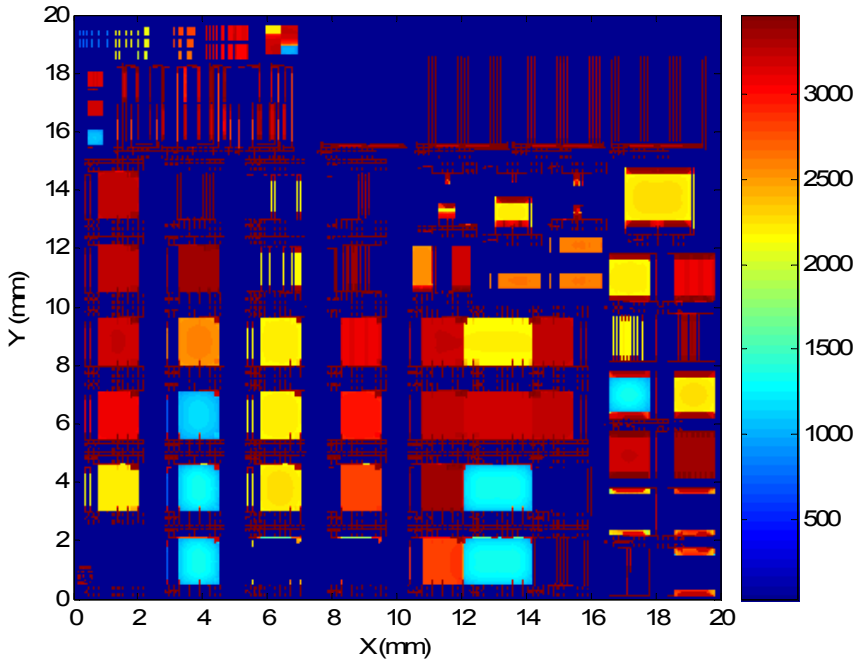
Chip-Scale ECD Modeling at t=30 sec

ECD Chip-Scale Model: Simulation (4)



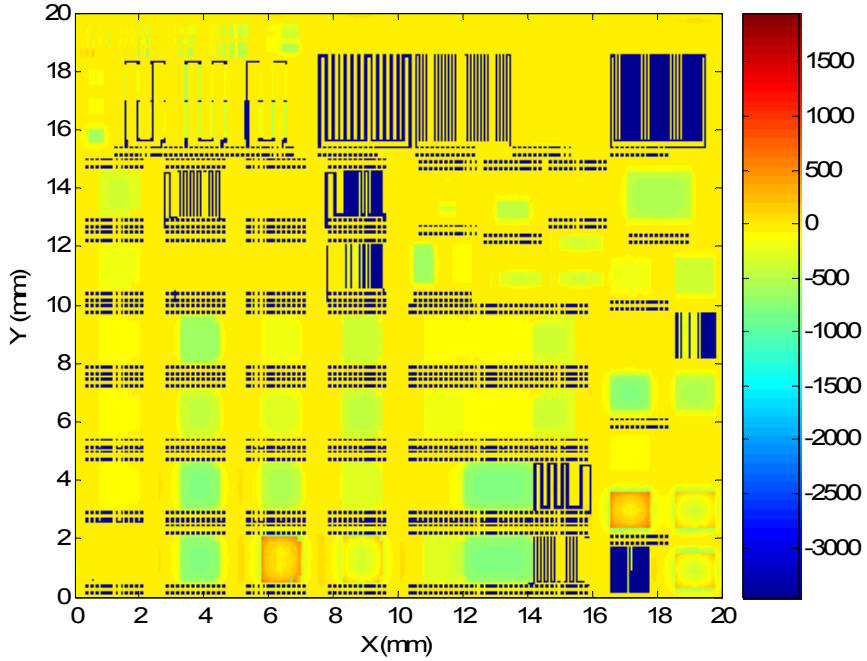
(Relative) Envelope map (Å)

Effective step-height map (Å)



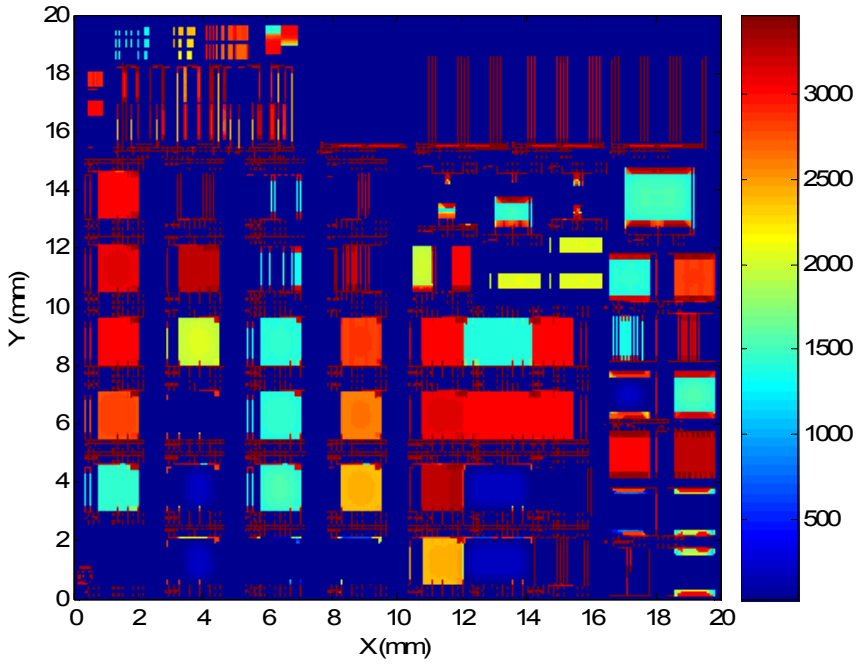
Chip-Scale ECD Modeling at t=40 sec

ECD Chip-Scale Model: Simulation (5)



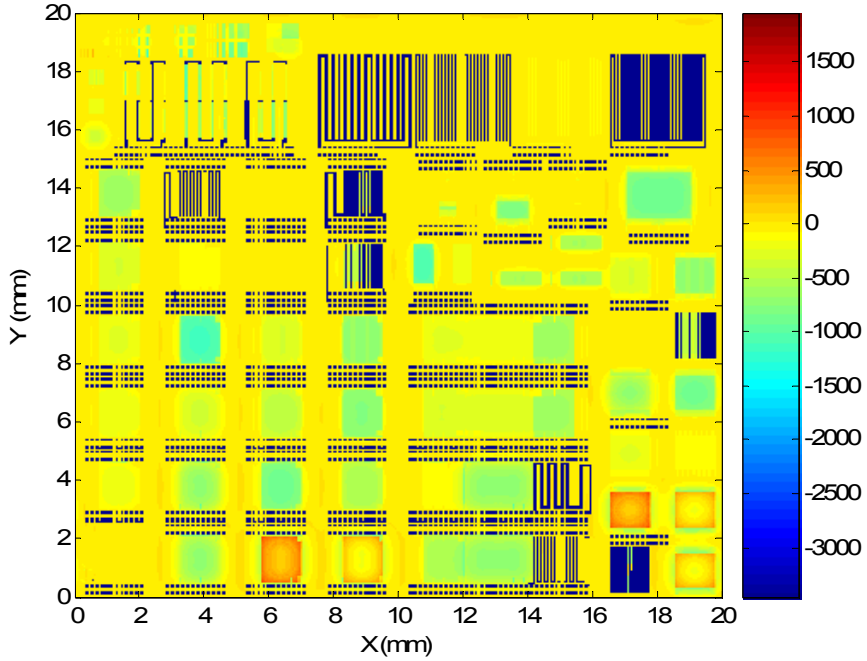
(Relative) Envelope map (Å)

Effective step-height map (Å)



Chip-Scale ECD Modeling at t=60 sec

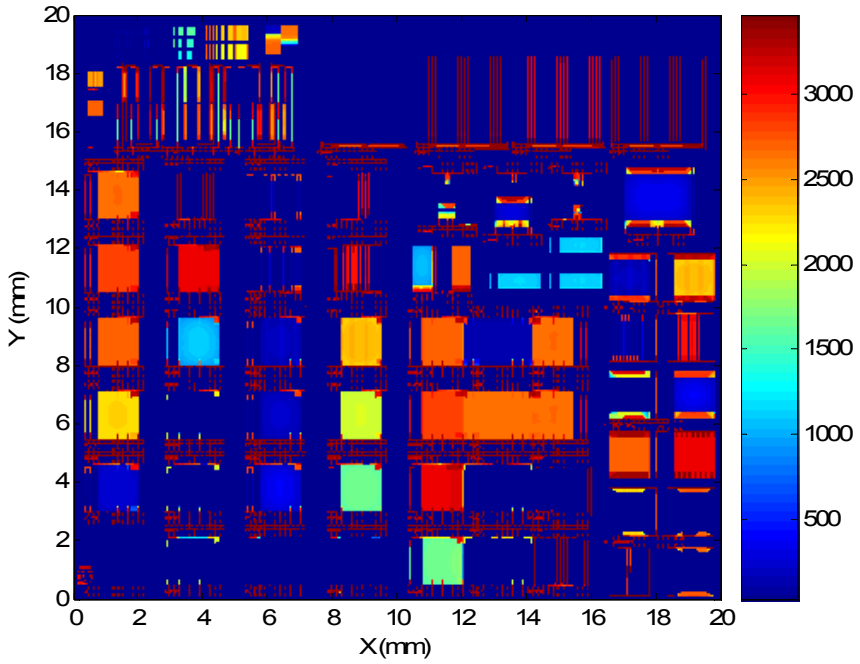
ECD Chip-Scale Model: Simulation (6)



(Relative) Envelope map (Å)

- Substantial topography from ECD to be planarized by CMP

Effective step-height map (Å)



Chip-Scale ECD Modeling at t=100 sec

ECD Chip-Scale Model: Summary

- A chip-scale ECD model is developed by incorporating the effective and proved feature-scale model. The additive competitive absorption and accumulation/dilution due to surface area change are considered by reasonable simplification.
- Edge effect is identified and addressed in this model.
- This model can accurately capture the electroplated copper surface height variation in the ordinary process window used in the semiconductor industry.
- The layout extraction and the two-dimension implementation in the model make it possible to process any feature size and shape.
- The pattern dependent pre-electroplating topography from the previous processes of the underlying level, especially CMP, has been concluded no significant contribution to the pattern dependency of the following ECD process.
- Seamless integration with CMP model for the ECD/CMP process integration and optimization, layout screening and dummy design.

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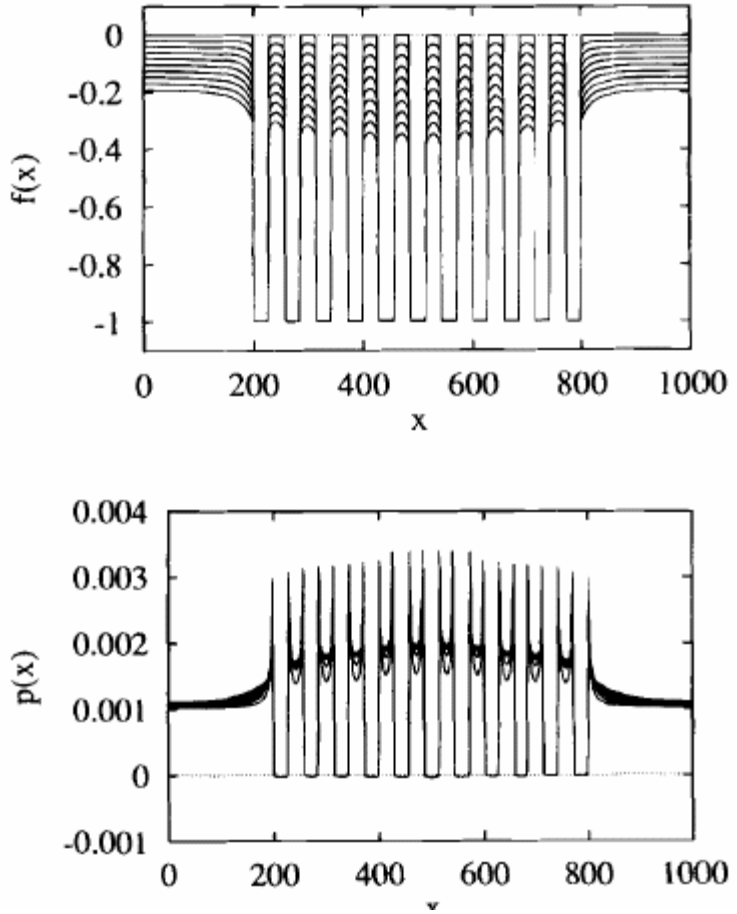
CMP Chip-Scale Model: Contact Wear Model Review (1)

Chekina's Model

- Relates localized pad deflection *w(x,y)* to localized pressures *p(x,y)*

$$w(x,y) = \frac{(1-\nu^2)}{\pi E}\int_{\omega} \frac{p(\xi,\eta)}{\sqrt{(x-\xi)^2+(y-\eta)^2}} d\xi d\eta$$

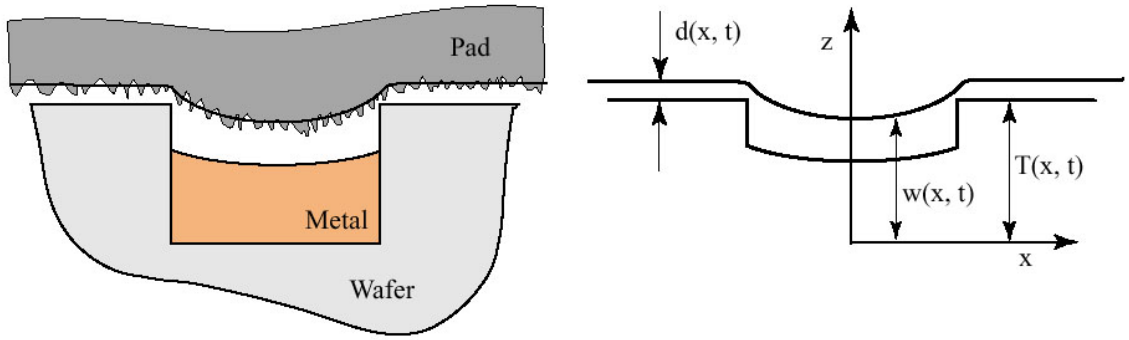
- Surface boundary computation is more efficient that volume finite element approach, but is still prohibitive for chip-scale simulation



Shape Evolution (Top) and Pressure Evolution (Bottom) in Polishing a Line Array Made of the Same Materials

O. G. Chekina et al., Journal of the Electrochemical Society, vol. 145, no. 6, pp. 2100–2106, June 1998.

CMP Chip-Scale Model: Contact Wear Model Review (2)



Vlassak's Contact Wear Model in CMP

Key Assumptions:

- Asperities with a given height exponential distribution
- Sphere Asperities

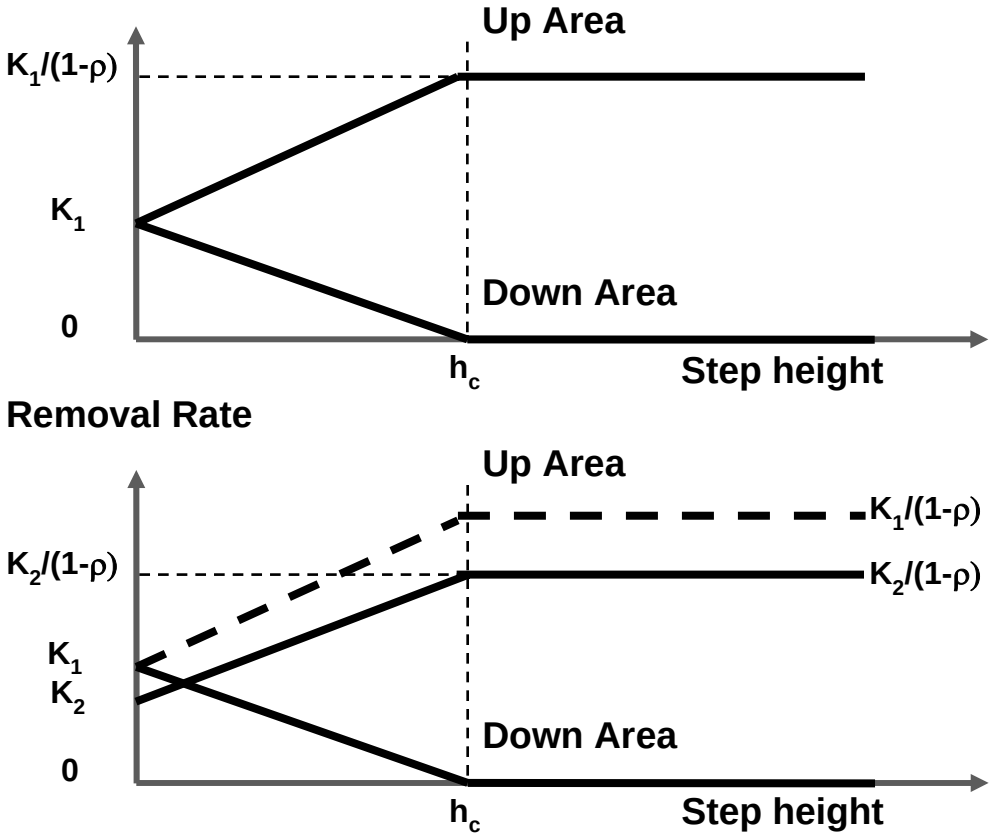
$$P(z) = \frac{1}{2\sigma}\exp\left(-\frac{|z|}{\sigma}\right)$$

$$p(x,t) = \frac{4}{3\sqrt{\kappa}}\frac{E}{1-\nu^2}\exp\left(-\frac{w(x,t)-T(x,t)}{\sigma}\right) \qquad for \quad w-T \geq 0$$

$$w(x,t) - C(t) = -\frac{2\left(1-\nu^2\right)}{\pi E}\int_{-L/2}^{L/2} p(s,t)\ln\left|\sin\frac{\pi(x-s)}{L}\right| ds$$

J. J. Vlassak, Mat. Res. Soc. Symp. Proc., vol. 671, paper M4.6, 2002.

CMP Chip-Scale Model: Density-Step-Height Model Review

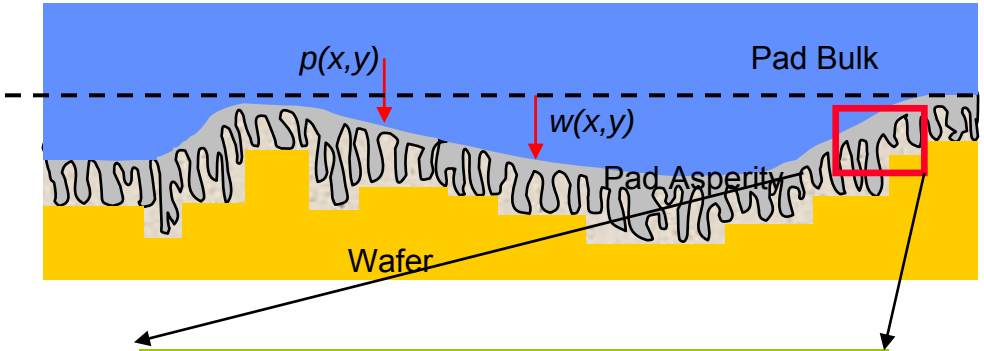


Removal rate (or pressure) vs. step height

CMP Chip-Scale Model: New Three-Part Framework (1)

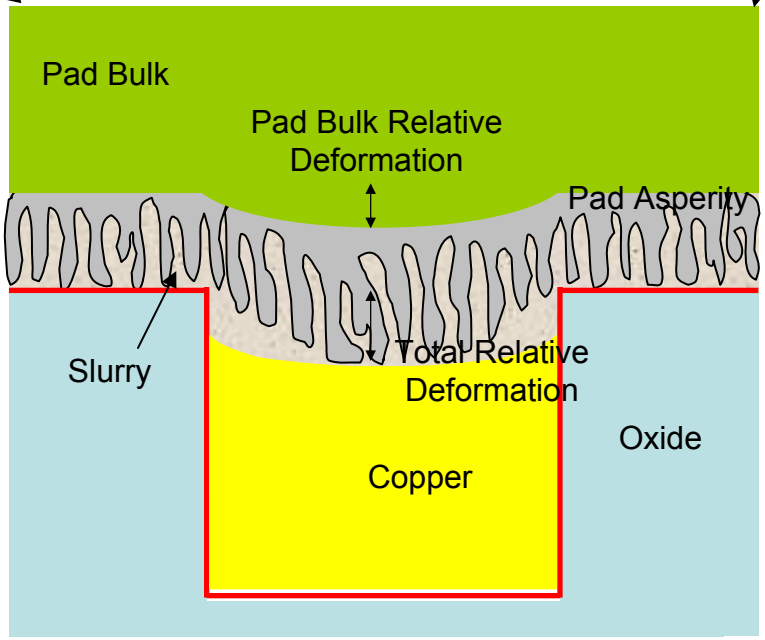
Contact Wear Model in the New Model Framework.

Part A: pad bulk pressure



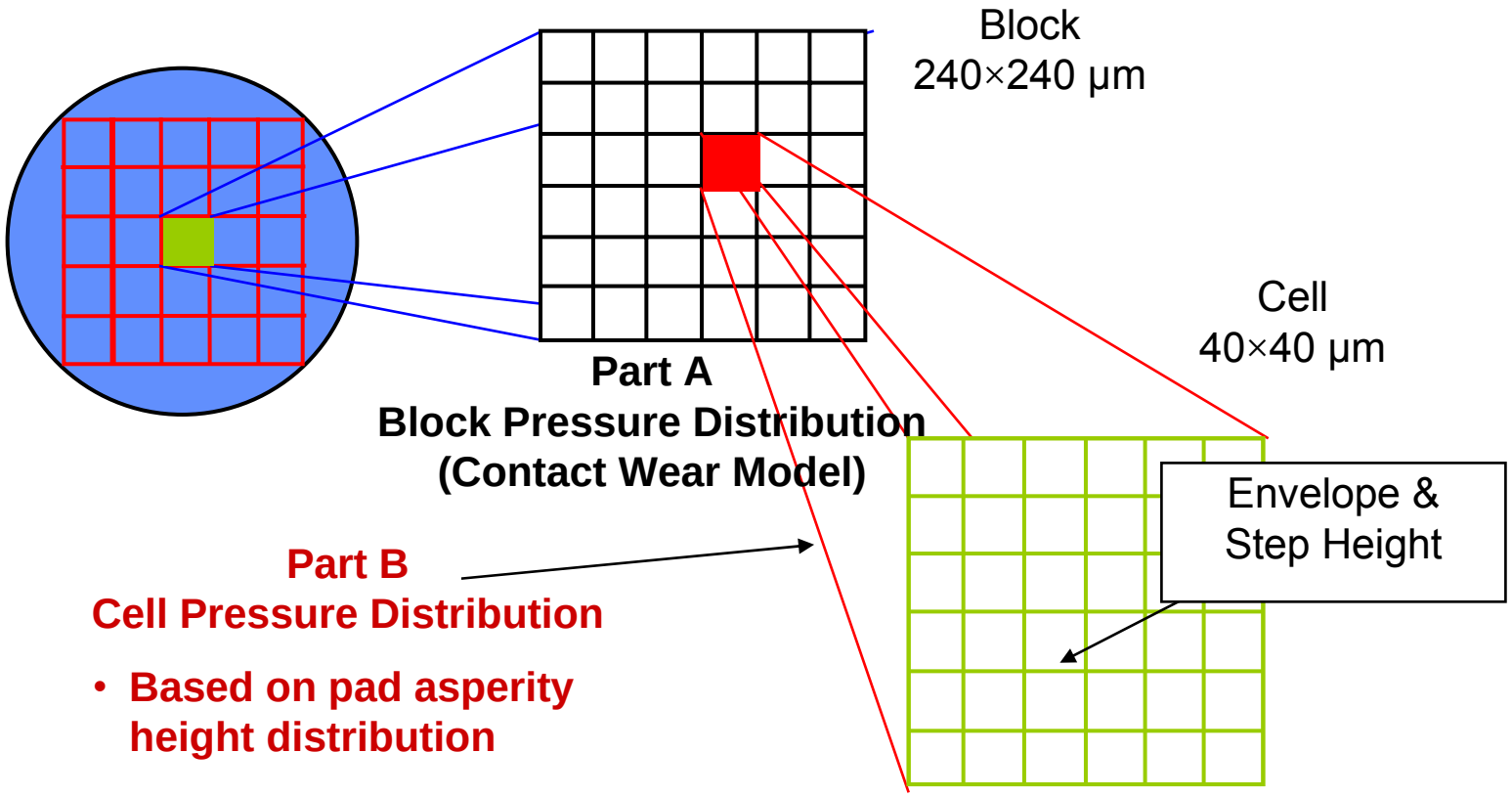
Part B: redistribute block pressure onto local cells

Part C: local pattern-density & step-height



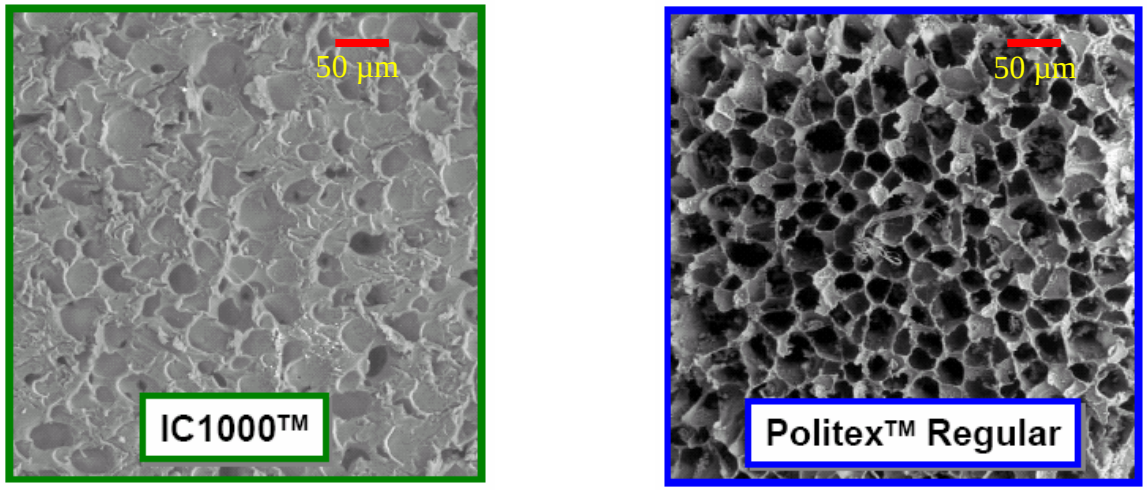
Pad and Asperity Deformation in the Feature Scale

CMP Chip-Scale Model: New Three-Part Framework (2)



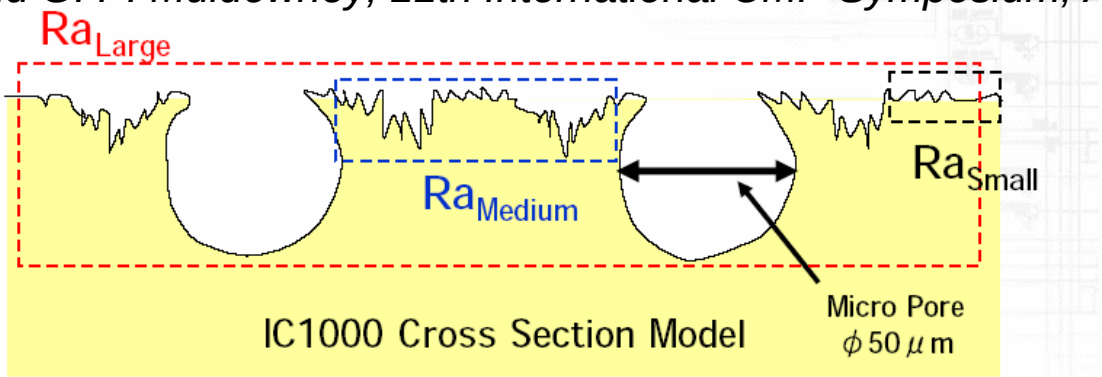
Three-Part Strategy in the New Model Framework

CMP Chip-Scale Model: Asperity Distributions



Rohm Haas IC-1000 and Politex Pad

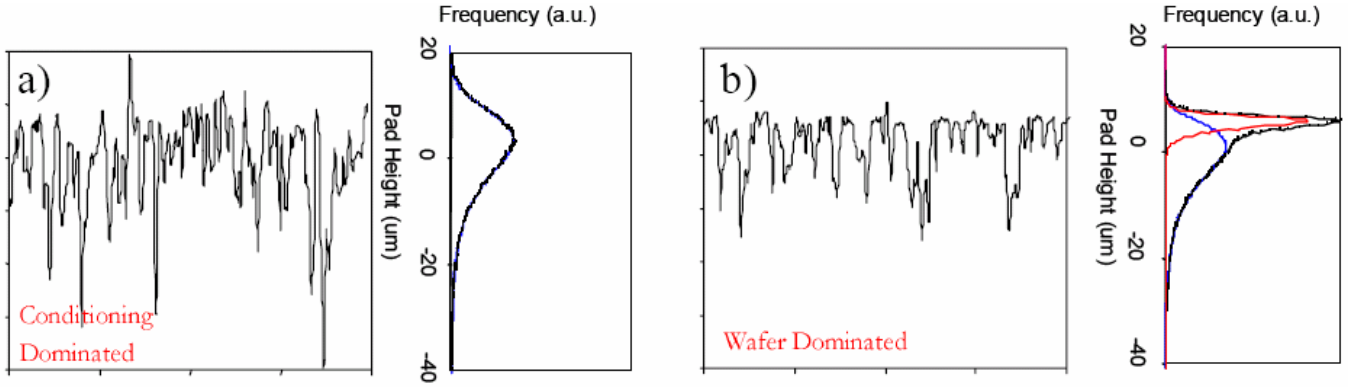
C. L. Elmufdi and G. P. Muldowney, 11th International CMP Symposium, August 2006.



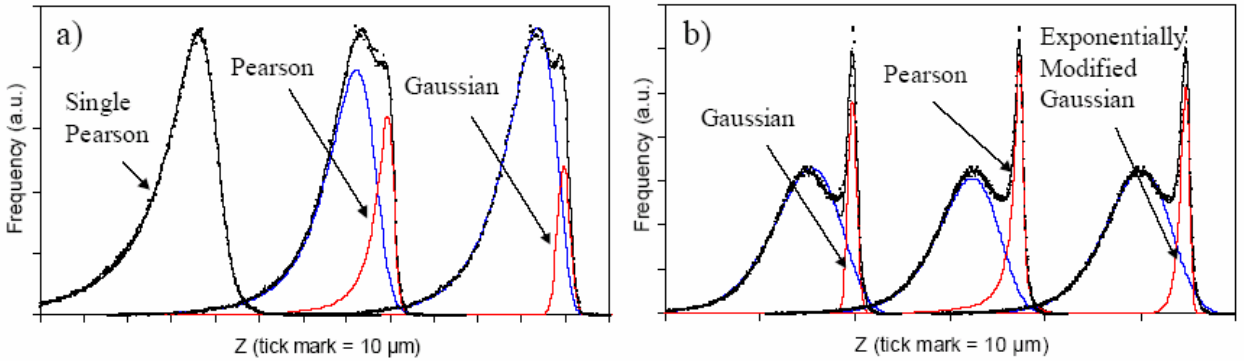
IC-1000 Pad Hierarchical Roughness

M. M. Kinoshita and Y. Matsumura, NSF/SRC Engineering Research Center, Annual Retreat, Stanford University, August 2004.

CMP Chip-Scale Model: Asperity Height Distribution



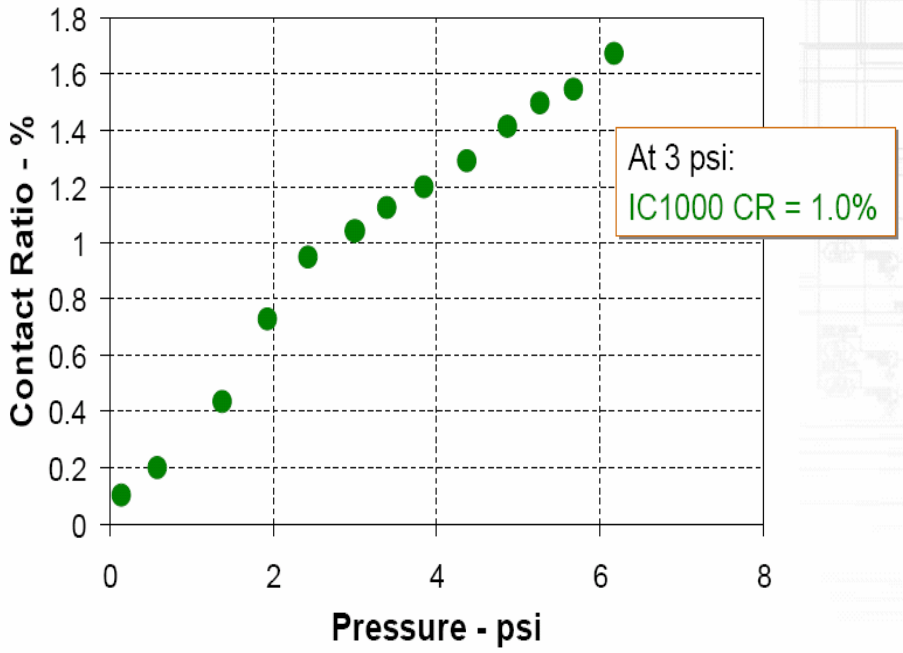
(a) Fully Conditioned (b) Wafer Dominated (Glazed)
IC 1000 Pad Surface Representative Line Scans
and Pad Height Probability Distributions



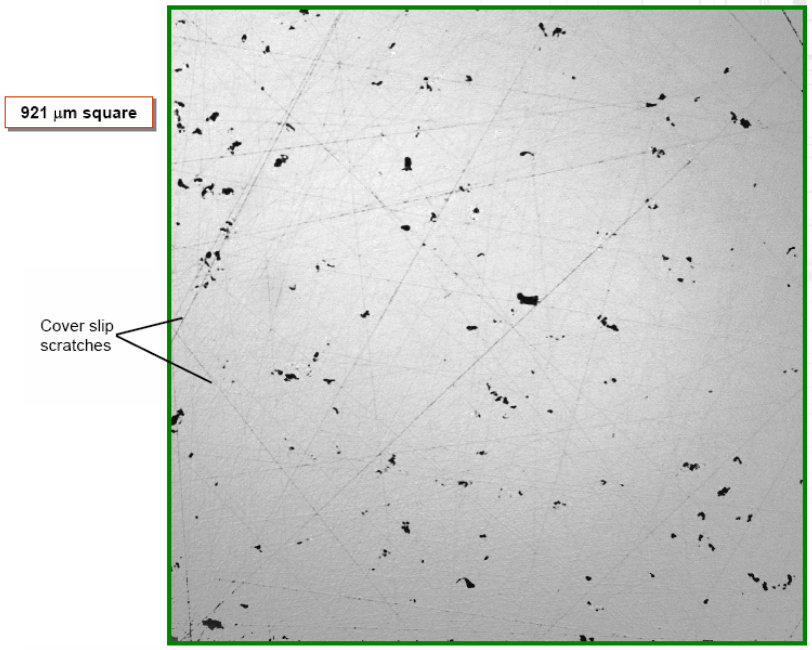
Examples of the Peak Fitting Procedure
Left: low deformation, Right: High Deformation

A. Lawing, Mat. Res. Soc., Symp. Proc. Vol. 732E, paper I5.3.1, San Francisco, CA, April 2002.

CMP Chip-Scale Model: Asperity Height/Size Distribution



Contact Area of IC 1000 Pad under Pressure

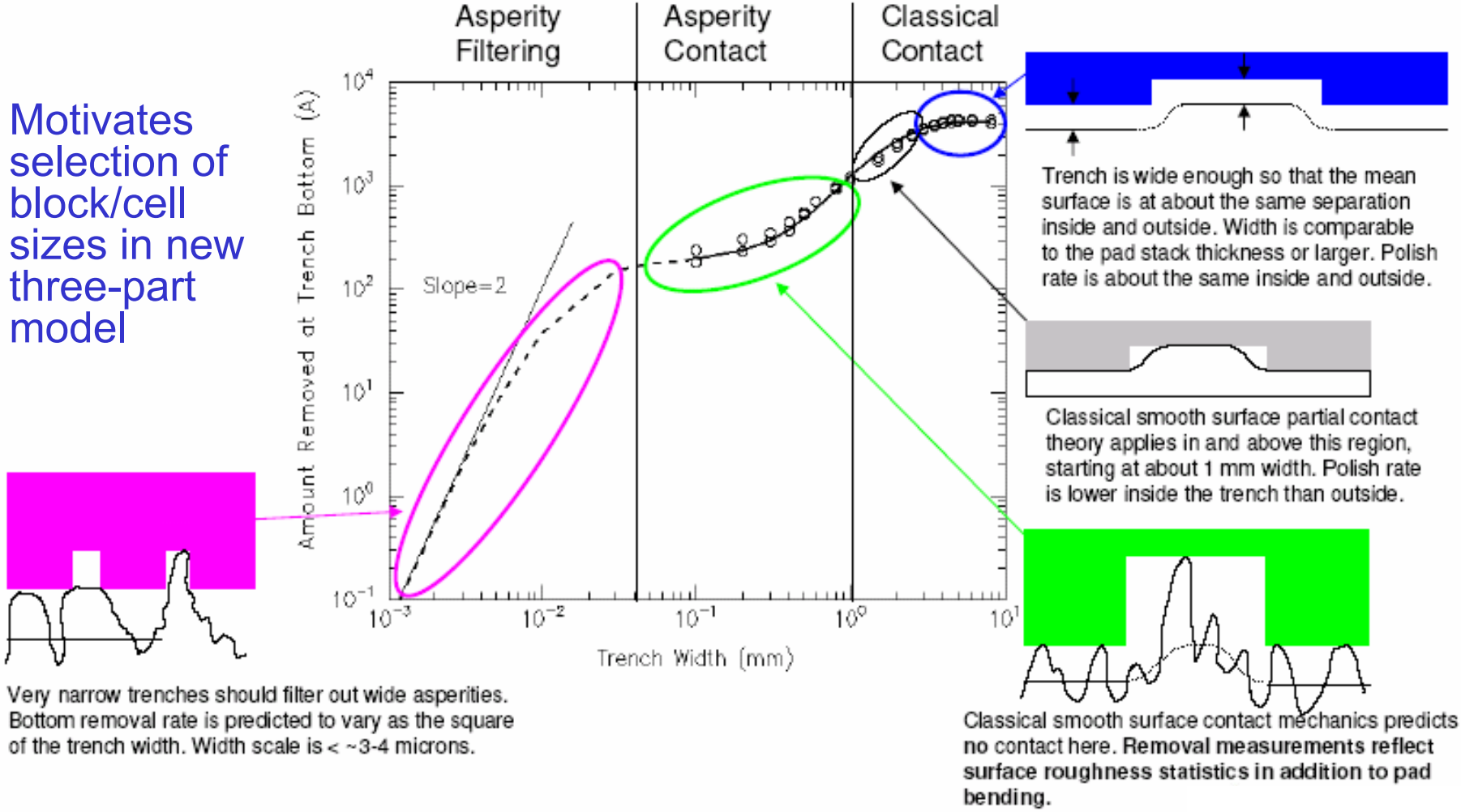


Contact Image of IC 1000 Pad under Pressure

C. L. Elmufdi and G. P. Muldowney, 11th International CMP Symposium, August 2006.

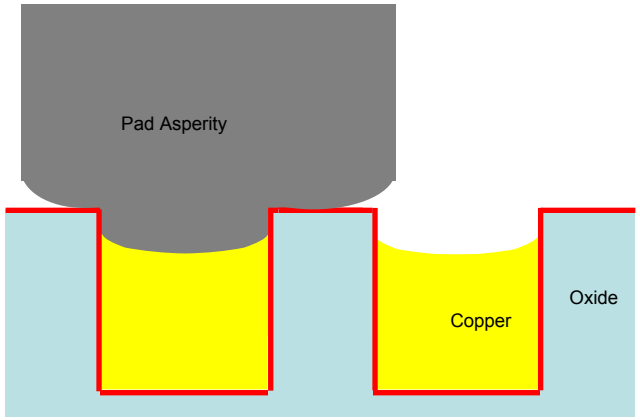
CMP Chip-Scale Model: Asperity Size Distribution

- Motivates selection of block/cell sizes in new three-part model

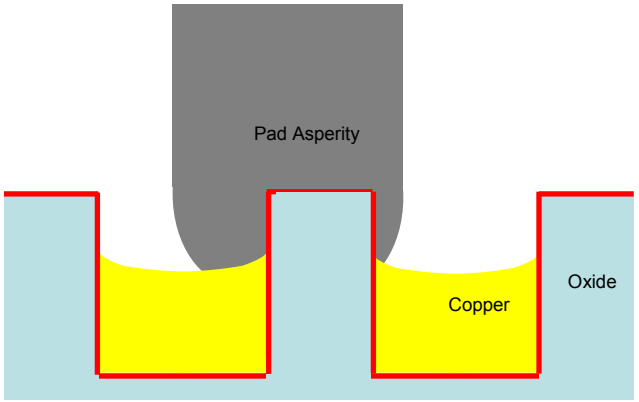


T. Merchant et al., AIChE, Invited Talk, November 2004.

CMP Chip-Scale Model: Updated Pattern-Step-Height Model (1)



Asperity Bending over the Whole Pitch



Asperity Bending over Line Space

- Model pressure ratios as a function of step height (*s*) and asperity size function *F*

local pattern density

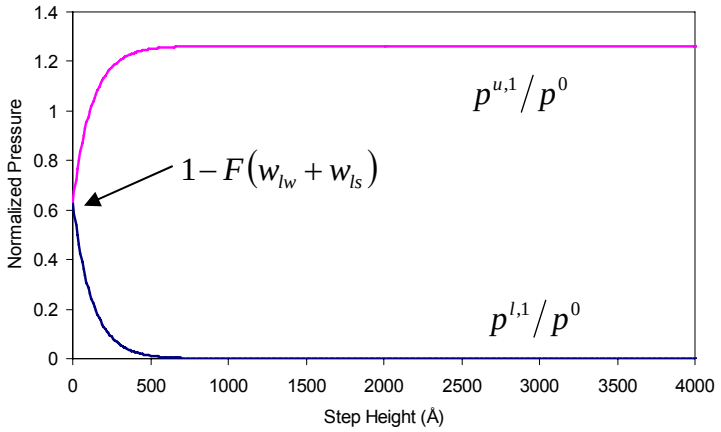
$$p^{u,1} / p^{0} = \left(1 - F\left(w_{lw} + w_{ls}\right)\right)\left[\left(1 - D_{cell} \exp\left(-s / h_c\right)\right) / \left(1 - D_{cell}\right)\right]$$

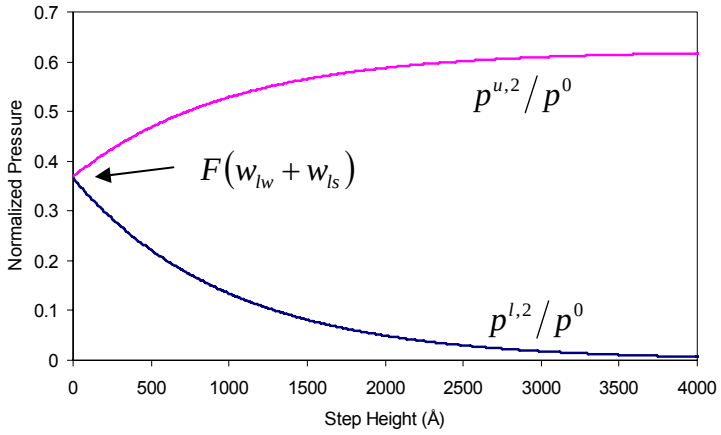
$$p^{l,1} / p^{0} = \left(1 - F\left(w_{lw} + w_{ls}\right)\right)\exp\left(-s / h_c\right)$$

step height

asperity contact size function

CMP Chip-Scale Model: Updated Pattern-Step-Height Model (2)

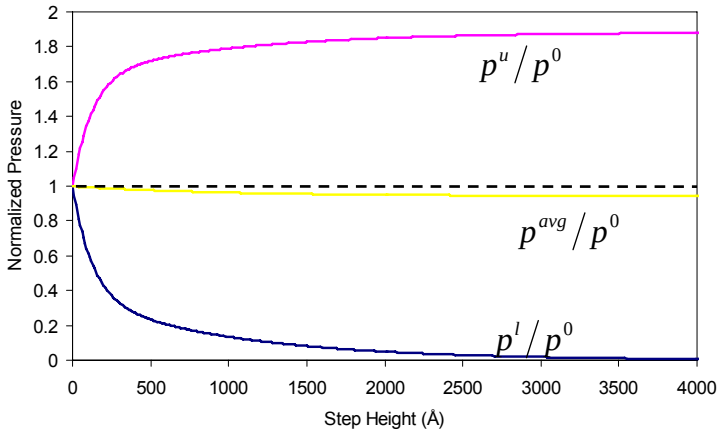




Pressure contribution from large asperities

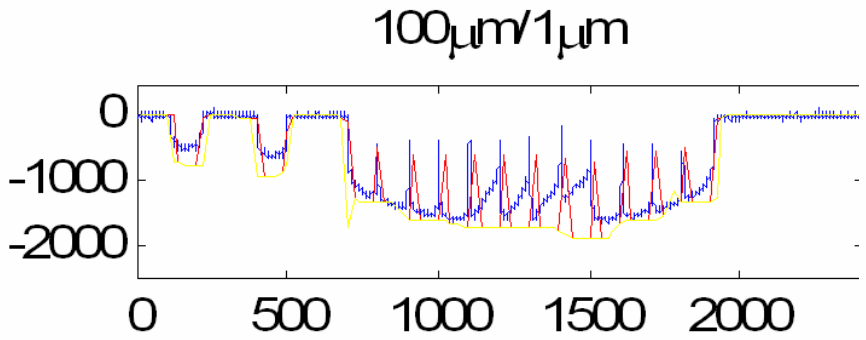
+

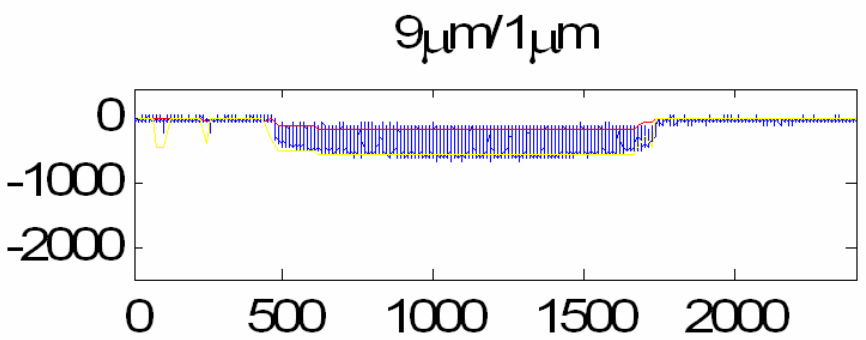
Pressure contribution from small asperities

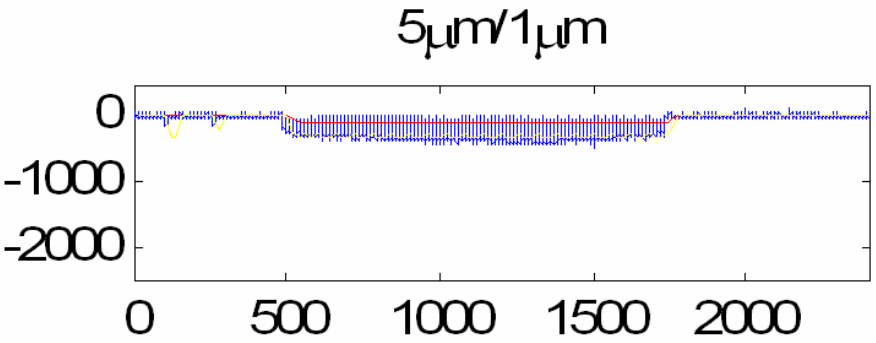


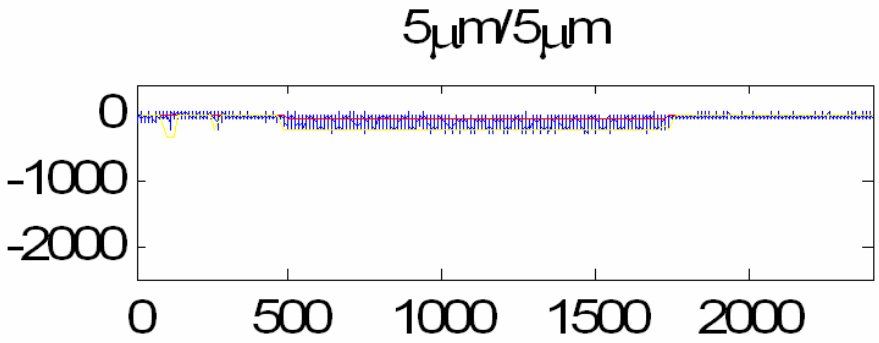
= Total pressure vs. step height

New CMP Model Results









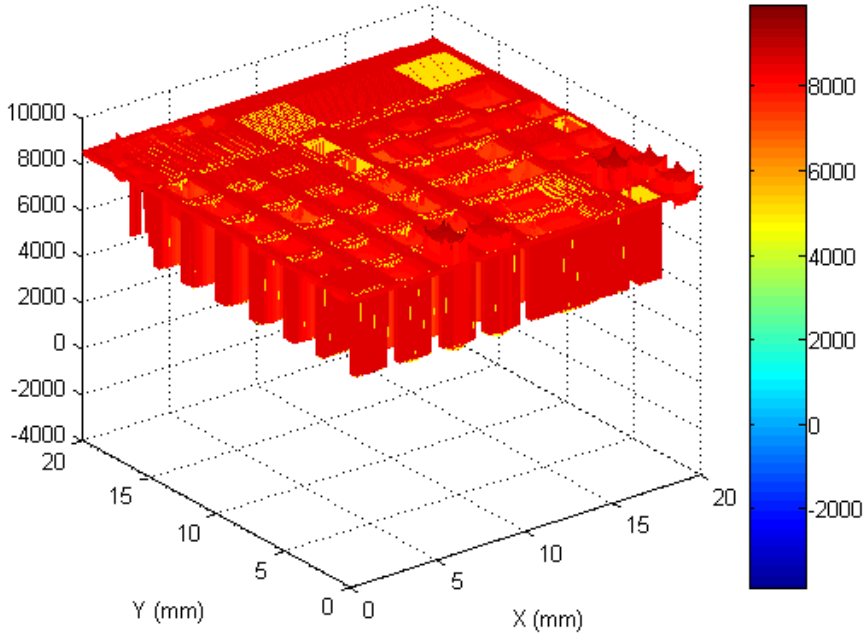
Previous model (Tugbawa):

- Two-Part or One-Part Framework
- No Pad Asperities Information
- Not Seamlessly Integrated with ECD Model
- RMS Error: 100 – 500 Å (Dishing/Erosion)

New model:

- Three-Part-Framework
- Pad Asperity Distributions
- Seamlessly Integrated With ECD Model
- RMS Error: 40 – 90 Å (Dishing/Erosion)

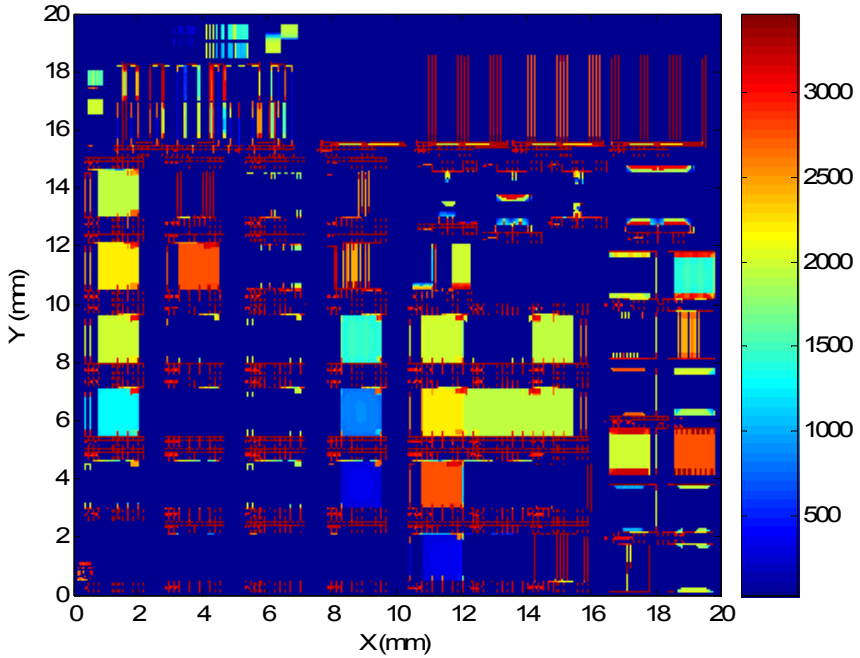
CMP Chip-Scale Model: Simulation (1)



Envelope map (Å)

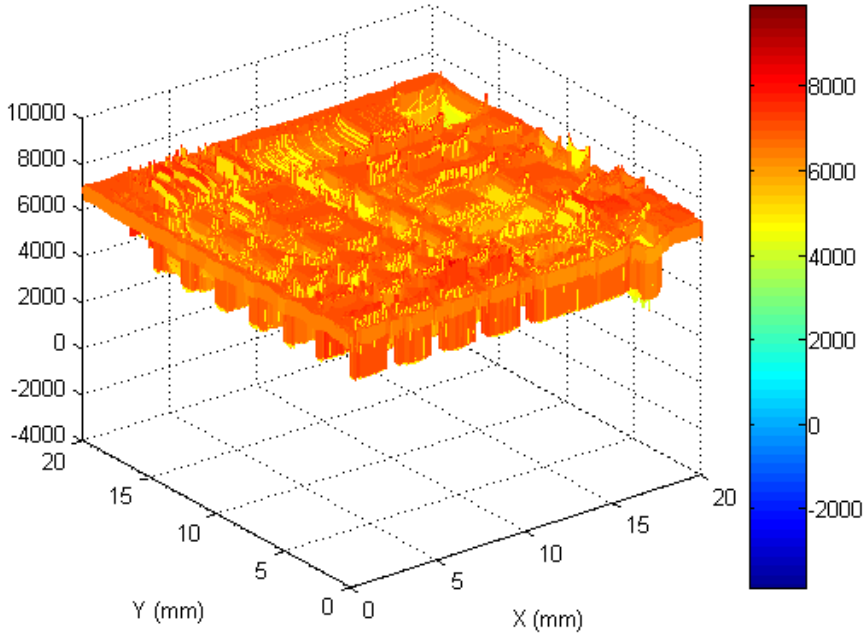
- Starting topography: simulation result from ECD model

Step height map (Å)



Chip-Scale CMP Modeling at t=0 sec

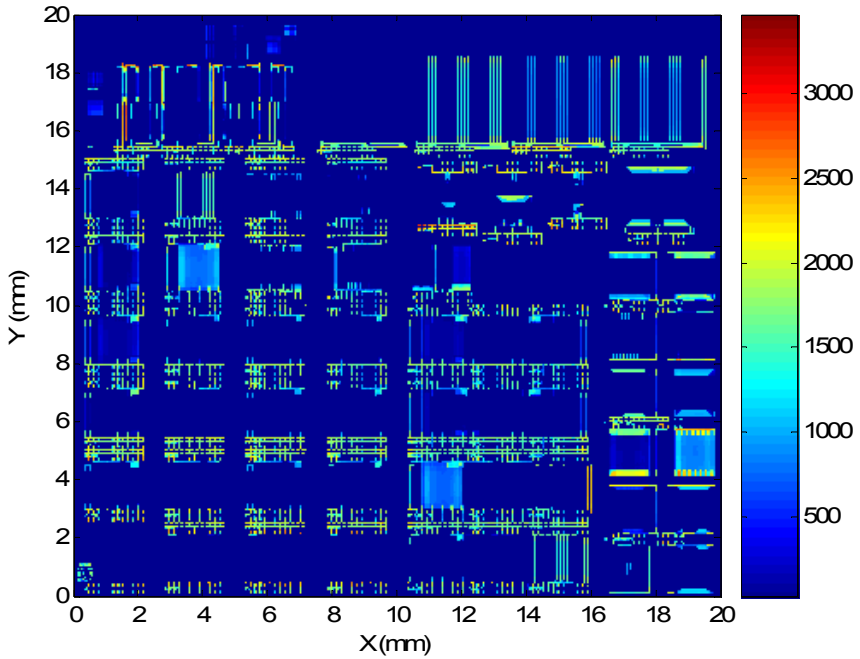
CMP Chip-Scale Model: Simulation (2)



Envelope map (Å)

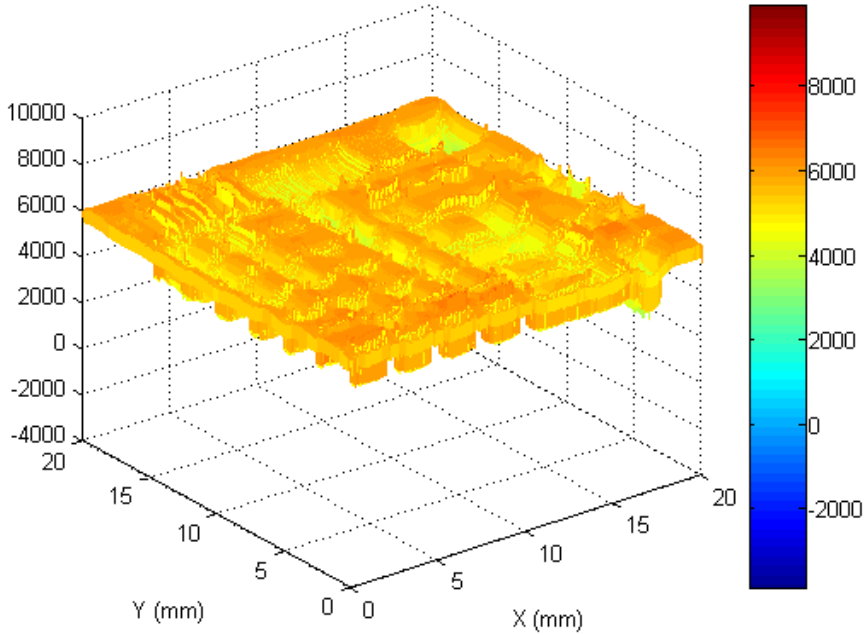
- Start of CMP simulation

Step height map (Å)



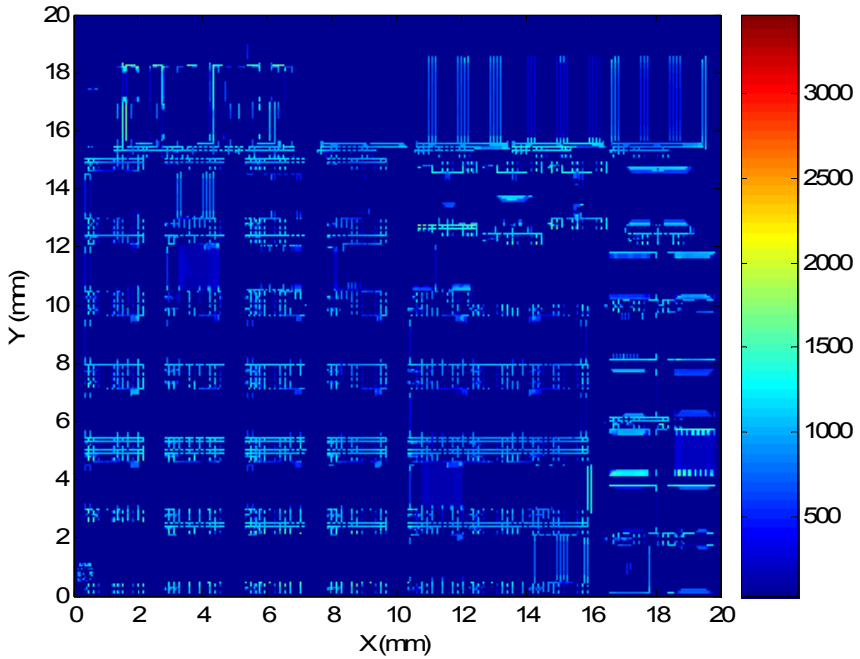
Chip-Scale CMP Modeling at t=10 sec

CMP Chip-Scale Model: Simulation (3)



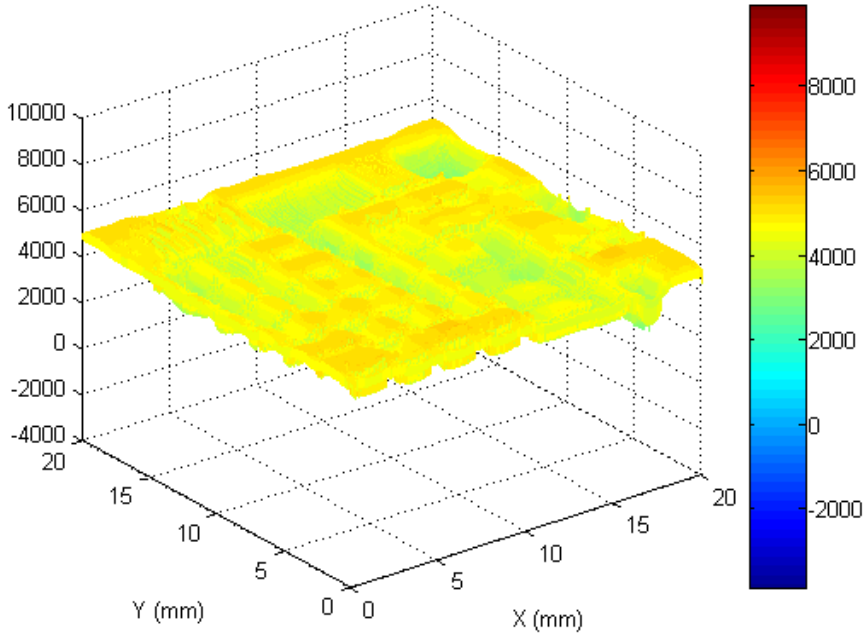
Envelope map (Å)

Step-height map (Å)



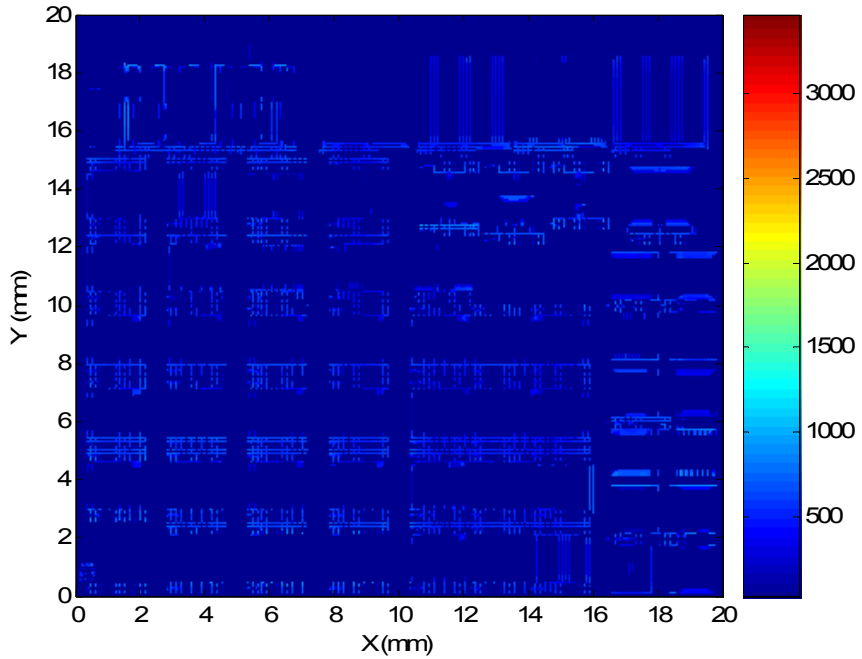
Chip-Scale CMP Modeling at t=20 sec

CMP Chip-Scale Model: Simulation (4)



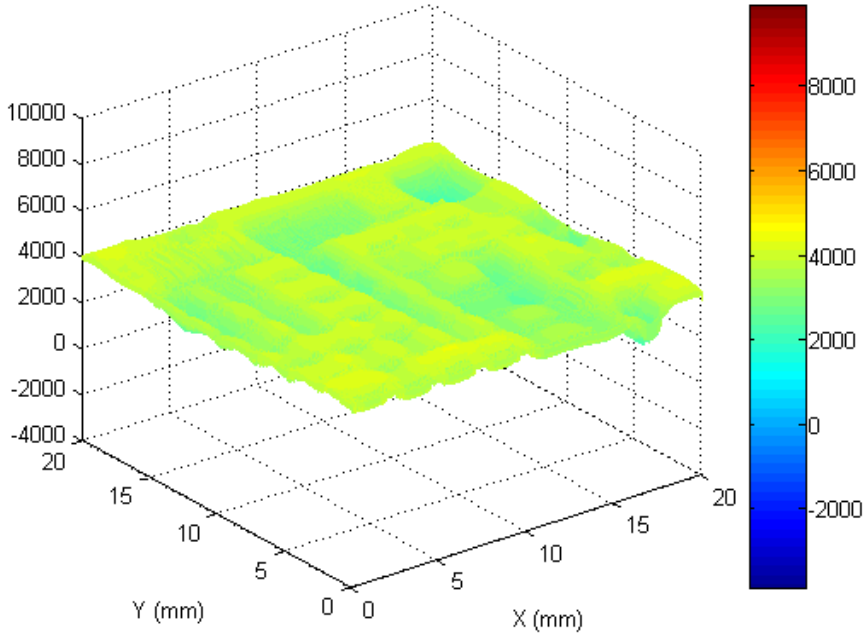
Envelope map (Å)

Step height map (Å)



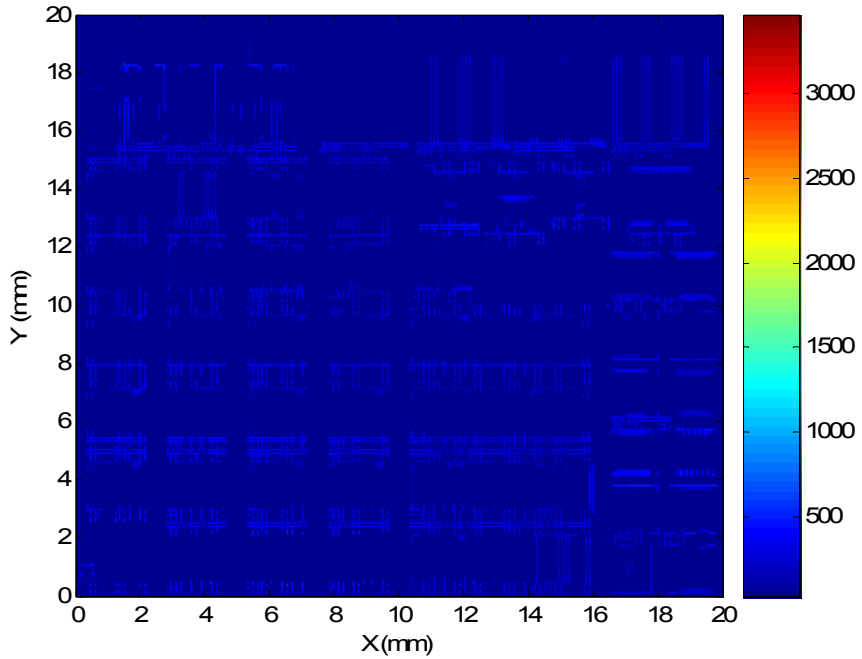
Chip-Scale CMP Modeling at t=30 sec

CMP Chip-Scale Model: Simulation (5)



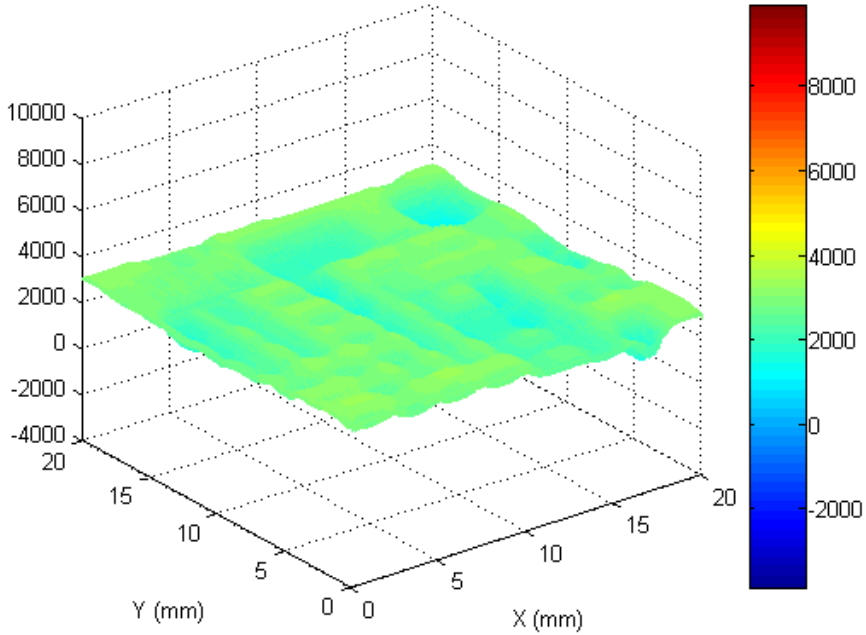
Envelope map (Å)

Step height map (Å)



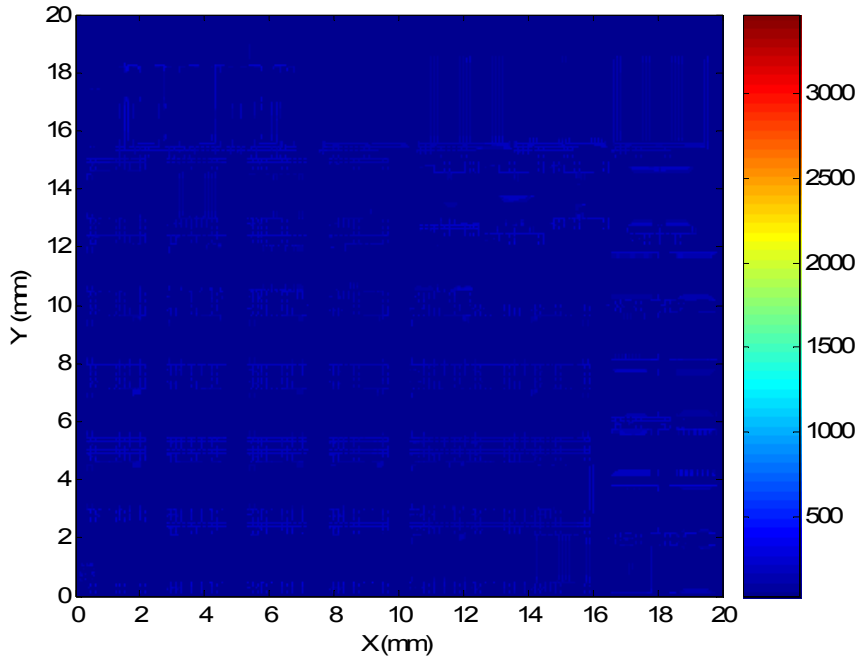
Chip-Scale CMP Modeling at t=40 sec

CMP Chip-Scale Model: Simulation (6)



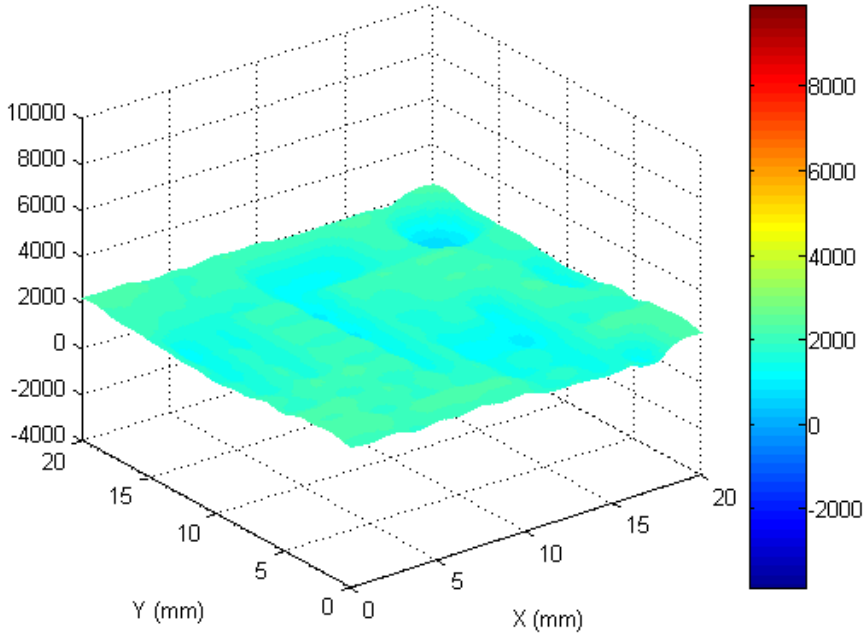
Envelope map (Å)

Step height map (Å)



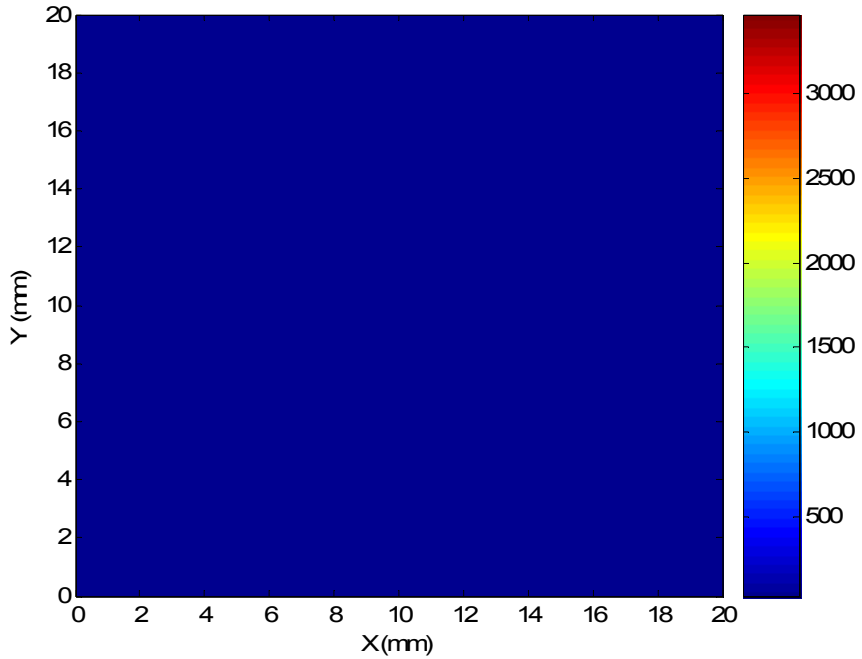
Chip-Scale CMP Modeling at t=50 sec

CMP Chip-Scale Model: Simulation (7)



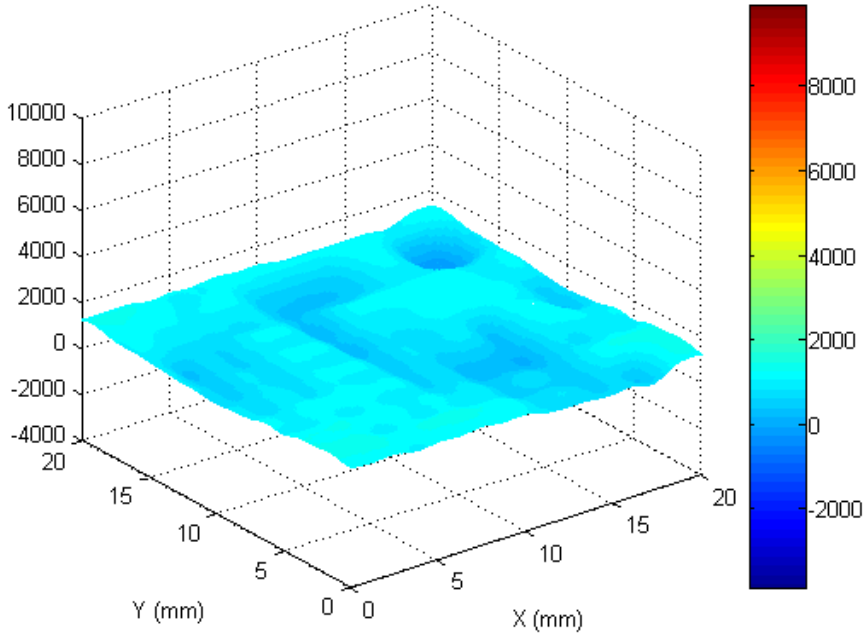
Envelope map (Å)

Step height map (Å)



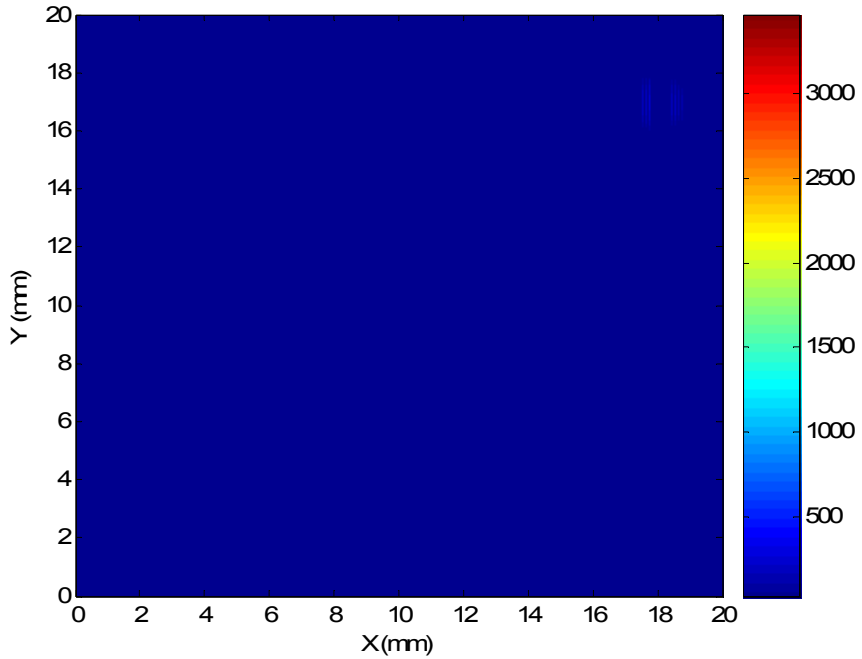
Chip-Scale CMP Modeling at t=60 sec

CMP Chip-Scale Model: Simulation (8)



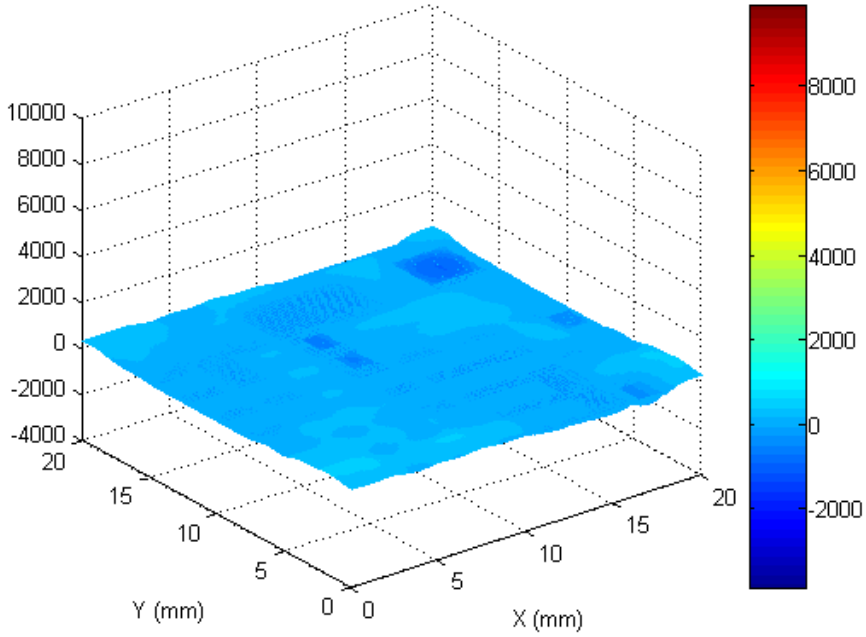
Envelope map (Å)

Step height map (Å)



Chip-Scale CMP Modeling at t=70 sec

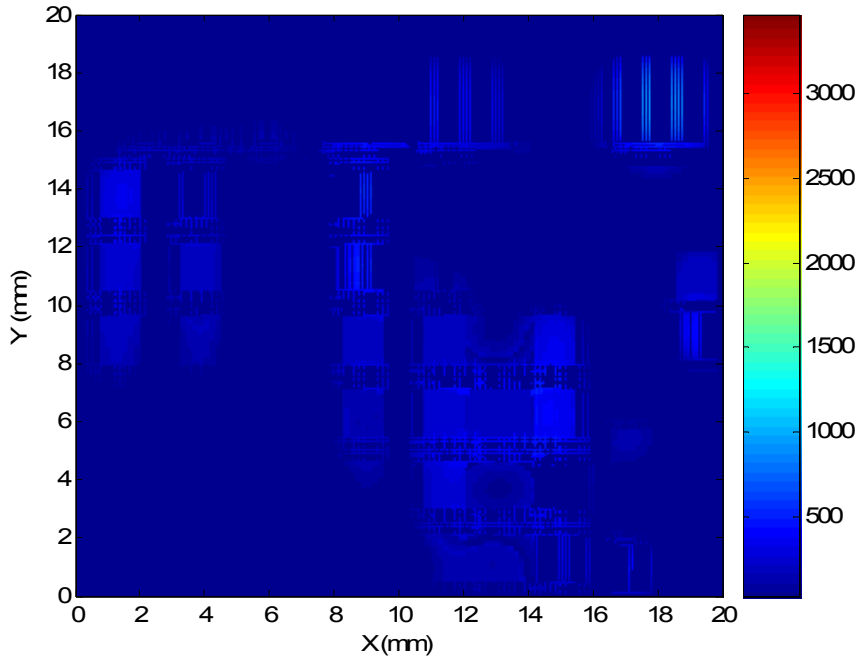
CMP Chip-Scale Model: Simulation (9)



Envelope map (Å)

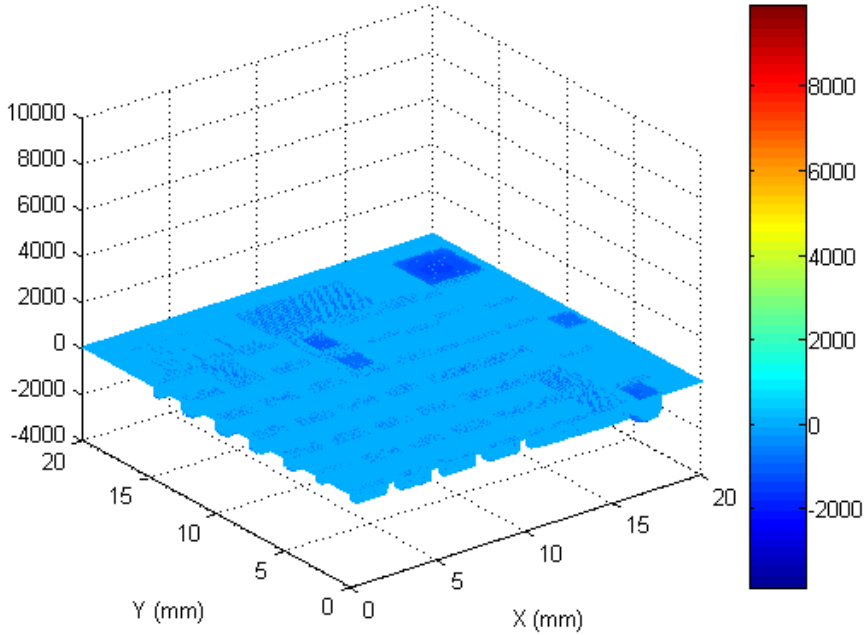
- Copper clearing to barrier and overpolishing

Step height map (Å)



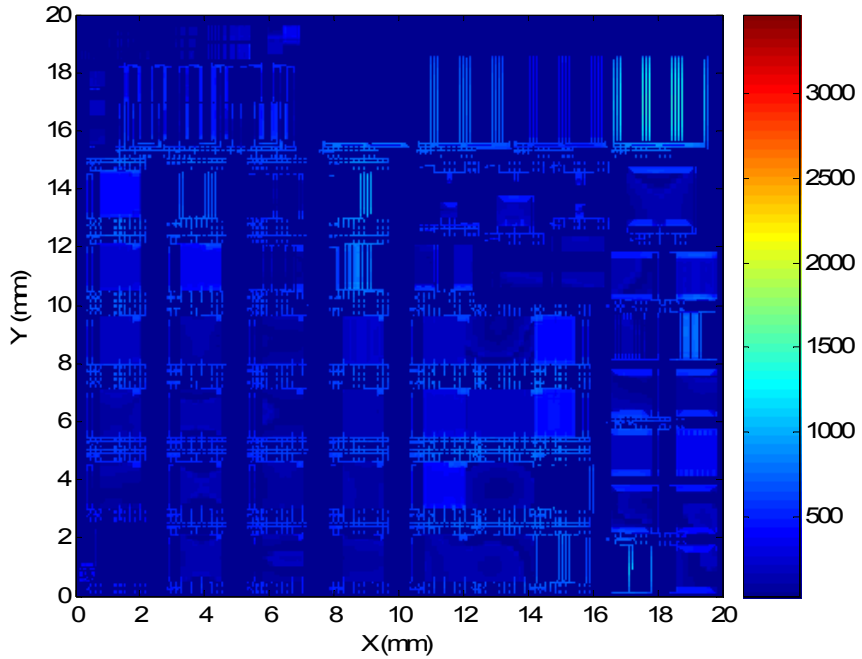
Chip-Scale CMP Modeling at t=80 sec

CMP Chip-Scale Model: Simulation (10)



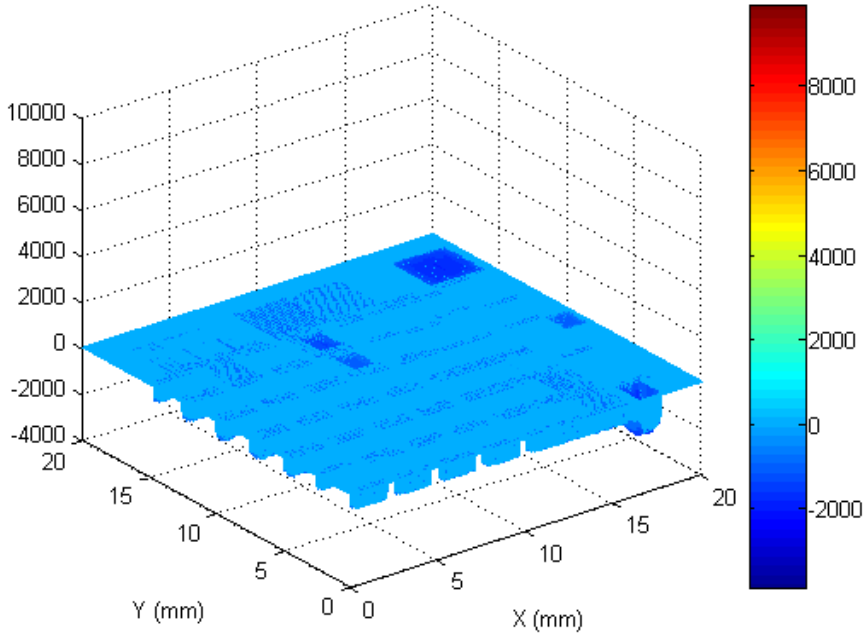
Envelope map (Å)

Step height map (Å)



Chip-Scale CMP Modeling at t=90 sec

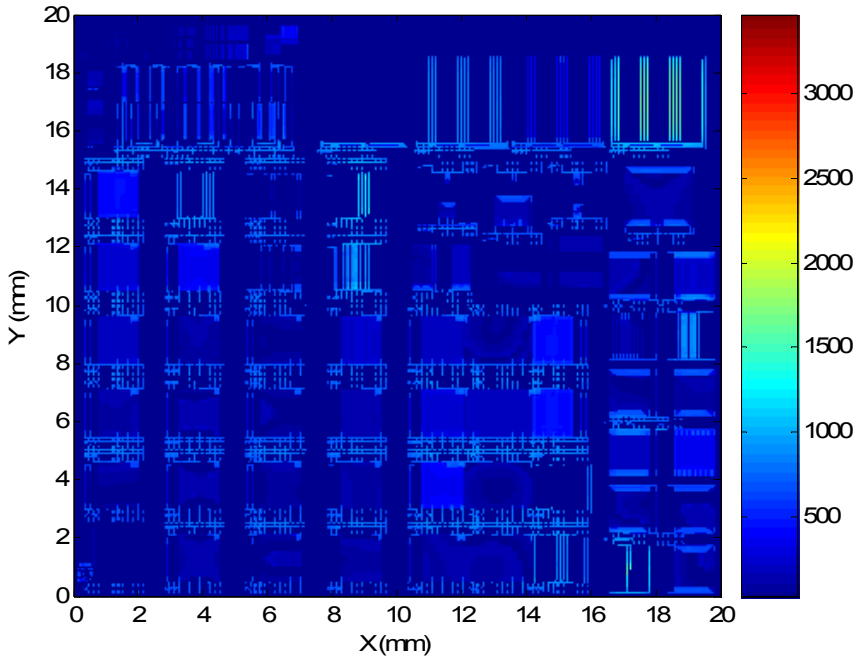
CMP Chip-Scale Model: Simulation (11)



Envelope map (Å)

- Final topography

Step height map (Å)



Chip-Scale CMP Modeling at t=100 sec

CMP Chip-Scale Model: Summary

- A new chip-scale CMP model incorporating asperity height and contact area size distributions is developed, and extended to the multi-level case.
- Good modeling accuracy without significant sacrifice in computation efficacy.
- A three-part modeling framework, has been developed that matches the hierarchical scale structure in the CMP process.
- The contact-wear model and the modified density-step-height model are seamlessly integrated.
- The different steps (bulk copper polish, copper over-polish, and barrier polish) at different metal levels, as well as the ECD process are seamlessly integrated.
- Temperature effect in the pad properties and slurry removal rate during copper polishing.
- Other pattern dependencies from other process in the multi-level copper metallization, such as etching and deposition, have to be modeled and incorporated into the integrated ECD/CMP model to fully capture the surface height variation in random layouts.

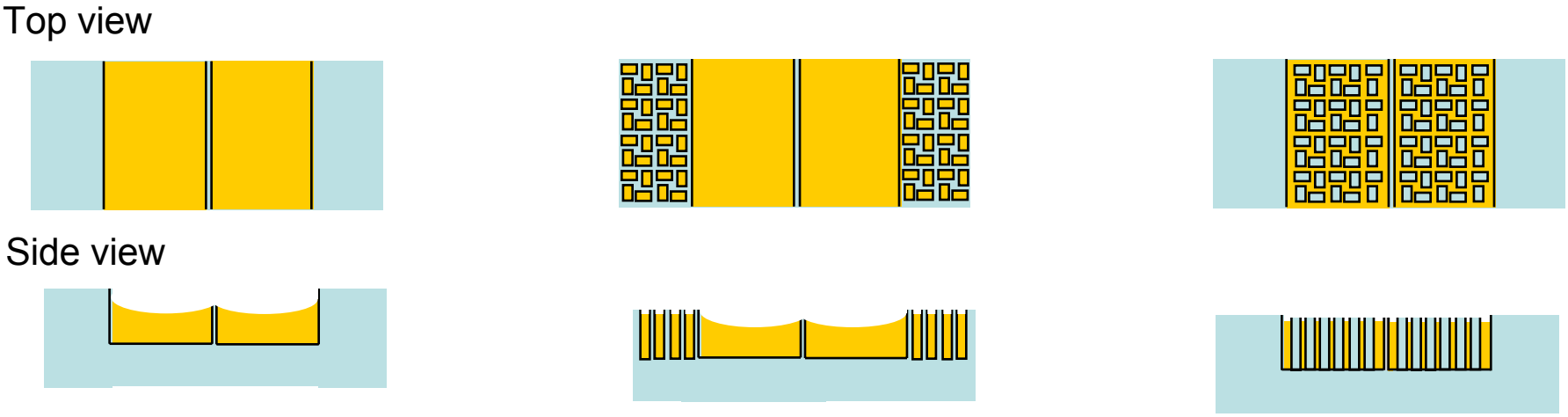
OUTLINE

- Motivation for Research
- ECD Chip-Scale Model
  - Model Review
  - New Model Framework
  - Calibration and Verification
  - Summary
- CMP Chip-Scale Model
  - Model Review
  - New Model Framework
  - Calibration and Verification
  - Summary
- Application
  - In-Pattern Dummy
  - Sensitivity Analysis
- Conclusion and Future Work

Application Objective

- Problems in Conventional Copper CMP
  - Low copper removal rate at low pressure compatible to low-K materials
  - Dishing and erosion problems
  - Competition from other planarization techniques, eg. ECMP
- Strategy to Extend Conventional CMP
  - Reduce the electroplated copper film thickness (1 times of trench depth)
  - Improve the slurry and polishing pad to increase the removal rate at low down force
  - High linear relative polishing velocity
  - Dummy fills!

Dummy Fill Strategies

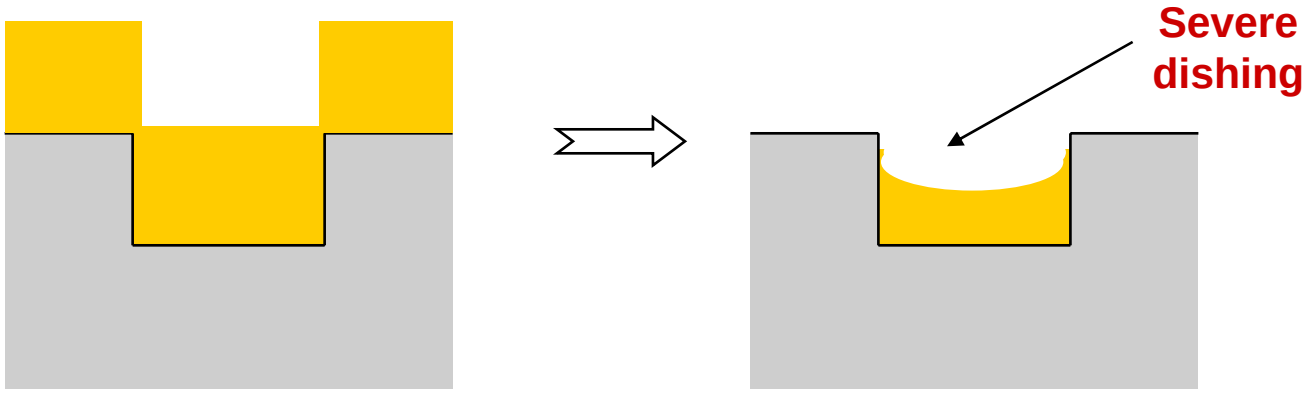


Between-pattern dummy fills

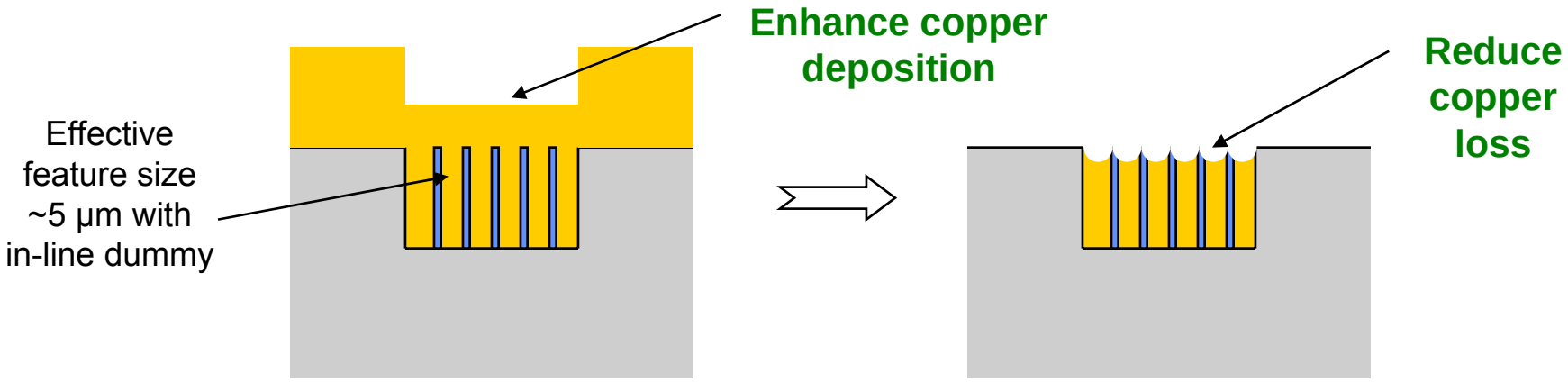
- Sacrifice the inserted copper to even the topography after polishing
- Increase dielectric loss
- Relatively ineffective for both small and large features

Topography Evolution without and with In-Pattern Dummy Fill

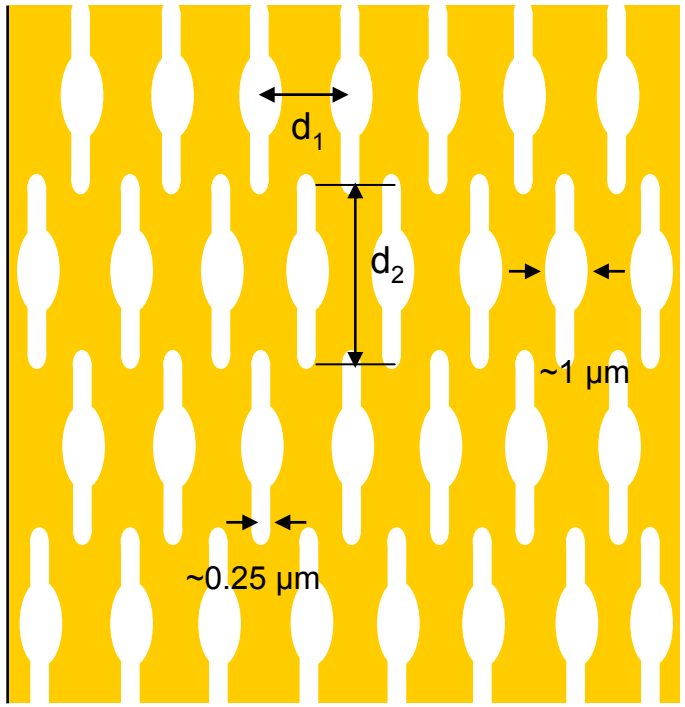
Wide Feature with Thin Deposited Copper Film

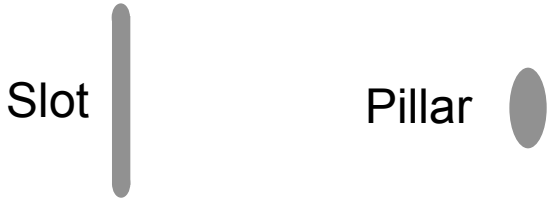


Wide Feature with Thin Deposited Copper Film and In-Pattern Fill



In-Pattern Dummy Design



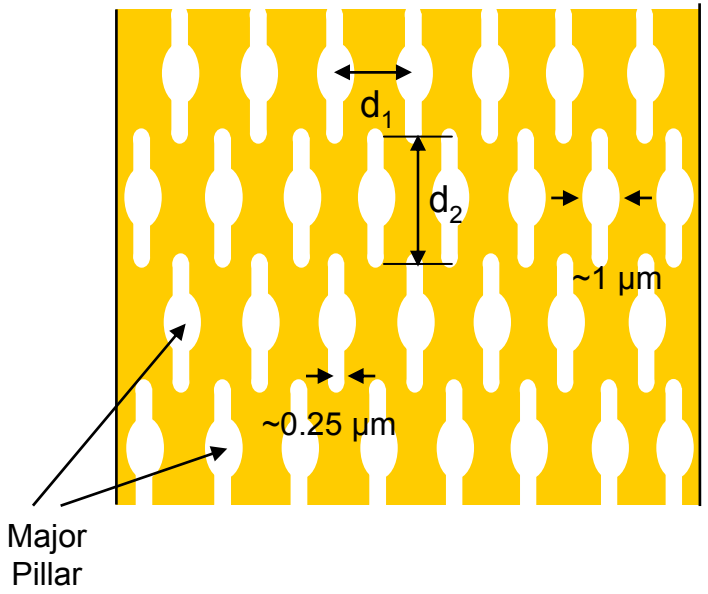


- Goals:
  - Optimize dummy design to improve *both* plating and post-CMP topography
- Approach:
  - Add "slot" to
    - increase trench wall surface areas
    - increase plated copper thicknesses
  - Add "pillar" oxide structures to
    - support the pressure of the pad
    - restrict ability of asperities to reach copper between fill structures

In-Pattern Dummy Fill in Co-Optimization

Impact of size specifications of in-pattern dummy fills

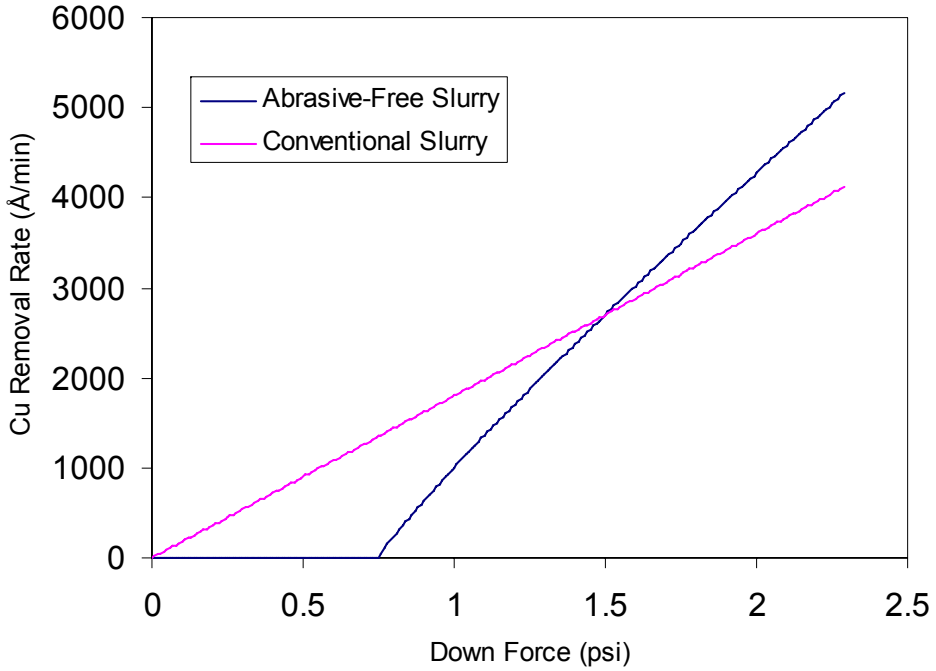
#	d_1 (μm)	d_2 (μm)	Dummy Fill Area Fraction (%)	Dummy Fill Perimeter in Cell (μm)
1	5	10	7.24	163
2	4	8	9.75	205
3	3	6	14.55	275



Hypothetic Abrasive Slurry in Co-Optimization

Removal rate vs. down force

for hypothetical abrasive-free and conventional slurry



$$R = R_{cu}\left(\frac{P - P_{th}}{P_0 - P_{th}}\right)^{\alpha} \qquad for \;\; P > P_{th}$$

$$P_{th} = 0.75\,\text{psi}$$

$$\alpha = 0.9$$

$$R_{Cu} = 2700\ \text{Å/min (at 1.5 psi)}$$

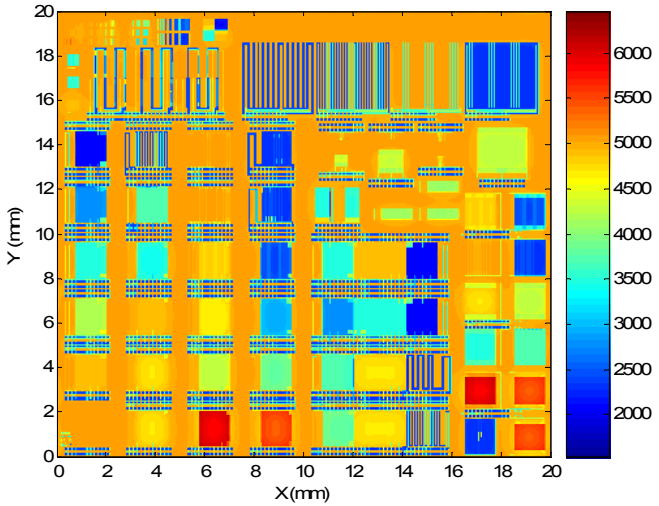
- The removal rates for TaN and Oxide are assumed to follow Preston's equation with a rate of 0.4 Å/sec at the nominal down force of 1.5 psi
- Non-selective barrier slurry is assumed in the following polishing step and only copper CMP is simulated for this case

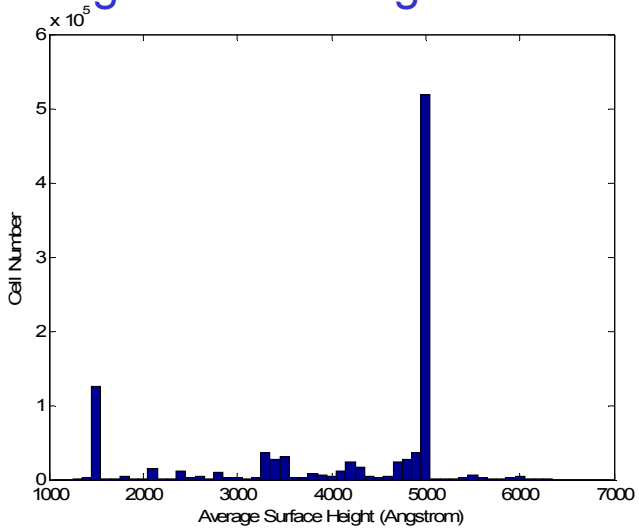
ECD Chip-Scale Simulation

Average Surface Height Map (Å)

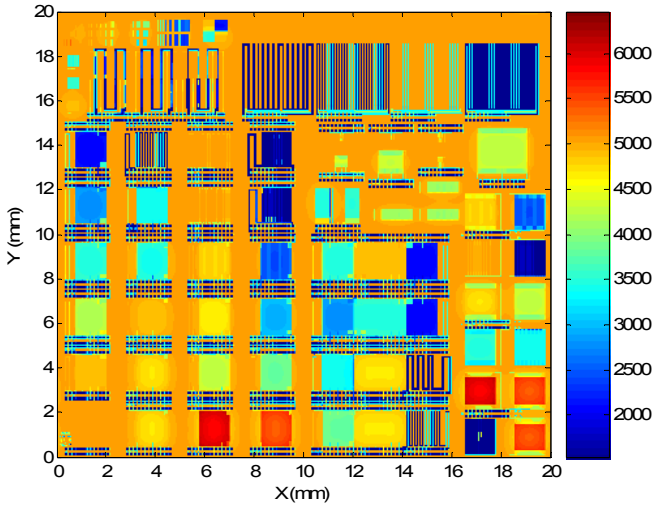
Histogram of Average Surface Height

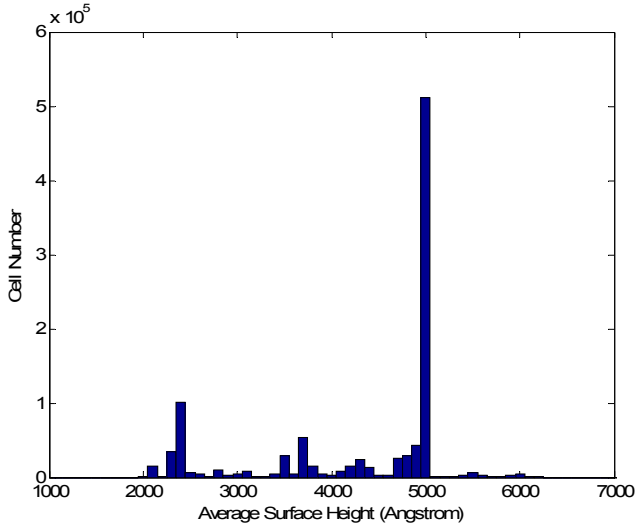
w/o dummy fills





w/ dummy fills



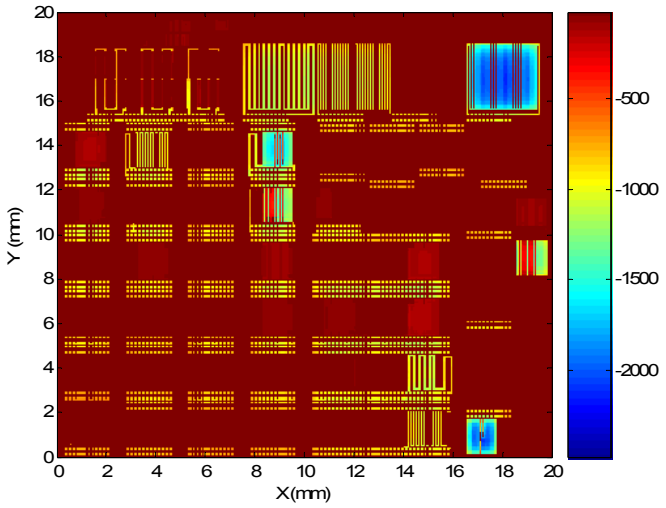


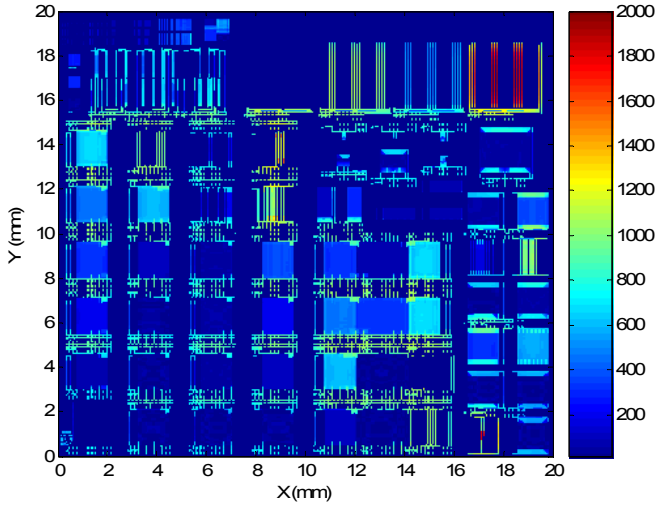
CMP Chip-Scale Simulation

Envelope Map (Å)

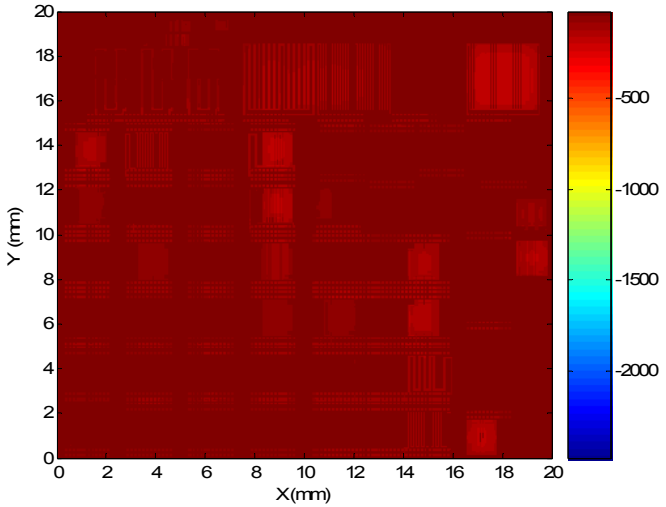
Step Height Map (Å)

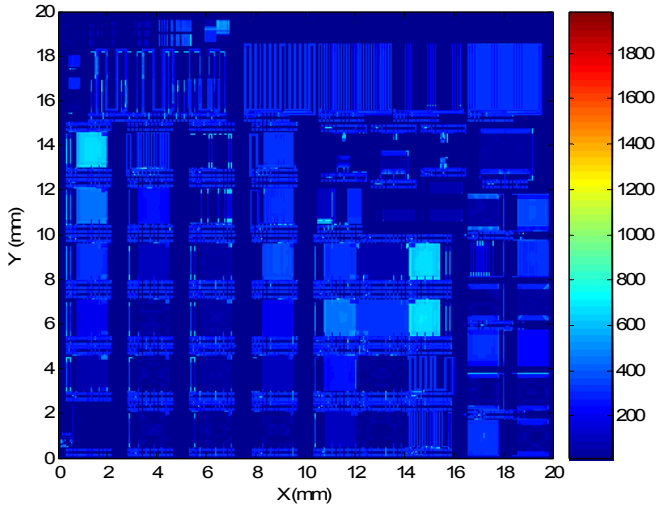
w/o dummy fills



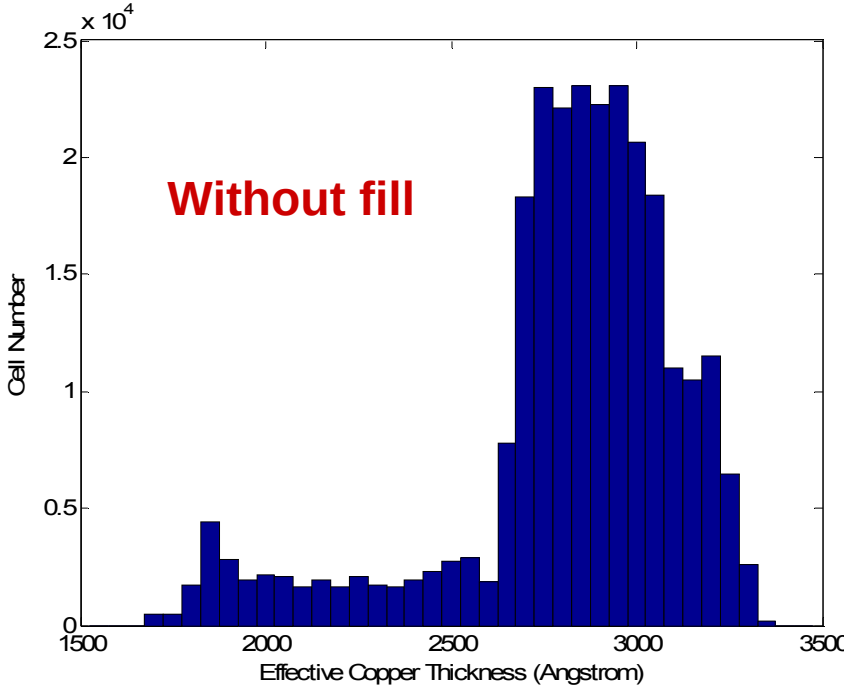


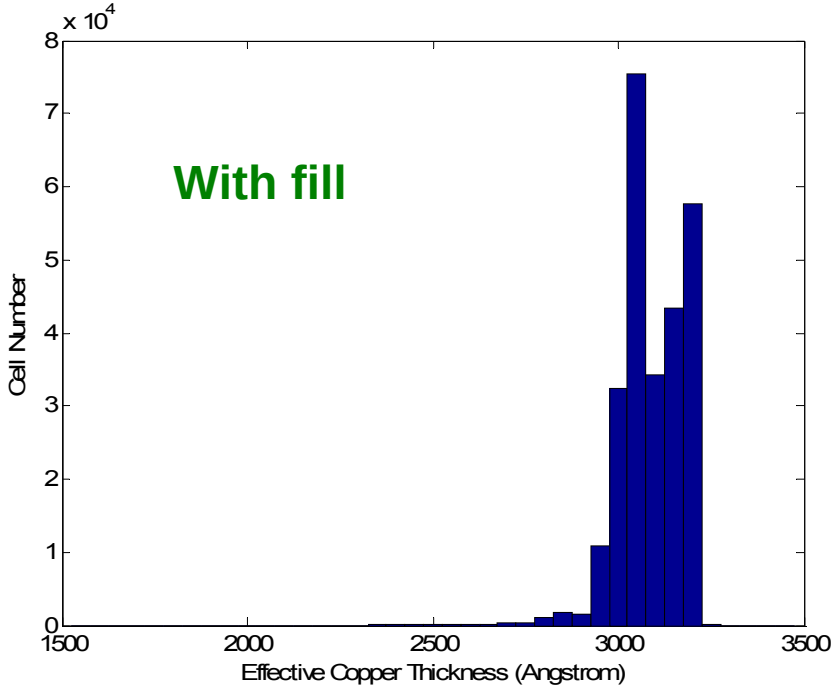
w/ dummy fills





Comparison: Effective Copper Thickness w/o and w/ In-Pattern Dummy Fills





- Key results
  - Dramatically improved topography variation based on fills designed with *both* ECD and CMP in mind
  - Reduction of copper thickness required, from 8500 Å to 5000 Å, results in >40% reduction in plating and polishing
  - The topography effects from the CMP process dominate those from the ECD process

Low-K Dielectric Impact on Dummy Fill

- Assumptions of in-pattern dummy design and optimization
  - Copper to dielectric selectivity is high
  - Barrier slurry has low-selectivity
  - Details of the barrier removal step are ignored
- However, in some emerging low-K and copper damascene approaches, reverse selectivity is used
  - Higher removal rate of low-K materials could introduce significant dielectric loss in the wide non-patterned areas
  - *Between-pattern* dummy fills can help limit low-K dielectric loss
- The general rule of dummy fill design
  - Insert dummy fills in the wide areas, whether patterned or non-patterned, where the removal rate is higher
  - Simulation using chip-level ECD and CMP models can be used to optimize the dummy fill design

Summary

- New physics-based integrated ECD/CMP model used to
  - simulate the topography evolution
  - study various in-pattern dummy fill designs
- Simulation results: optimized dummy fill design can
  - significantly improve the post-CMP topography
  - enhance the electrical performance (net cross-sectional area) of interconnects in some cases
  - reduce electroplated copper thickness, and consequently reduce the polishing time in CMP
  - save costs on the consumables, energy
  - reduce environmental impact
- Results suggest that next generation planarization needs can be met with joint use of (a) conventional CMP technology, (b) abrasive free slurries, and (c) dummy fill

Contributions

- Developed a chip-scale copper electroplating model that incorporates the effects of additives, feature-scale dependencies, and copper depletion, and can be applied to random layouts.
- Developed an improved copper CMP model integrating contact wear, pattern density, and step height dependence in order to improve the prediction of dishing and erosion for random layouts.
- Improved layout parameter extraction procedures and terminology for topographical features, enabling the seamless integration between electroplating and CMP models.
- Characterized and validated both metal 1 and metal 2 electroplating and CMP pattern dependent effects, and extended the integrated model into the multilevel cases.
- Identified the impacts of temperature variation and pattern dependency of other processes on the CMP modeling.
- Illustrated the co-optimization of electroplating and CMP and demonstrated the significant improvement in the topography and effective copper thickness from the use of in-pattern dummy fills.

Future Work

- Improvement and refinement of the current ECD/CMP integrated models.
  - Include leveler into ECD model
  - Details of slurry in CMP model
  - Temperature effect in CMP model
  - Further dummy fill optimization, experiments
  - Impact of the electroplated copper thickness and dummy fills on the copper resistivity
- Seamless model integration with other pattern dependent processes in the back-end-of-line.
  - Etching pattern dependency
  - Film deposition pattern dependency (CVD, PVD, Spin-on …)

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