Environmentally Benign Manufacturing of Three Dimensional Integrated Circuits (3D ICs)

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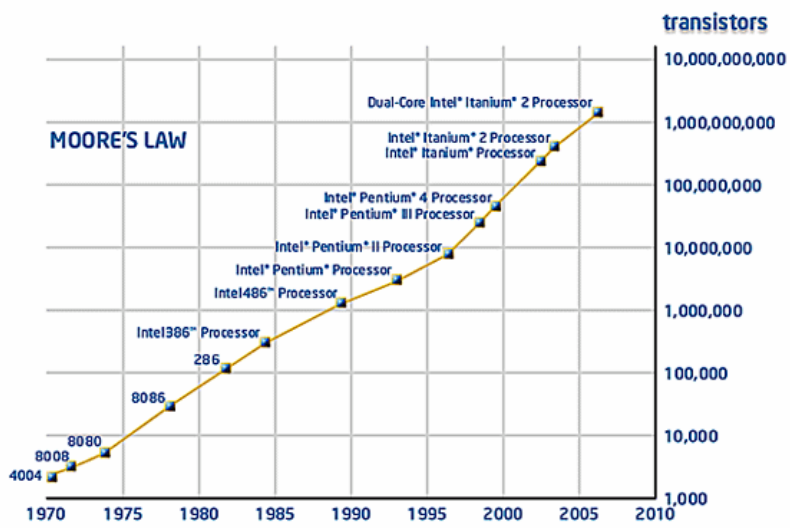
Outline

- Motivation and Background
- Environmental Impact Assessment Methodology
- Case Study: MIT 3D IC vs. 2D IC
- Assessment of Alternative Handle Wafer Options
- Summary

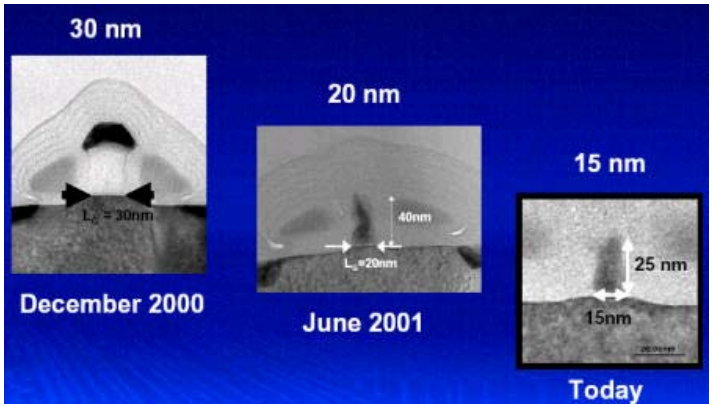
Motivation – Environmental Impact Assessment



Moore's law

(Source Intel's website)

Scaling

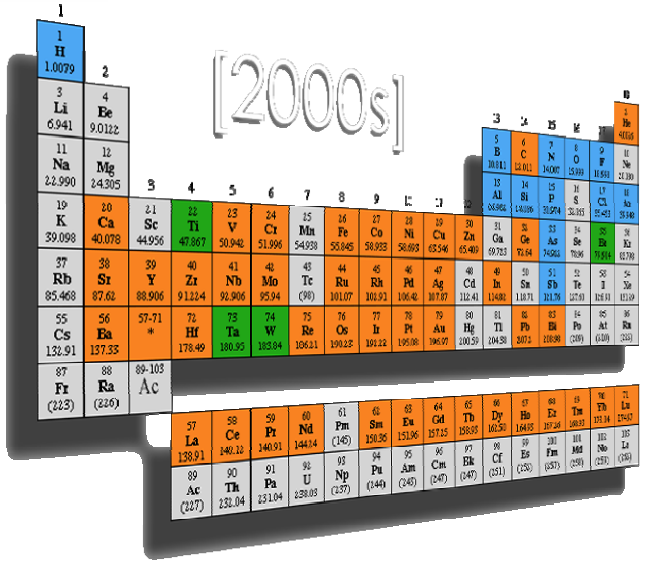


(Source – Intel's website)

- Increasing process complexity
- More energy consumption - fabrication

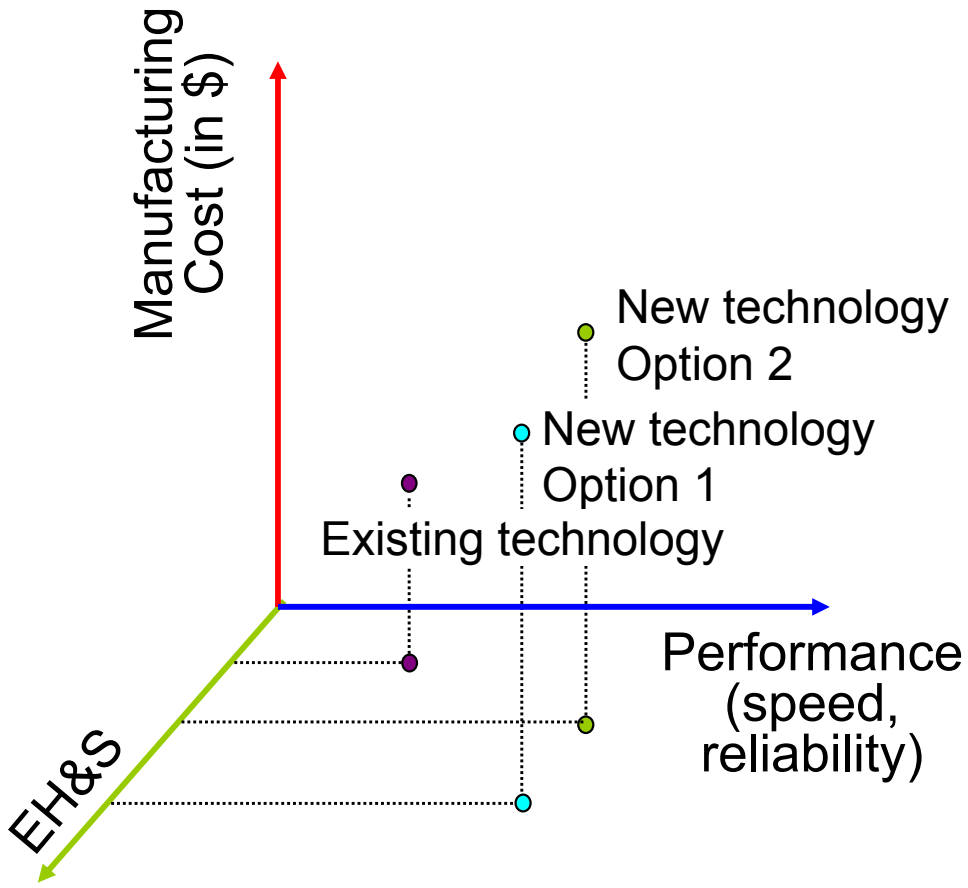
Introduction of New Elements

(Source – Intel)



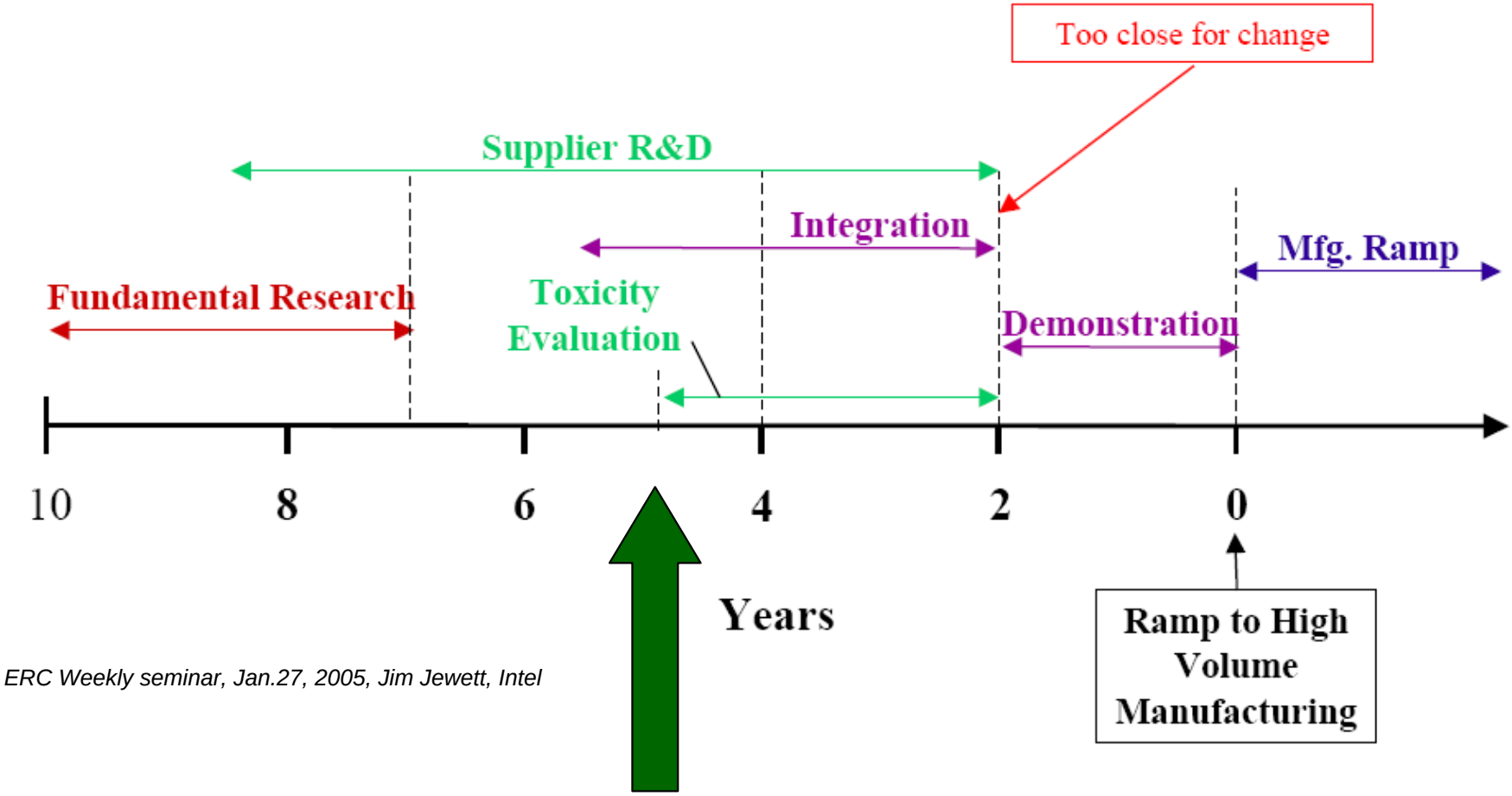
- More rare elements are used
- Limited information about environmental and health impacts

Motivation – Environmental Impact Assessment



- Each semiconductor technology can be mapped on manufacturing cost and performance axis
- Interplay decides future technology
- Need to integrate EH&S as 3rd axis
  - help in decision making
  - avoid surprises, such as lead ban
- As a first step, we focus on evaluating environmental impact
  - health and safety assessment needed in future work
- Goal: environment assessment methodology

Technology Development Cycle



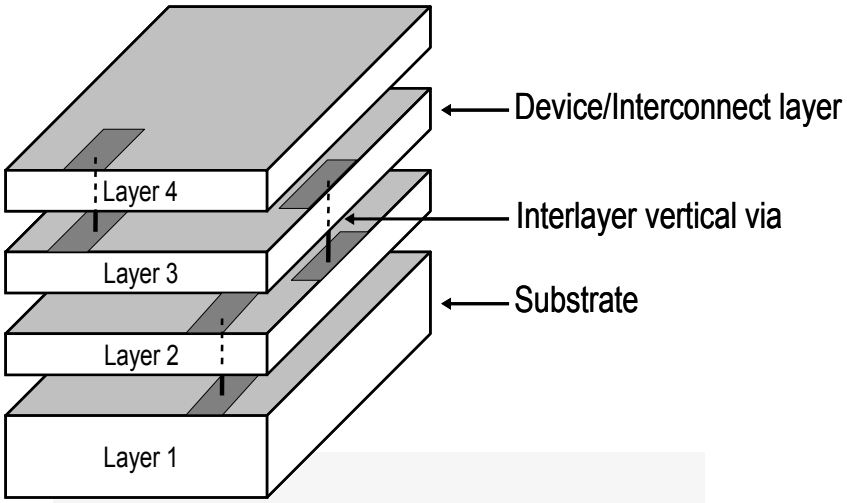
ERC Weekly seminar, Jan.27, 2005, Jim Jewett, Intel

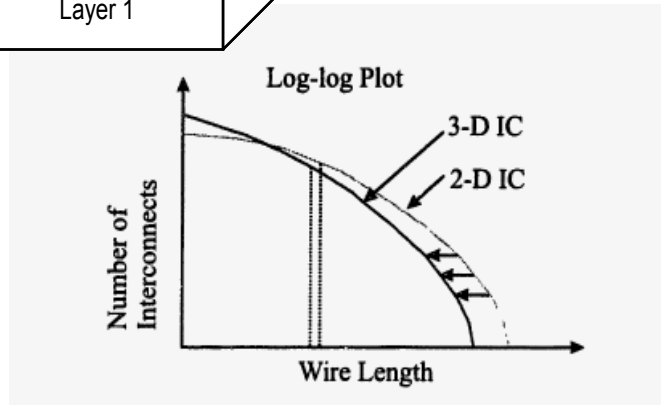
OPPORTUNITY for Environmental Evaluation

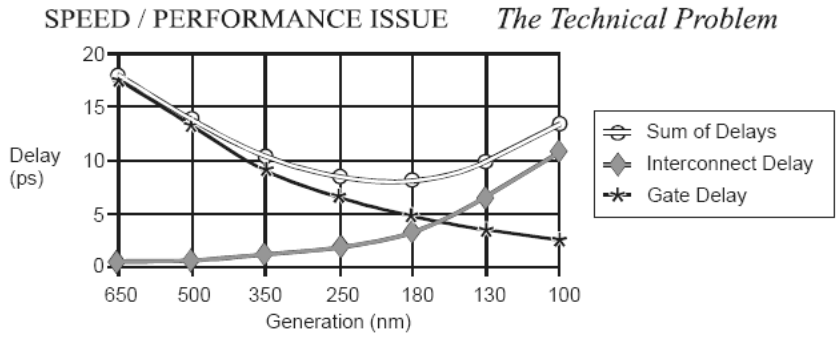
3D ICs at this stage of development

Three Dimensional Integrated Circuits (3D ICs) Motivations and Benefits

A vertical stack consists of multiple device and interconnect layers that are connected together by interlayer vertical vias







RC Delay vs. Generation

Performance Benefits:

- Narrower interconnect length distribution
- Improved chip form factor
- Enables hybrid CMOS
- Enables heterogeneous integration

A. Rahman, Ph.D. Thesis, MIT, 2001

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- Motivation and Background
- Environmental Impact Assessment Methodology
  - LCI for Wafer Fab
  - Assessment Methodology: Six Steps
- Case Study: MIT 3D IC vs. 2D IC
- Assessment of Alternative Handle Wafer Options
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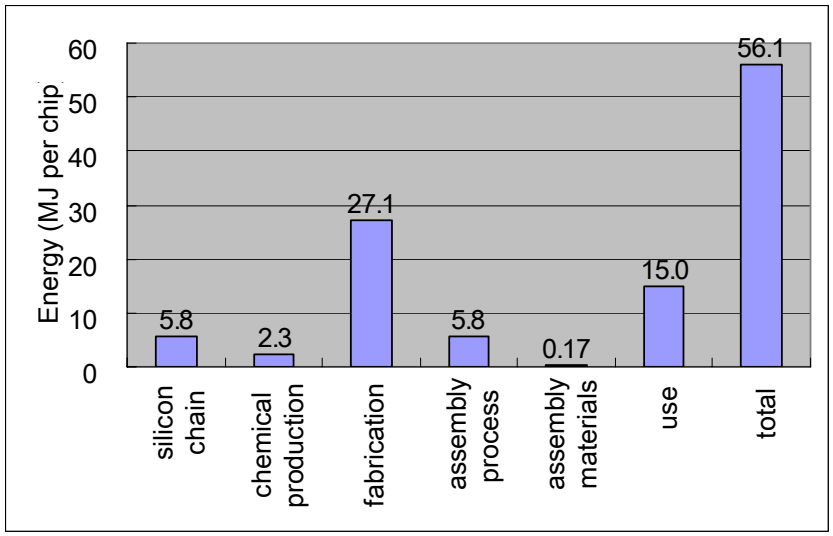
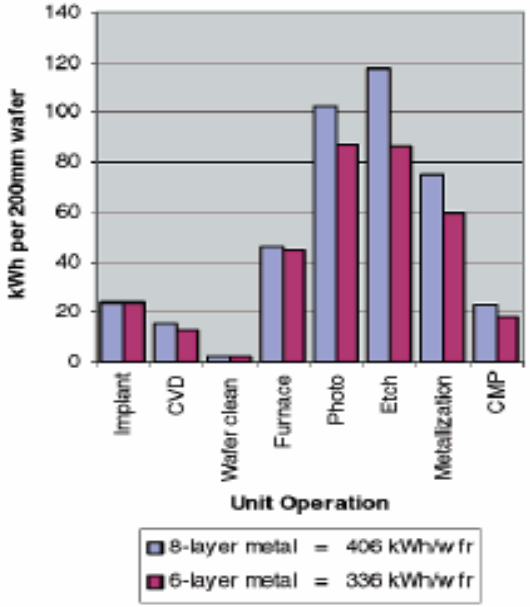
Life Cycle Inventory (LCI)

- Data based approach for quantifying inputs (energy, materials) and outputs (emissions and wastes)
  - More objective, can be applied to other process flows
- Williams et al. showed that fabrication is the most energy and materials intensive part
- Murphy et al. – LCI for wafer fab for 130 nm node and 200 mm wafers
  - Compared 6 and 8 metal layer circuits
  - Energy consumption for 8 metal layers is 406 KWhr/8 in. wafer
- Limitations
  - Studies focused on energy
  - Not transparent, data was confidential
  - Lack assessment component and did not provide guidelines for improving environmental footprint

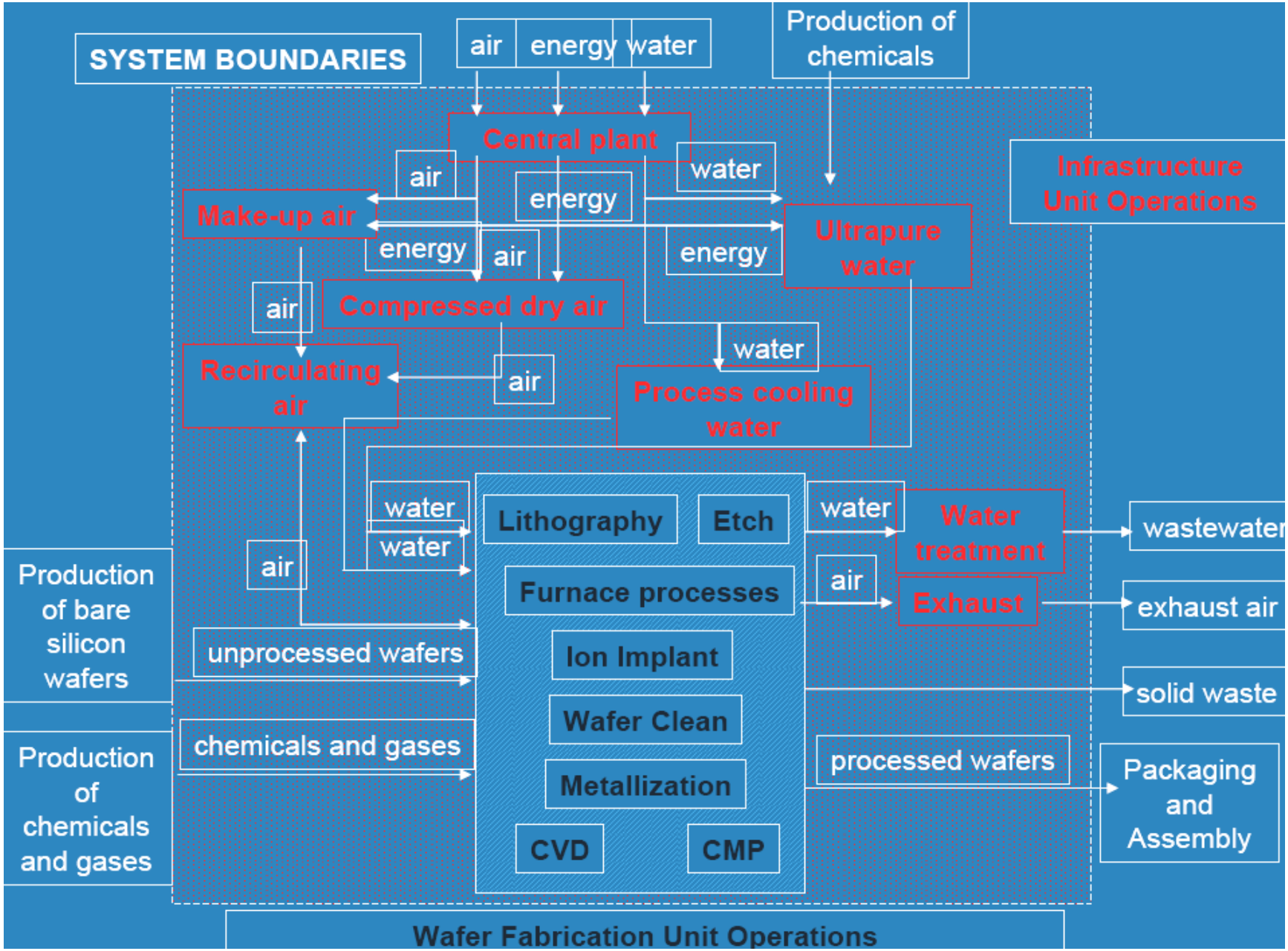


Eric Williams et al., 1.7 Kilogram microchip: Energy and materials use in production of semiconductor devices, Env. Sci. & Tech.'02



Cynthia Murphy et al., Parametric Inventories for material, energy and emission, Env. Sci. & Tech.'03

LCI for Wafer Fab: System Boundaries

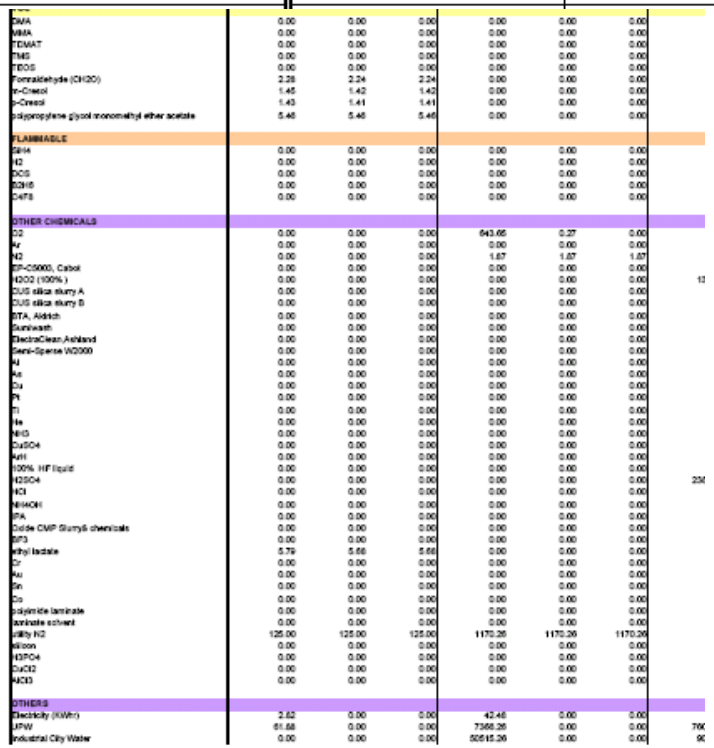


C.F. Murphy, J.P. Laurent, D.T. Allen, "Life Cycle Inventory Development for Wafer Fabrication in Semiconductor Manufacturing", IEEE International Symposium on Electronics and Environment pp.276-281, 2003

New Process Based Inventory

- Created in collaboration with N. Krishnan and S. Boyd at Applied Materials
- Collected inventory for all CMOS process
  - Process energy, facilities energy
  - Water (ultra pure for process and process cooling water)
  - Listing 80 chemicals which are not confidential, divided into sub-groups of GWGs, VOCs
- Submitted to Journal of Environment Science and Technology
  - Will publish the inventory as supporting information

UNITS in g/wafer wherever possible		
	130 nm node 300 mm wafer 6 layer wafer	
Film Thickness (A)		Total Time
Time (s)	22508.70787	45936.13851
	IN	OUT
GWG		
CF4	15.98128683	17.38392932
CHF3	1.041828794	0.607741395
C2F6	0	0.863
CH4	1643.479613	0.338
CO2	0	763.7275313
NF3	353.2381958	8.254029167
C4F6	0.650892857	0.05



Environmental Assessment Methodology

1. Identify particular novel silicon process technology to be evaluated
2. Identify state of art technology, that is going to be replaced / augmented by novel technology under investigation and generate its environmental footprint
3. Define functional unit for comparison (e.g., # of transistors, area)
4. Design prototype process flow for novel technology
5. Compare environmental impact of alternative process technology to the standard technology, taking into account the functional unit
6. Identify and develop critical unit processes which have performance, cost, or environmental issues

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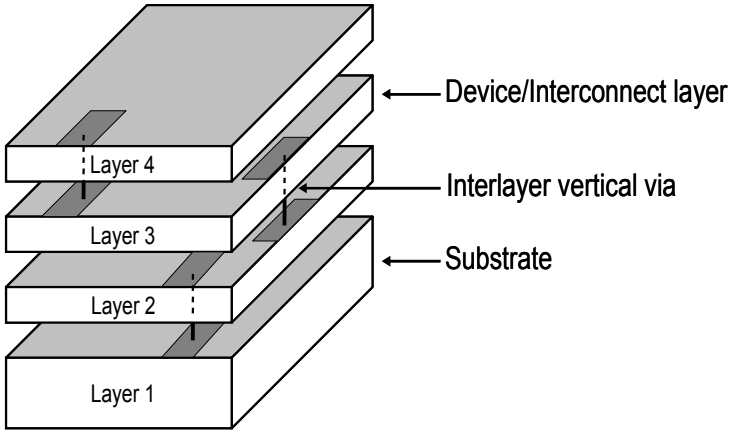
- Motivation and Background
- Environmental Impact Assessment Methodology
- Case Study: MIT 3D IC vs. 2D IC
  - Methodology Application: Six Steps
  - First-order Energy, Water and Chemical Consumption
- Assessment of Alternative Handle Wafer Options
- Summary

1. Why Do We Choose 3D IC?

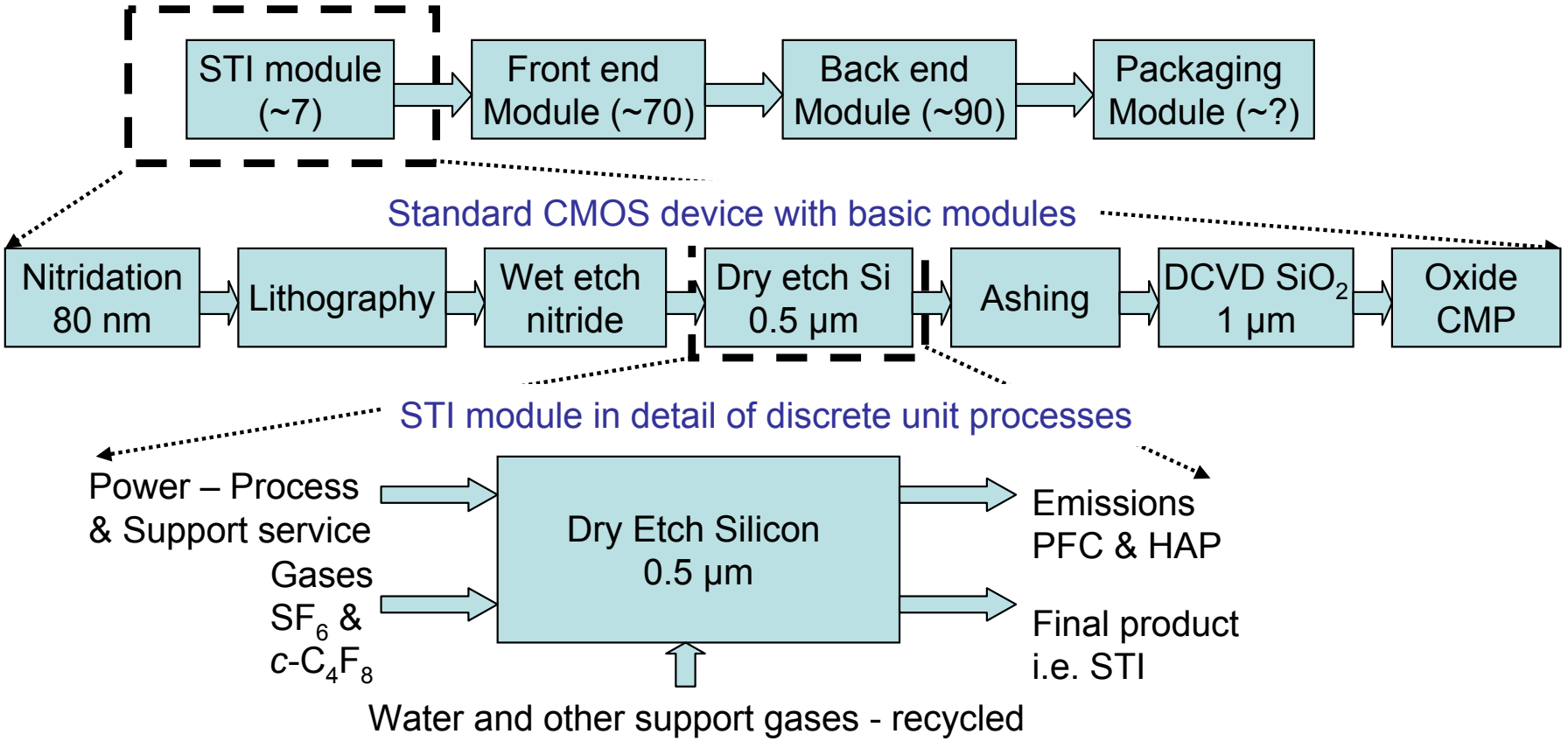
- Technology 4-5 years down the line
- Has various options available
  - Bonding, Recrystallization….
  - Wafer to Wafer, Die to Wafer



- Advantages along performance axis
  - Substantial existing performance research
- Need to assess environmental impact (and cost) as well

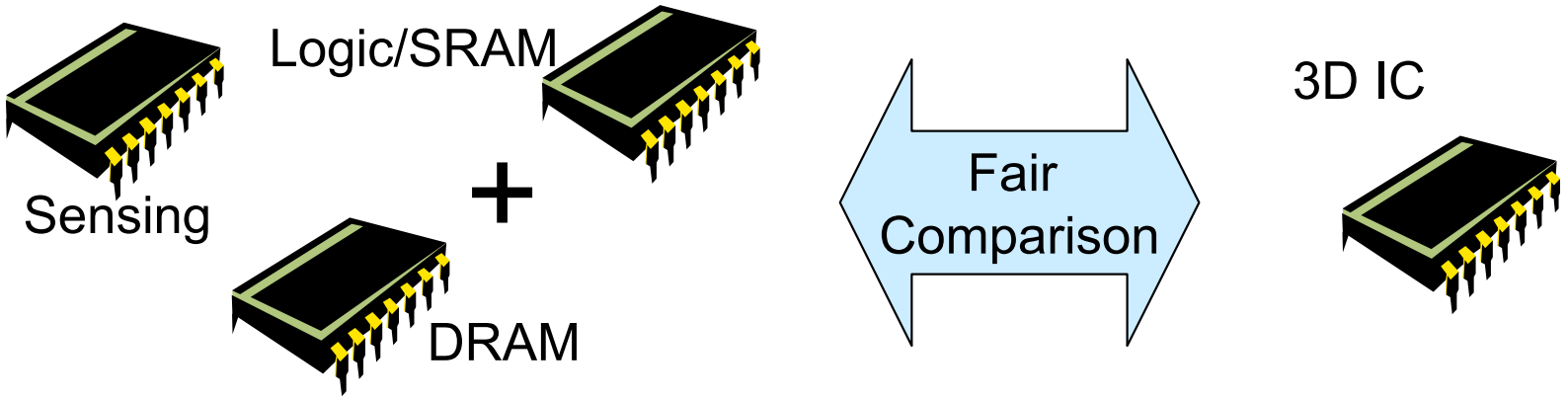
2. Environmental Footprint Standard 2D IC

- Issues: dynamic, extensive materials, various technologies, confidential
- Modular and hierarchical process flow
- Utilize our process inventory



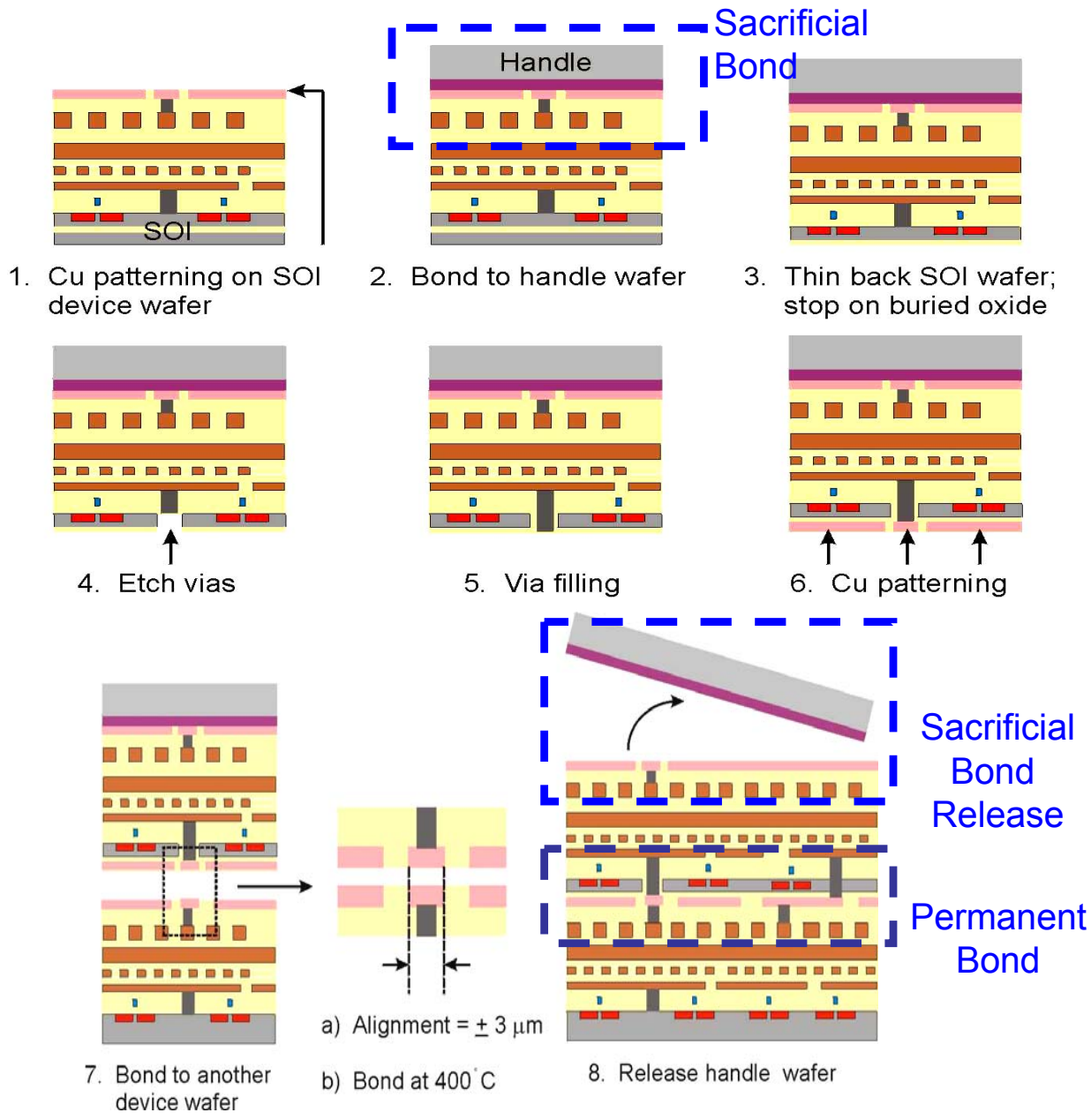
3. Functional Unit : 2D vs. 3D

- Identification of appropriate functional unit is a challenge in comparing 2D vs. 3D technologies
- If packaging changes, comparisons of environment, cost, and performance of packaging are also needed



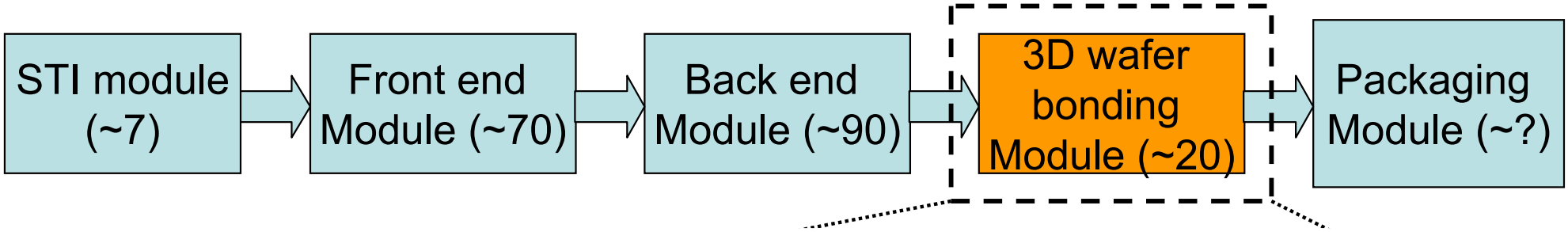
- Our focus: single chip 2D vs. single 3D chip
  - E.g., system on chip (SoC) that integrates logic and SRAM
    - Perhaps on separate layers in the 3D chip
  - Scope restricted to wafer fab issues; do not address packaging

4. Prototype Considered: MIT's 3D Process Flow

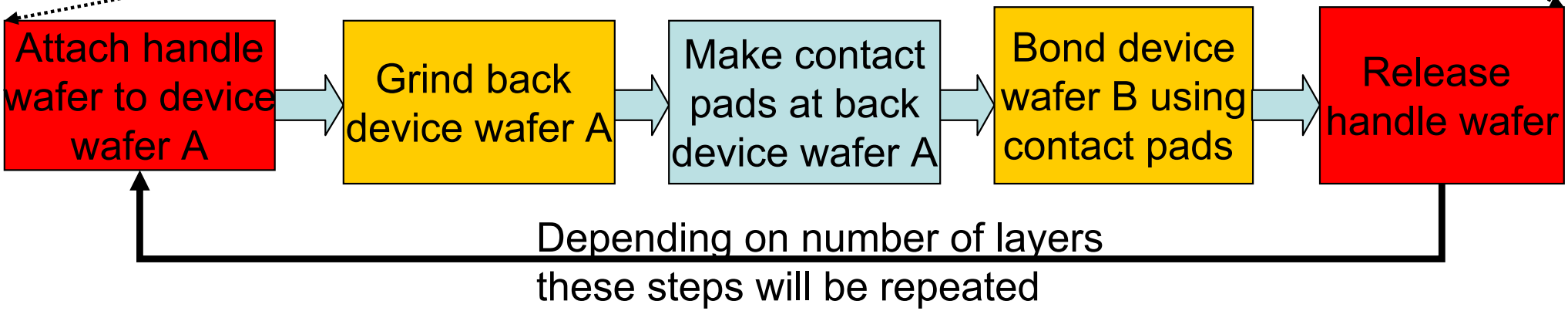


Fan, PhD Thesis, MIT 2006

5. Environmental Footprint 3D IC



Standard 3D IC using wafer bonding approach – MIT Approach



Describing 3D wafer bonding module in terms of process flow

New but not major concern

New step of potential concern

6. 2D vs. MIT 3D Process Step Summary

Unit operation	Unit steps in 2D process flow (for one wafer)	Additional unit process steps in 3D process flow
Photo/stepper/ashing	25	1
Dry Etch	13	2
Wet etch + Clean	31 + 14	3 + 4
CVD	11	1
CMP	14	2
Sputtering Al	1 (0.5 μm for metal 1)	2 (20 μm)
Sputtering Ta/Cu	6	1
Electrodeposition Cu	6	1
Annealing	15	2
Bonding	0	2
Grinding	0	1

Results – First-order Comparison

	Energy Consumption (KWh)	Water Consumption (m^3)			Chemical Consumption
		PCW	UPW	ICW	
Adding 1 layer to 3D Stack	**340 +**	**14.7 +**	**0.6 +**	**0.1 +**	**Equivalent to adding 1 more interconnect layer**
2D CMOS, 300 mm wafer, 130 nm technology, 6 metal layers	**540**	**26.6**	**0.96**	**0.65**	**Summarized in thesis Appendix A**

- Novel processes such as bonding and grinding are estimated using process knowledge and literature
- 17 additional standard unit processes consume 40 KWh of energy
- 270 KWh energy and 13 m^3 PCW is attributed to the two thick metal sacrificial deposition steps
- Handle Wafer has large environmental footprint

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- Motivation and Background
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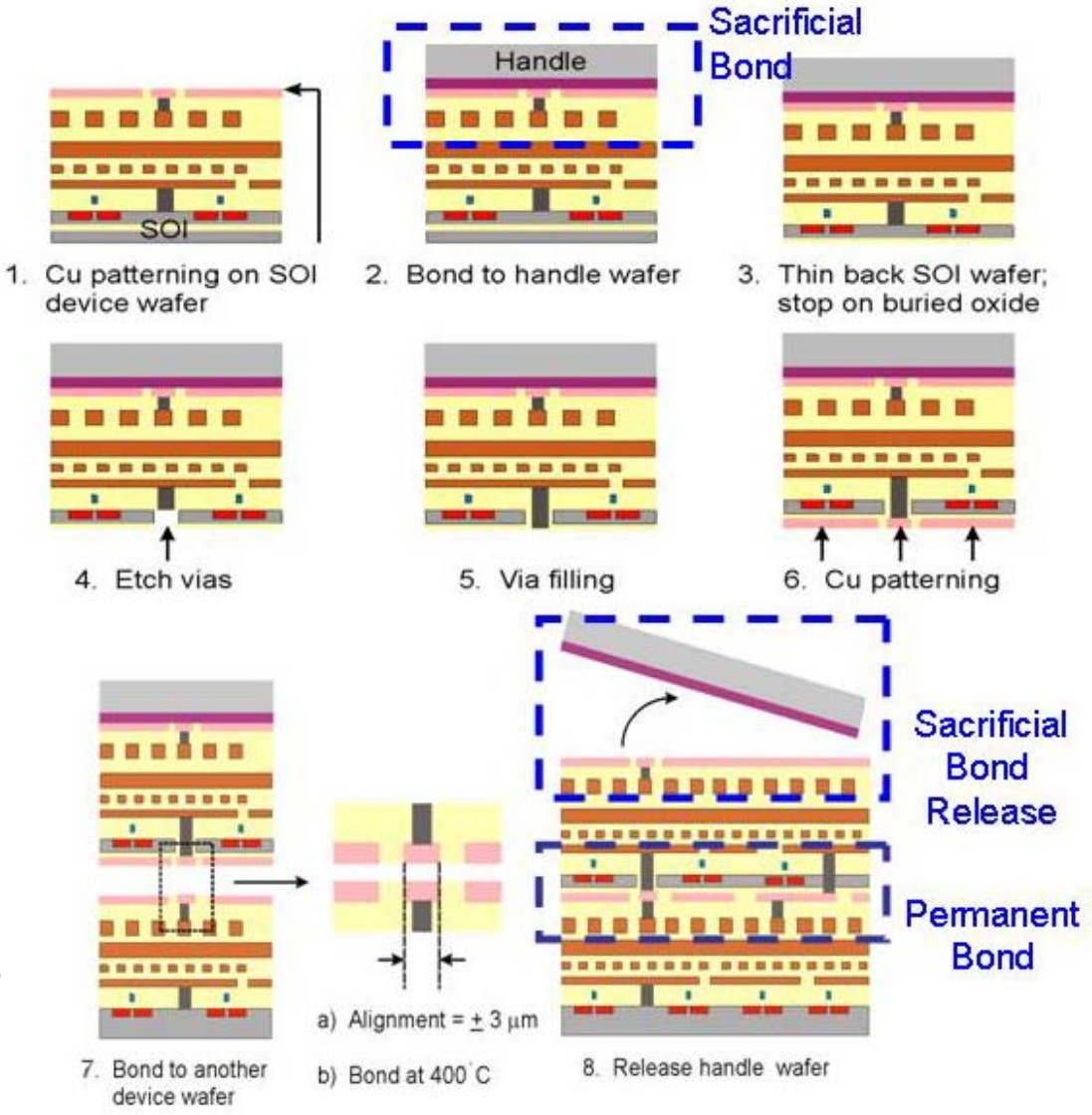
- Case Study: MIT 3D IC vs. 2D IC
- Assessment of Alternative Handle Wafer Options
  - Requirements
  - New Approaches
  - Assessment of Handle Wafer Options
- Summary

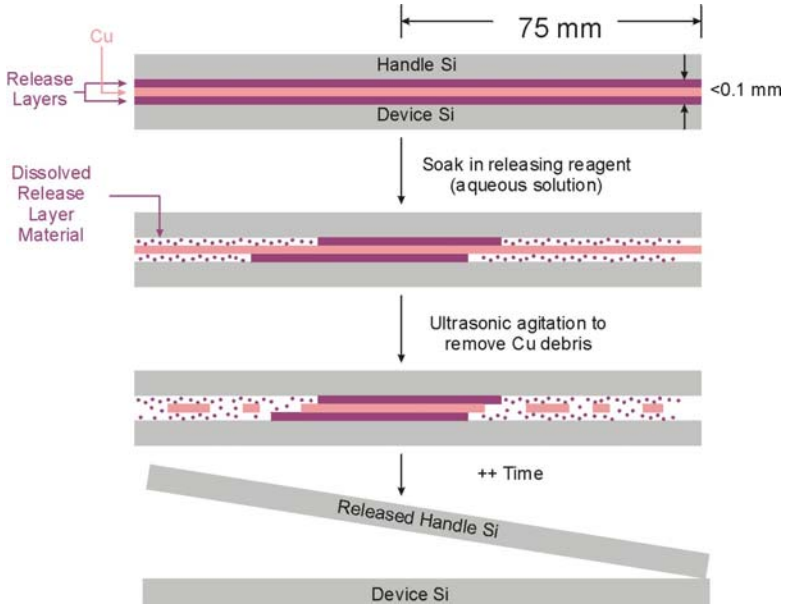
Handle Wafer Process: Functions and Requirements

- Functions
  - Support wafer during thinning and subsequent processing
  - Provides stackability
- Requirements
  - Bond Strength of Temporary-bond
  - Void Free Bonding
  - Thinning Back Capability
  - Chemical Resistance
  - Thermal Processing Range
  - Ease of Debonding



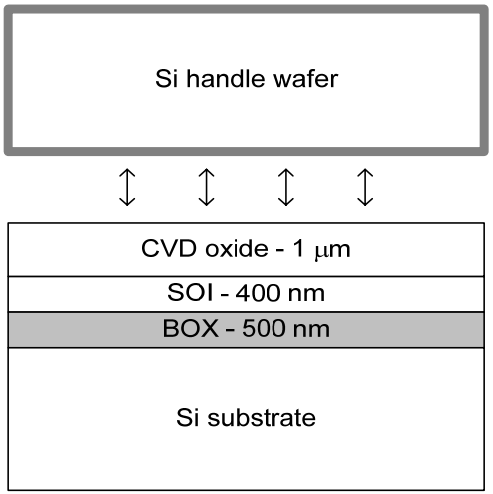
Previous MIT Approaches

- Al release layer
  - 20 μm Al is deposited on both wafers and etched with HCl
  - Mass diffusion limited



Andy Fan, EECS MIT PhD Thesis 2006

- Smart Cut
  - H_2 implantation on handle wafer
  - Thermal activation to release
  - Thermally unstable and expensive



Top wafer is bonded to handle wafer (CVD-to-thermal oxides bonding).

Chuan-Seng Tan, EECS MIT PhD Thesis 2006

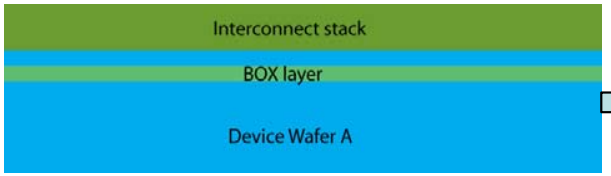
Performance Comparison – Previous Handle Wafer Options

Handle Wafer Approaches	Bond strength	Void Formation	Chemical Selectivity	Thinning-back Capability	Temperature range	Time to debond
Al Release Layer	3 J/m^2 ✓	No ✓	Probably with TMAH ↔	Good ✓ < 1 μm	Good ✓	Does not release in finite time ✗
Smart Cut	2 J/m^2 ✓	Few ↔	Good ✓	Good ✓ < 1 μm	Requires processing temp. less than 250^{o}C ✗	Good, released in 60 min ✓

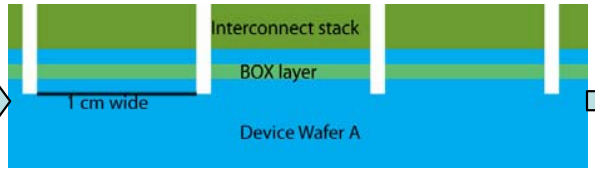
New Approaches for Handle Wafer Processes

1. Between-Die Channels
   - Overcome diffusion problem – introduce channels in the *device* wafer
   - Laminate structure: Al release layer with copper bonding stack
2. Oxide Release Layer
   - Overcome diffusion problem – introduce channels in the *handle* wafer
   - Oxide bonding and release layer
3. Alternative Low-Temperature Permanent Bonding
   - Enable permanent bonding at temperature such as 200^{o}C
   - Using copper-indium SLID bonding

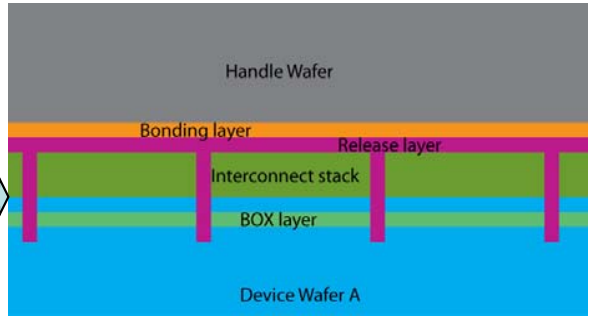
1. Between-Die Channel Approach



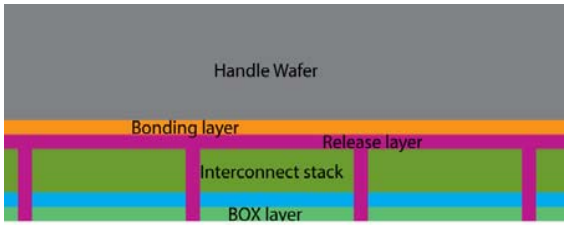
Device Wafer Ready for Packaging



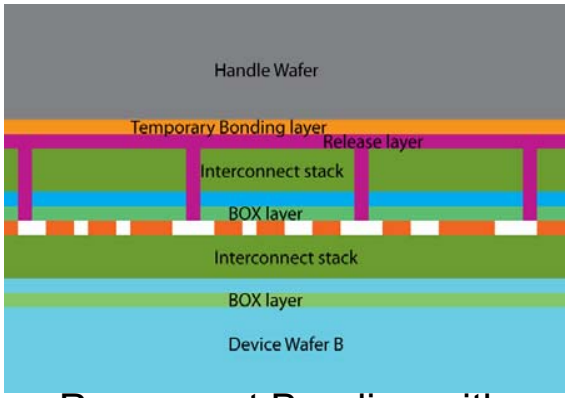
Patterning Die-Saw Mask and Etching



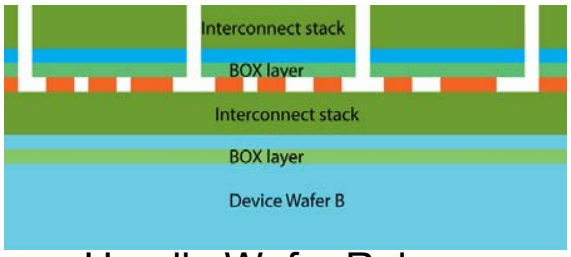
Temporary Bonding with Release Layer



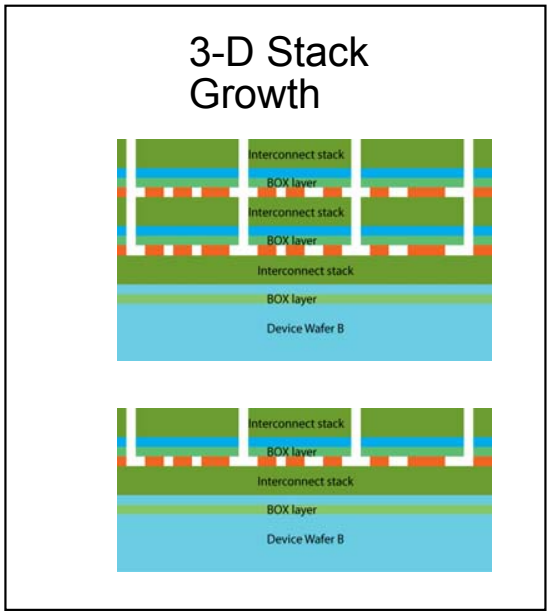
Thinning Back Wafer



Permanent Bonding with Active Electrical Contacts and Dummy Mechanical Pads



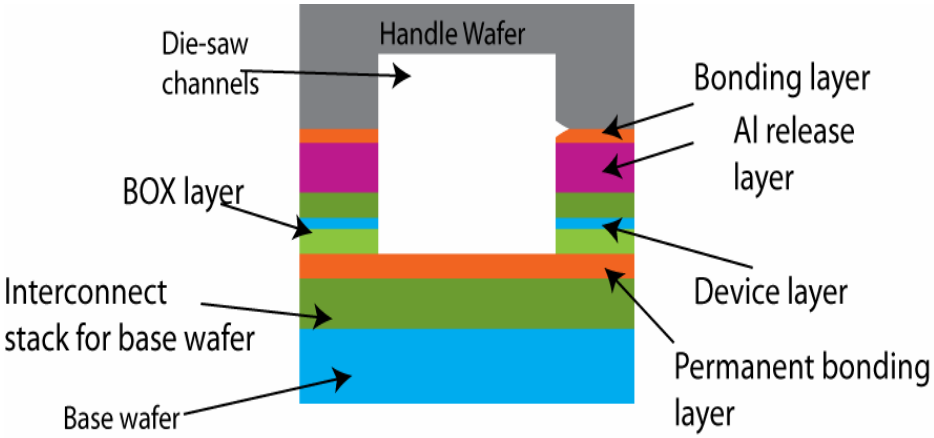
Handle Wafer Release

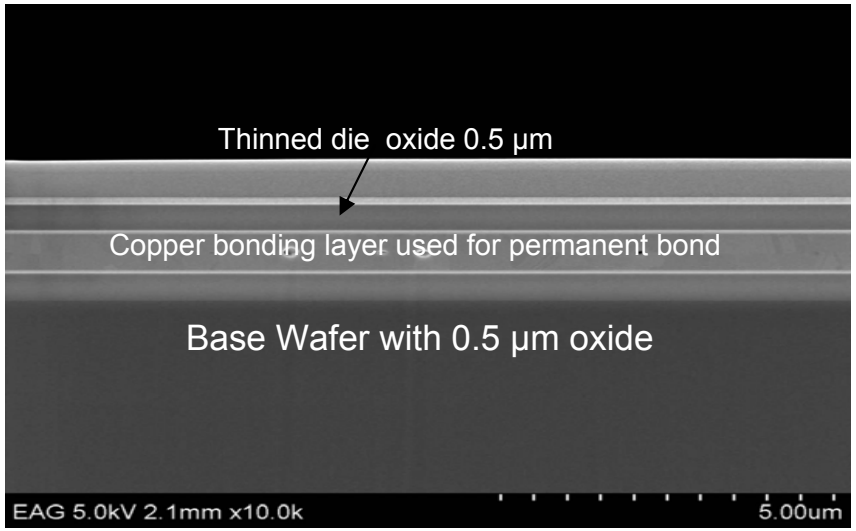


Repeated several times for 3D Stack

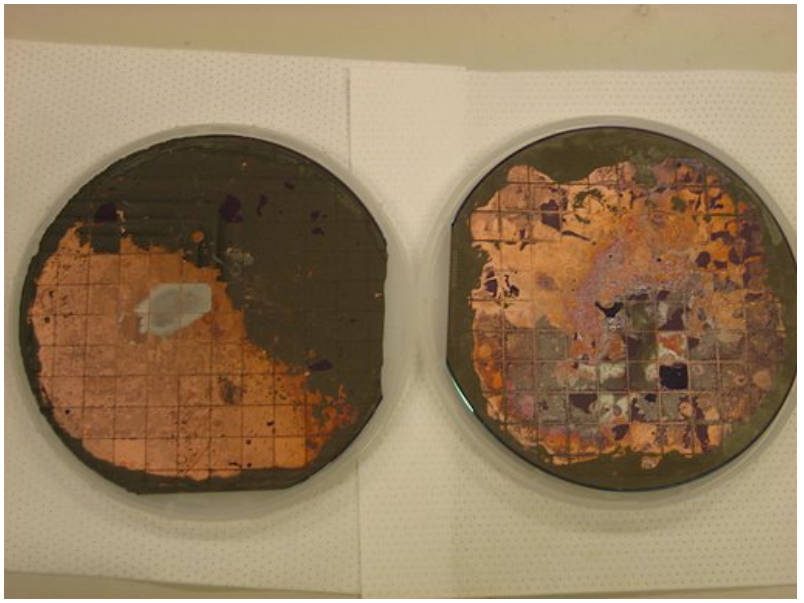
Results for Between-Die Channel on Both Handle and Device Wafer

- Channels etched in handle wafer to also act as diffusion channels
- Channels on handle wafer are 20 μm deep – takes 8 hours to release at bath temperature 60°C in HCl:H_2O ratio 1:1 with intermittent ultra-sound
- FIB-SEM shows that die was transferred successfully





FIB-SEM of die on base wafer bonded with copper

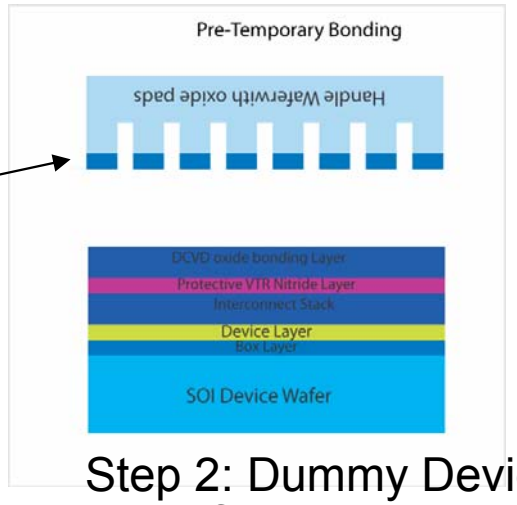


Released Handle wafer and transferred dies on base wafer in left and right respectively

2. Oxide Release Layer

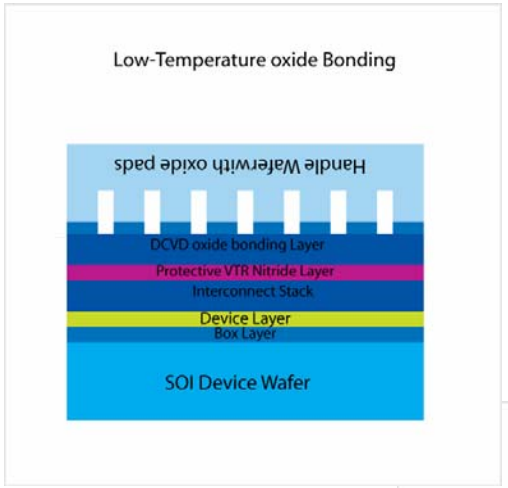
Idea: put channels above whole body of die, not just between die

Step 1: Handle Wafer Fabrication

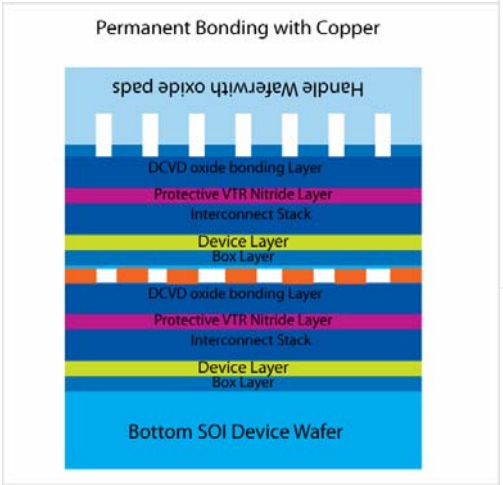


Step 2: Dummy Device Wafer Fabrication

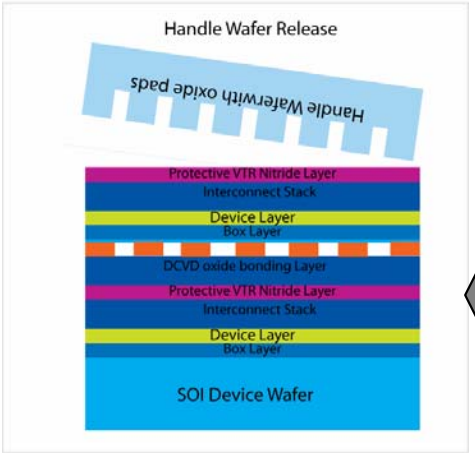
Step 3: Low-Temperature Plasma Assisted Oxide Bonding



Step 4: Wafer Thinning



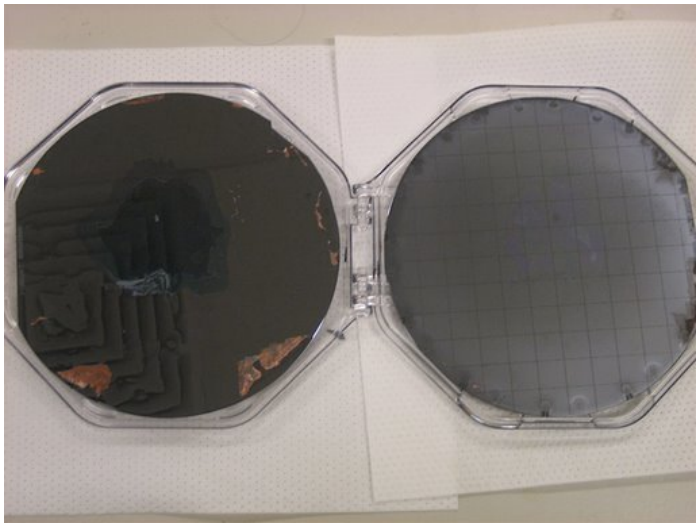
Step 5: Permanent Copper Bonding



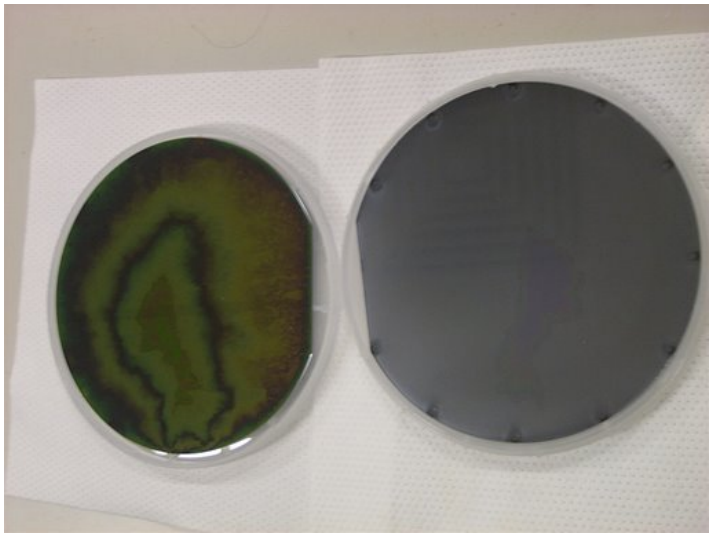
Step 6: Handle Wafer Release

Oxide Release Layer Results

- Wafers on the left show two examples of successful release
- Release was conducted and thin layer was transferred to another substrate in 45 min (best time) and 80 min (worst time)
- Final Release time depends on
  - Pattern (pad size and channel), pad size ↑ causes time ↑
  - Channel depth ↑ causes time ↓
  - Processing temperature ↑ causes time ↑
- Concern
  - HF acid highly corrosive



Wafer scale release but nitride was etched away. Handle wafer was 40 μm deep with 80 μm pads and die-saw lines etched. It took 80 min



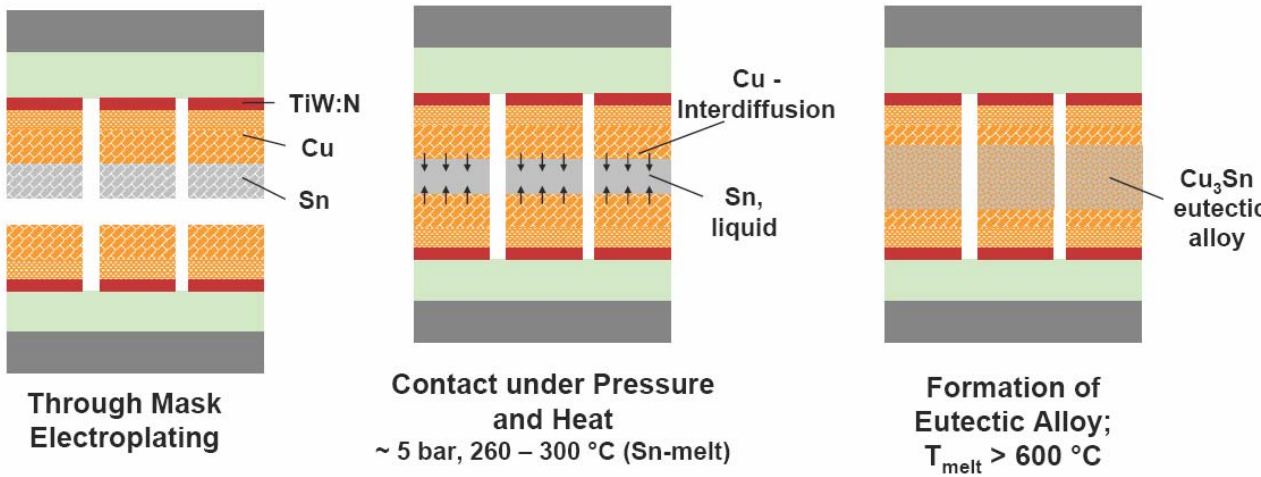
Successful release with nitride and oxide stack beneath is intact. Handle wafer was 60 μm deep with 80 μm pads. It took 45 min

3. Alternative Permanent Cu-In Bonding

- Motivation: enable low-temperature bonding
  - Provide flexibility or ease in designing handle wafer options
- Solid Liquid Interdiffusion Bonding (SLID)
  - Deposit *elemental stack* for low and high melting point metals on different wafers
  - Bond (at 200^{o}C) under pressure using thermo-compression bonding
  - Liquid diffusion creates *intermetallic compound* that is stable at higher temperature

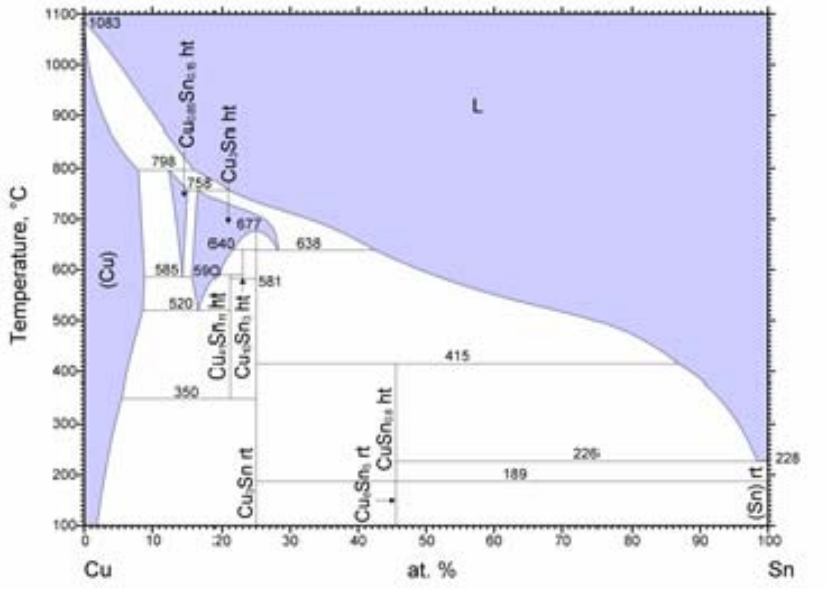
Solid Liquid Inter-Diffusion (SLID)

- Basic sequence of events
  - Wetting
  - Alloying
  - Liquid Diffusion
  - Gradual solidification
  - Solid-diffusion



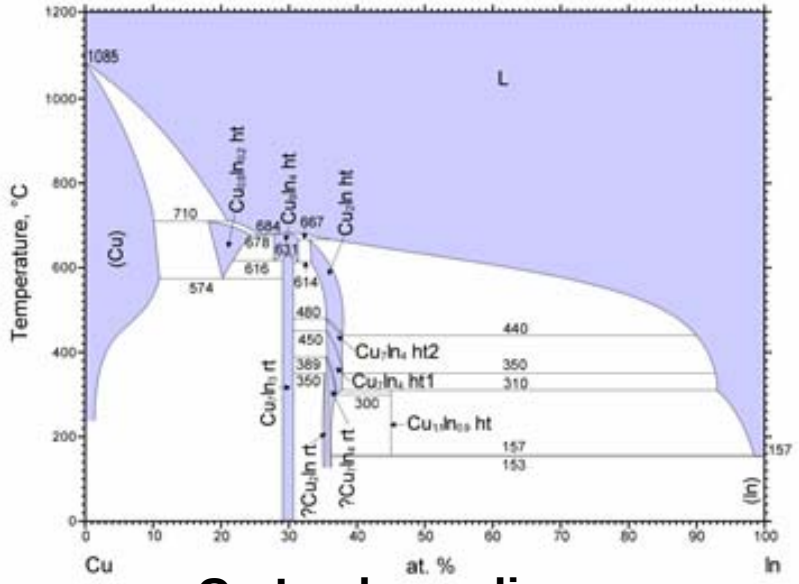
IZM, MRS, 2003

- Cu-Sn under investigation by IZM



Cu-Sn phase diagram

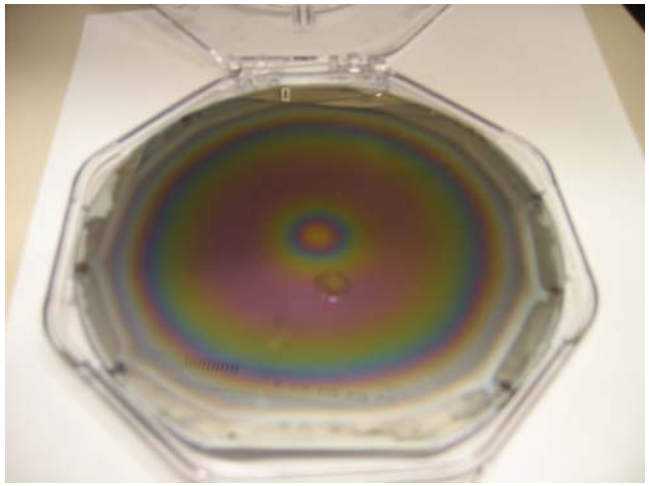
- Our focus : Cu-In



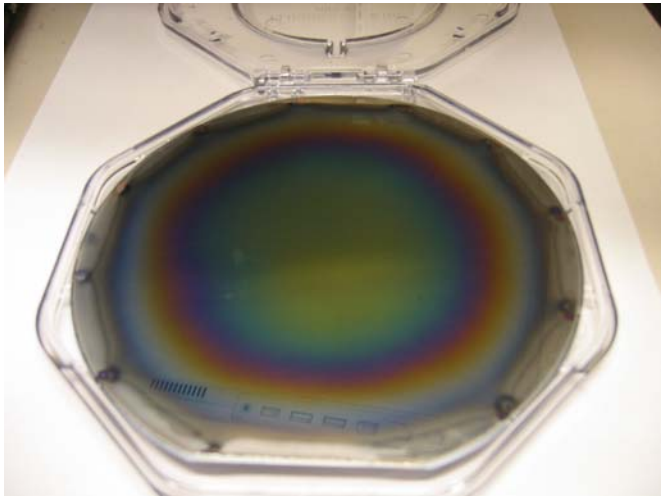
Cu-In phase diagram

Blanket Bonding Experiments

- E-beam deposition of Cu and In multi-layers
- Two different Cu-In stacks bonded to Ta-Cu (TC) stacks
  - TCI: Ta/Cu/In 50/100/300 nm
  - TCIC: Ta/Cu/In/Cu 50/100/520/80 nm
- Bonded to TC (Ta/Cu 50/300 nm) by thermo-compression with 6000 N force (150 mm wafers) and 200°C, followed by anneal for 4 hours at 230°C
- Successful thinning achieved



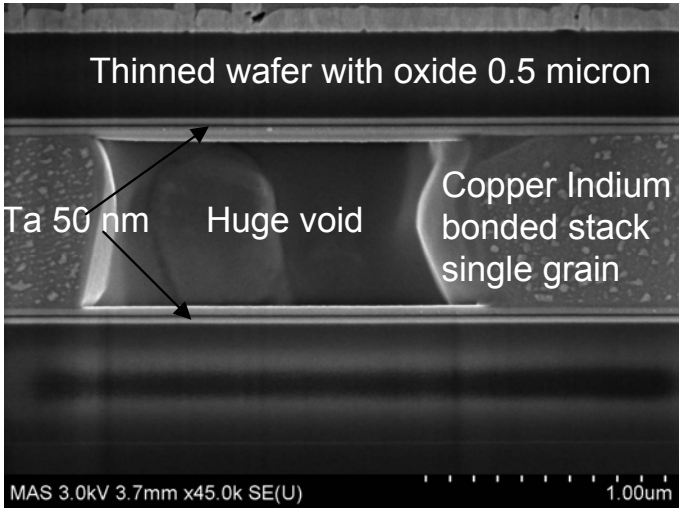
TCIC – TC
After Thinning



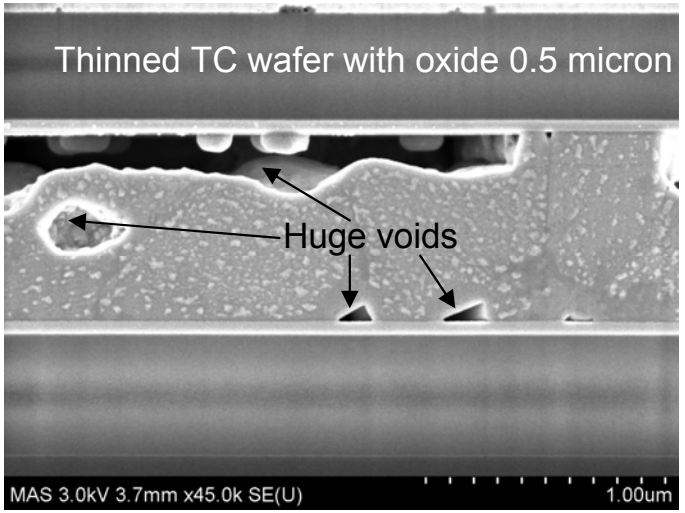
TCI – TC
After Thinning

Bonding Interface Characterization

- Both films shows voids
  - TCI voids go across the bonding interface
  - TCIC voids are located in the TC wafer
- Grain in both films looks homogeneous
- No apparent bonding interface
- STEM suggests that bonded samples have homogeneous Cu and In – no segregation
- $Cu_{11}In_9$ intermetallic compound formed



TCI - TC



TCIC - TC

Outline

- Motivation and Background
- Environmental Impact Assessment Methodology
- Case Study: MIT 3D IC vs. 2D IC
- Assessment of Handle Wafer Options
  - Performance
  - Cost
  - Environmental Impact
    - Energy and Water Consumption
    - Chemical Consumption and Effluents
- Summary

Performance Comparison

Handle Wafer Approaches	Bond strength	Void Formation	Chemical Selectivity	Thinning-back Capability	Temperature range	Time to debond
Smart Cut	2 J/m^2 ✓	Few ↔	Good ✓	Good ✓ < 1 μm	< 250°C, Cu-In bonding at 200°C ↔	Good, released in 60 min ✓
Al Release Layer	3 J/m^2 ✓	No ✓	Probably with TMAH ↔	Good ✓ < 1 μm	Good ✓	Does not release in finite time ✘
Between-Die Channel	3 J/m^2 ✓	No ✓	Probably with TMAH ↔	Good ✓ < 1 μm	Good ✓	Released in 8 hours ↔
Oxide Release Layer	1.6 J/m^2 ✓	No ✓	HF acid highly corrosive ↔	Minimum thickness 10 μm ✓	Higher temperature difficult to release ↔	Release in 45 min ✓

Cost Comparison

Handle Wafer Approaches	New Infrastructure	# of process steps with # of mask	Throughput	New processes/ Process complexity	Yield
Smart Cut	Hydrogen implanter, Oxide bonder	6 with no extra mask	High throughput ion implantation	Oxide bonding, H_2 implantation – expensive	Medium to High
Al release layer	Thick Al sputter, Copper bonder	7 with no extra mask	Very low ~ thick deposition and long release time	20 μm thick Al deposition, Cu bonding	Zero or Negligible
Between-Die Channel	Thick Al sputter, copper bonder	13 with two extra mask	Low ~ thick deposition and long release time	8 μm thick Al deposition, Cu bonding, silicon etch	High, needs development for effective release
Oxide release layer	DRIE silicon etcher, Oxide bonder	8 with one extra mask	Moderate, 2 hr DRIE; can reuse handle wafer	Silicon etch, oxide bonding	Low to moderate, needs more development

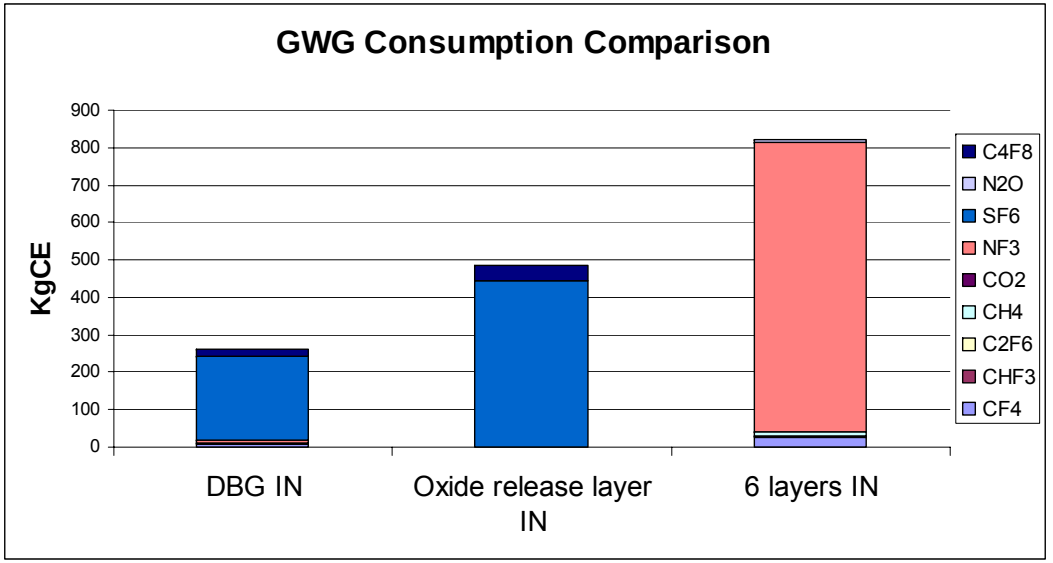
Environmental Comparison – Energy and Water

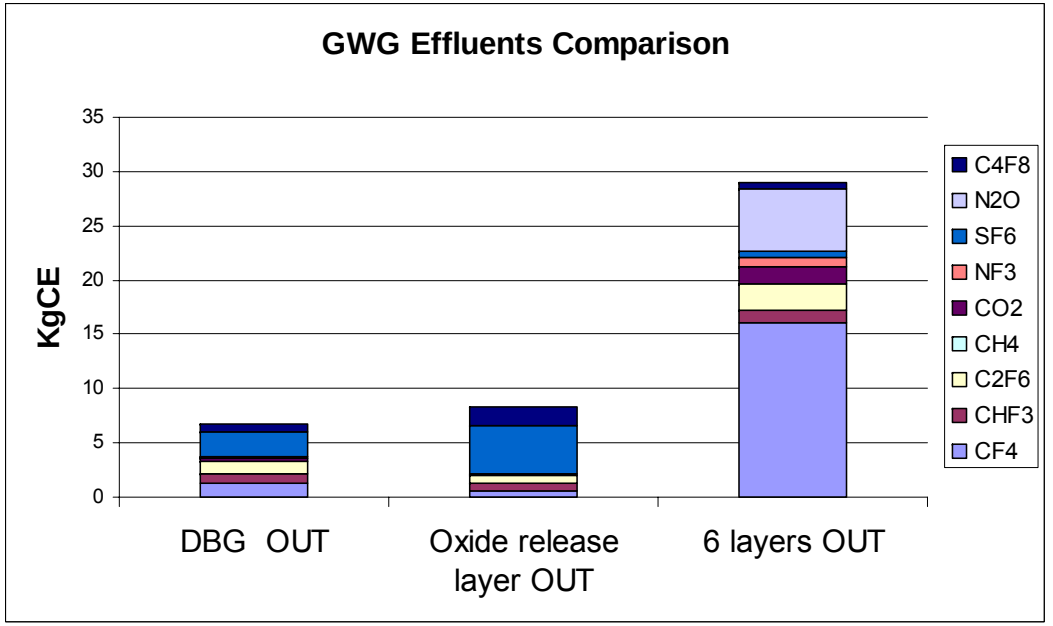
- Al release is the most energy and PCW expensive process, followed by between-die channel approach
- Smart Cut looks most promising in terms of environmental footprint
  - No acid release and no thick sacrificial layer or deep channel etching

Handle Wafer Approaches	Energy Consumption (KWh)	Ultra pure water (m^3)	Process Cooling Water (m^3)	Waste water generated (m^3)
Al Release Layer	296, thick Al deposition 40 micron	0.5, acid release	14.7, deposition and oxidation	~1, acid release, generates water containing $AlCl_3$
Between-Die Channels	240, thick Al deposition, All 6 layers of IMD and 50 µm silicon etching	0.62, acid release and clean	9.7, oxidation, deposition and etching	~1, acid release, generates water containing $AlCl_3$
Oxide Release Layer	60, 50 µm of silicon etching	0.73, acid release, activation	2.9, oxidation and etching	~1, waste water from acid and activation
Smart Cut	20, assumed H_2 implantation is similar to other implantation process	0.43, activation	4.71, oxidation and implantation	~0.5, waste water from activation

Global Warming Gases Comparison

- Consumption and effluents for oxide release layer and between-die channels are compared with 6 metal layer CMOS device, 130 nm technology node, 300 mm wafer
  - Smart cut and Al release layer steps release little GWG
  - Destructive efficiency
    - SF_6 assumed to be 90%
    - *c*-C_4F_8 assumed to be 80 %
- Result: Si etching using Bosch process is not environmentally benign





Summary: Integrated Assessment of Handle Wafer Options

- Al Release Layer – no functionality (low-yield) and high environmental footprint
- Between-Die Channels – high yield with large environmental footprint and low-throughput (moderate cost)
- Smart Cut – high yield, low environmental impact but high cost
- Oxide Release Layer – cost and environmental footprint are within limits because of reuse, and performance is moderate (can be improved)

	Al Release Layer	Between-Die Channel	Smart Cut	Oxide Release Layer
Performance	✗	✓	✓	●
Cost	✗	●	✗	✓
Environmental Impact	✗	✗	✓	●

Outline

- Motivation and Background
- Environmental Impact Assessment Methodology
- Case Study: MIT 3D IC vs. 2D IC
- Assessment of Alternative Handle Wafer Options
- Summary

Summary

- Developed an environmental assessment methodology for evaluating emerging silicon technologies
  - Applied to MIT "back-to-face" 3D IC in comparison to standard 2D IC
  - Identified handle wafer as process which is environmentally non-friendly and lacking in performance
- Furthered the development of three handle wafer options
  1. Between-Die Channels
     - Can be released in 8 hours, satisfy all other requirements
  2. Oxide Release Layer
     - Can be released in 45 min, satisfy all requirements but chemical selectivity
  3. Alternative Low-Temperature Permanent Cu-In Bonding
     - Can be bonded at 200^{o}C; needs further work to deposit smooth films
- Demonstrated an overall evaluation of competing technologies by comparing these two novel approaches with prior approaches for handle wafers on all three axes – performance, cost and environmental impact

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