Challenges of Emerging Nanotechnologies for Low Power High Performances Logics

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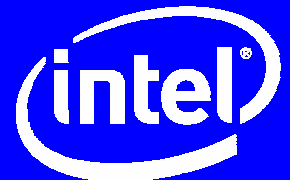
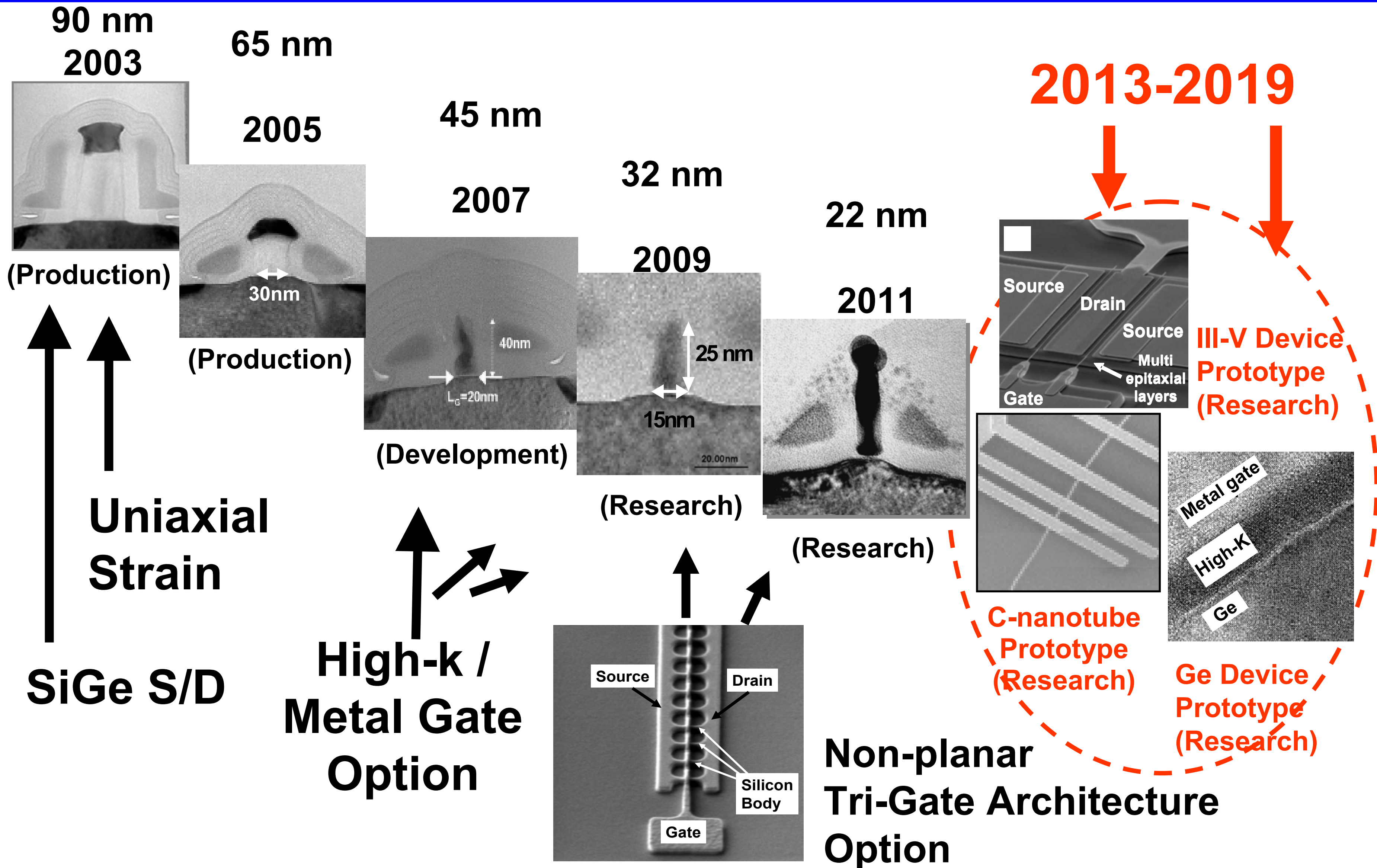
Intel Corporation

NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

Feb, 2006



Transistor Scaling and Future Options

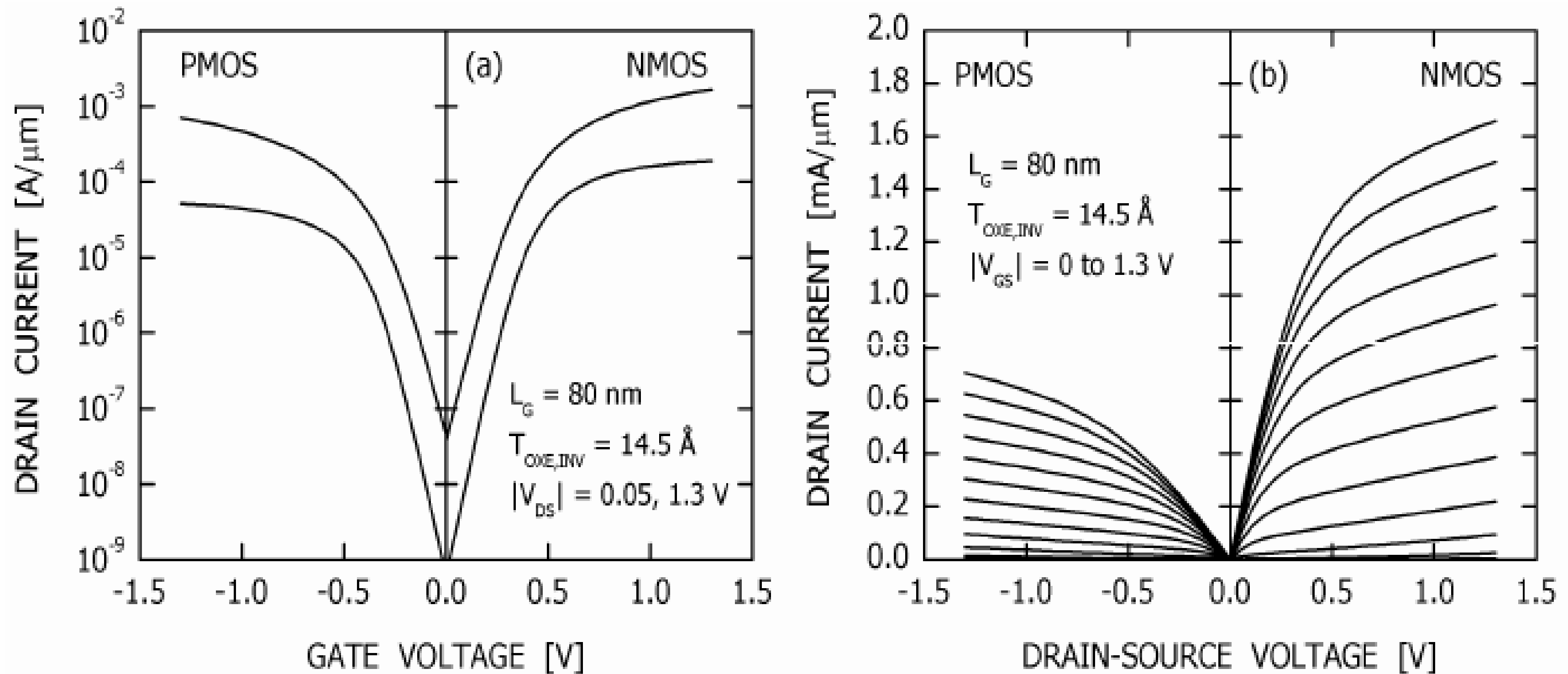


source: Intel

New Research Should be Directed Toward 22nm and Beyond

- Environment
  - 2 billion transistor chips
  - > 25 GHz clock speed
  - MOS gate dimensions < 10nm, EOT < 0.5nm
  - < 0.8 V operation
- Revolutionary, new Cool Ideas for high speed logic, memory
  - Very low impedance interconnect
  - High speed/low power transistor alternatives
  - Thermal and power delivery solutions
  - Stable, fast memory cell/architecture
- Encourage work on CMOS extensions and novel technologies that are compatible with silicon infrastructure
  - **High mobility channel devices, e.g. nanowire, Ge, III-Vs**
  - Devices beyond CMOS, with collateral interconnect, memories…

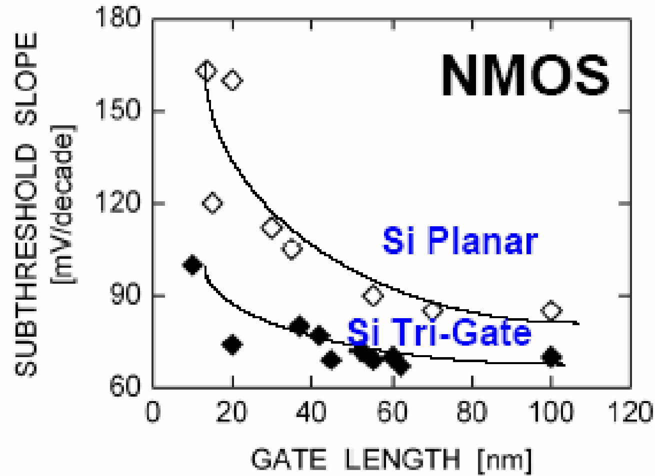
High k-metal gate Si transistor

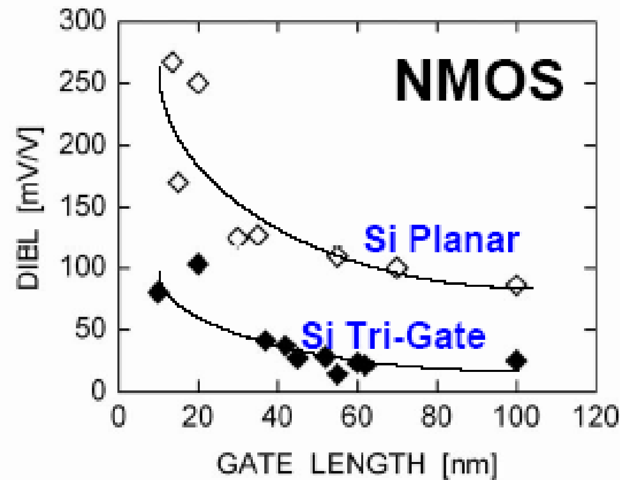


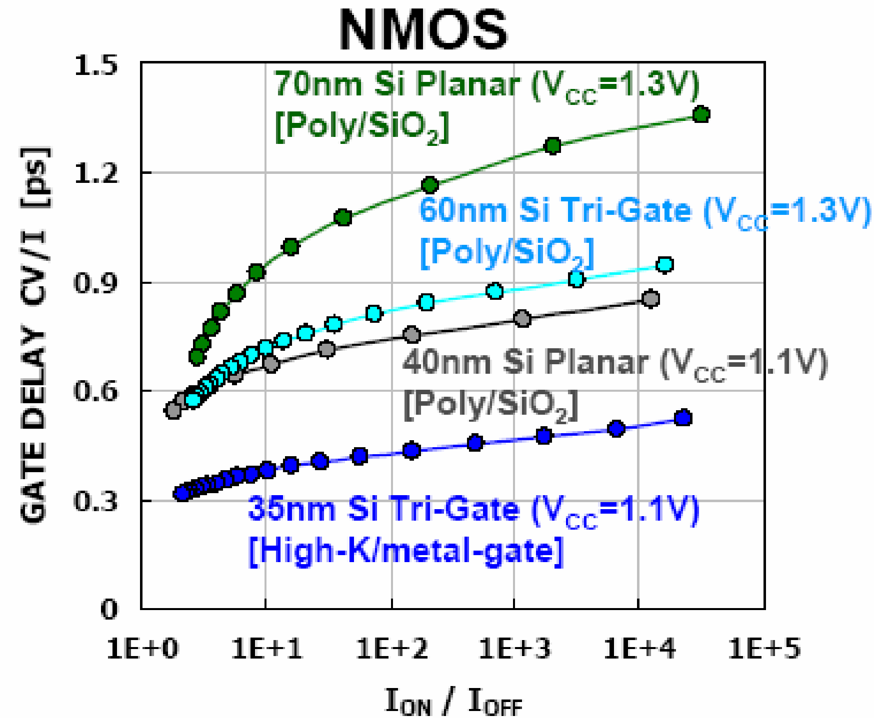
- **Example of high-performance CMOS transistors on bulk-silicon with high-K/metal-gate**
  - **Correct V_{TH}'s, high-mobility, low gate leakage**

R. Chau etal., EDL, 25, p408 (2004)

Planar vs non-Planar Si transistor



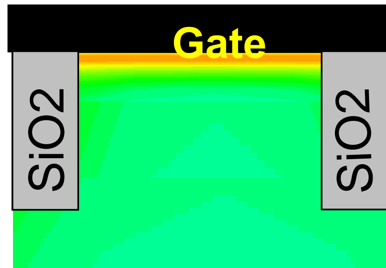




- Need to benchmark emerging non-Si nanoelectronic devices versus these conventional planar and non-planar Si NMOS transistors

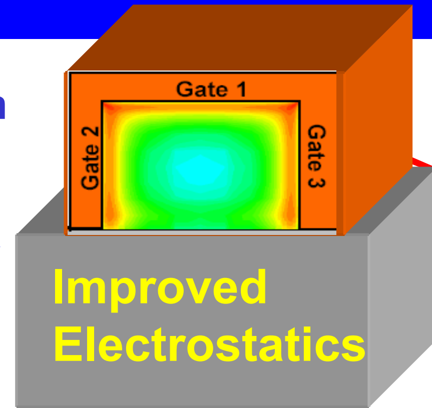
R. Chau, INFOS, Leuven, 6-2005

Device Evolution and Challenges



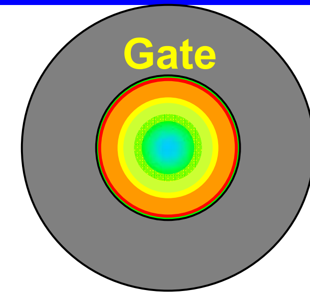
Conventional planar

Can happen as early as 2007



Trigate FET

2013



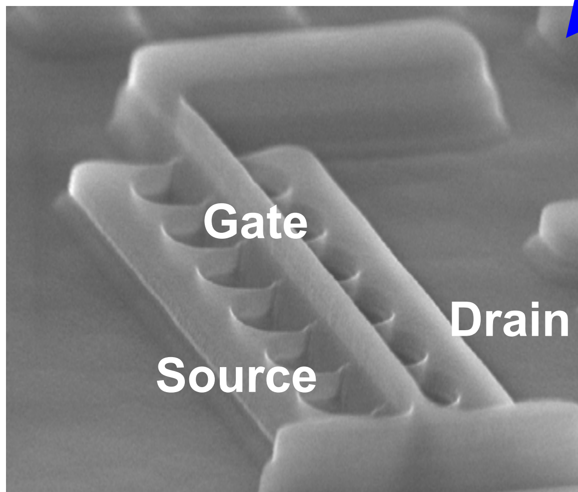
Nanowire/Nanotube

Very conventional processing (being done in 300mm Fab)

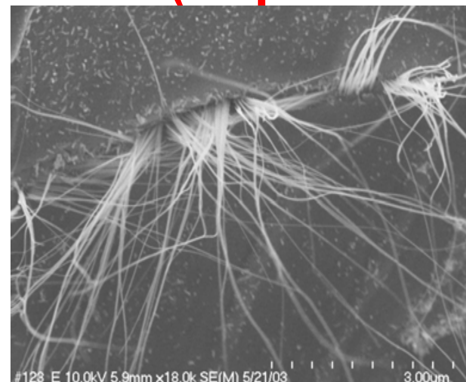
Many fundamental material issues to overcome

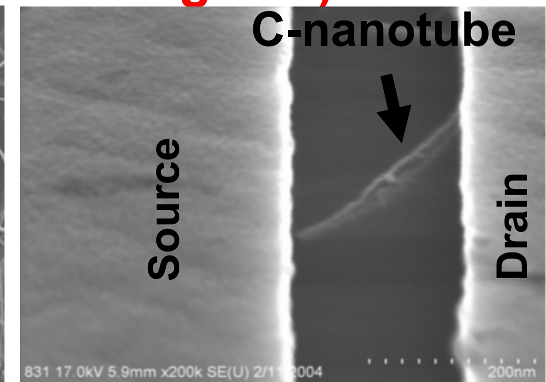
- chirality issue
- positioning issues

(require >10 billion gates)



Si Tri-gate Architecture





R. Chau, VLSI 2005

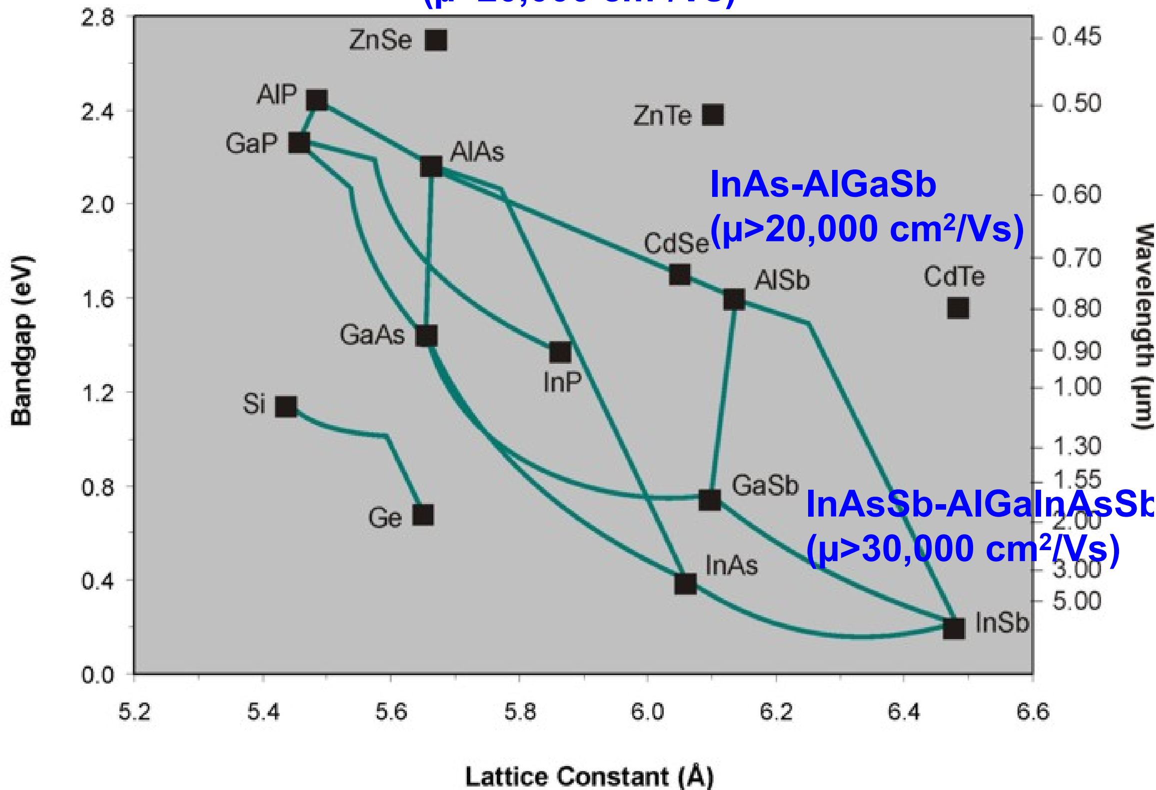
Why IIIV compound semiconductor ?

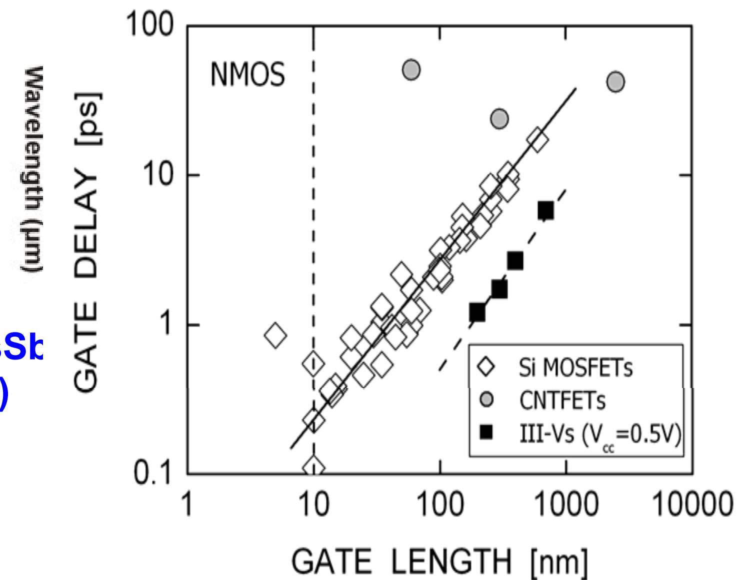
	Si	GaAs	$In_{.53}Ga_{.47}As$	InAs	**InSb**
Electron Mobility ($cm^2V^{-1}s^{-1}$) $n_s=1x10^{12}/cm^2$)	**600**	**4,600**	**7,800**	**20,000**	**30,000**
Electron Saturation Velocity (10^7 cm/s)	1.0	1.2	0.8	3.5	**5.0**
Ballistic Mean Free Path (nm)	28	80	106	194	**226**
Energy Band-gap	1.12	1.42	0.72	0.36	**0.18**

Channel Material Properties at 295K

InSb shows the highest room temperature electron mobility, but also the lowest energy band-gap

High mobility channel devices using III-V compound semiconductor

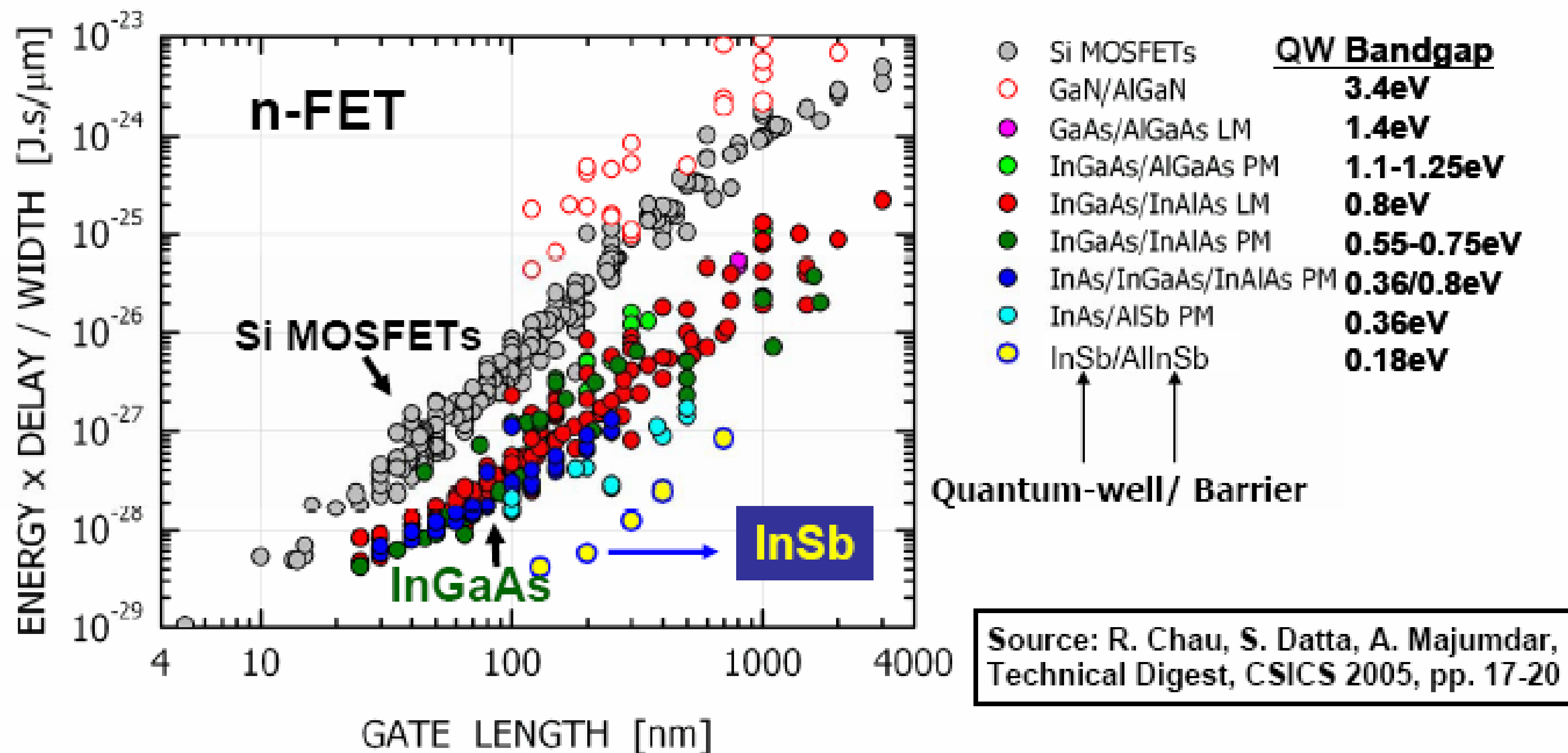




R. Chau etal ICSICT, 2004

III-V (InSb, InAs) devices show significant CV/I improvement over Si
III-V devices have >50X higher effective n-ch mobility than Si and operated at low VCC = 0.5V

III-V Nanoelectronics: Low Energy-Delay Product



- Of all the III-V quantum-well systems, InSb QW has the lowest energy-delay product [highest electron mobility, lowest band gap, lowest V_{CC} (0.5V)]
- InGaAs QW is also important for low V_{CC} (0.5V-0.7V)

Low power-high performance III-V FET Devices

Top-Down Approach: conventional litho/pattern techniques

Cutoff Frequency, fT (GHz)

180
160
140
120
100
80
60
40
20
0

1
10
100
1000

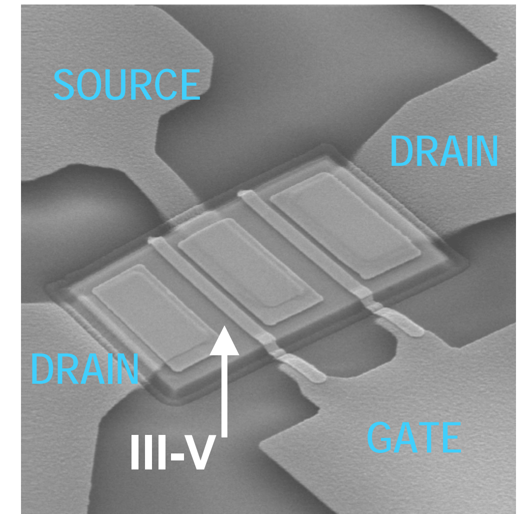
Power Dissipation (mW/mm)

III-V FETs
(Lg~200nm)

Si FETs
(Lg~80nm)

5-10X
Lower Power
Dissipation

InSb Vds=0.3V
InSb Vds=0.5V
InSb Vds=0.6V
InSb Vds=0.7V
Si Vds=0.5V
Si Vds=0.7V
Si Vds=1V
Si Vds=1.2V



S. Datta, R. Chau et al.
ICSICT 2004, Beijing.

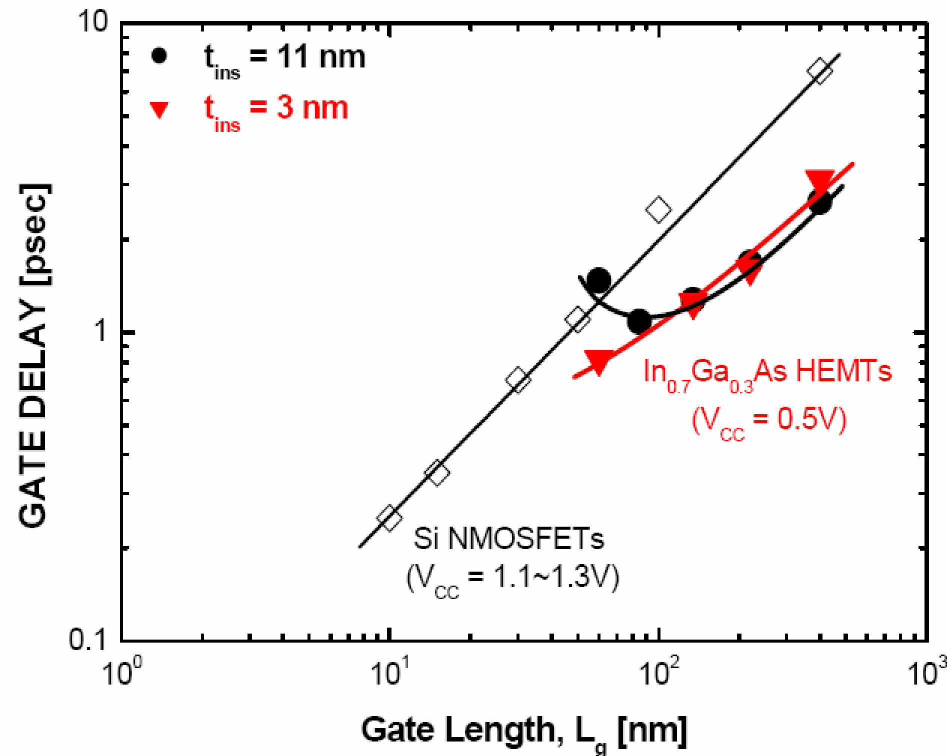
World's first depletion-mode InSb NMOS research transistors demonstrated with 200GHz cut-off frequency (FT) achieved at Vcc = 0.5V

Challenges of Heterogeneous Integration of IIIV/Si

- Self aligned architecture to minimize parasitics and footprint
- Lg Scalability
- IIIV epi growth on 300 mm Si
- P channel device (strain in IIIV ?)
- Low Conduction Band density of states ?
- High k on IIIV (last but definitely not least)

Logic Suitability of InGaAs HEMT

MIT - J. Alamo



- **III-V QW devices show very high performance at low Vcc (0.5V), compare favorably with 65 nm Si CMOS**

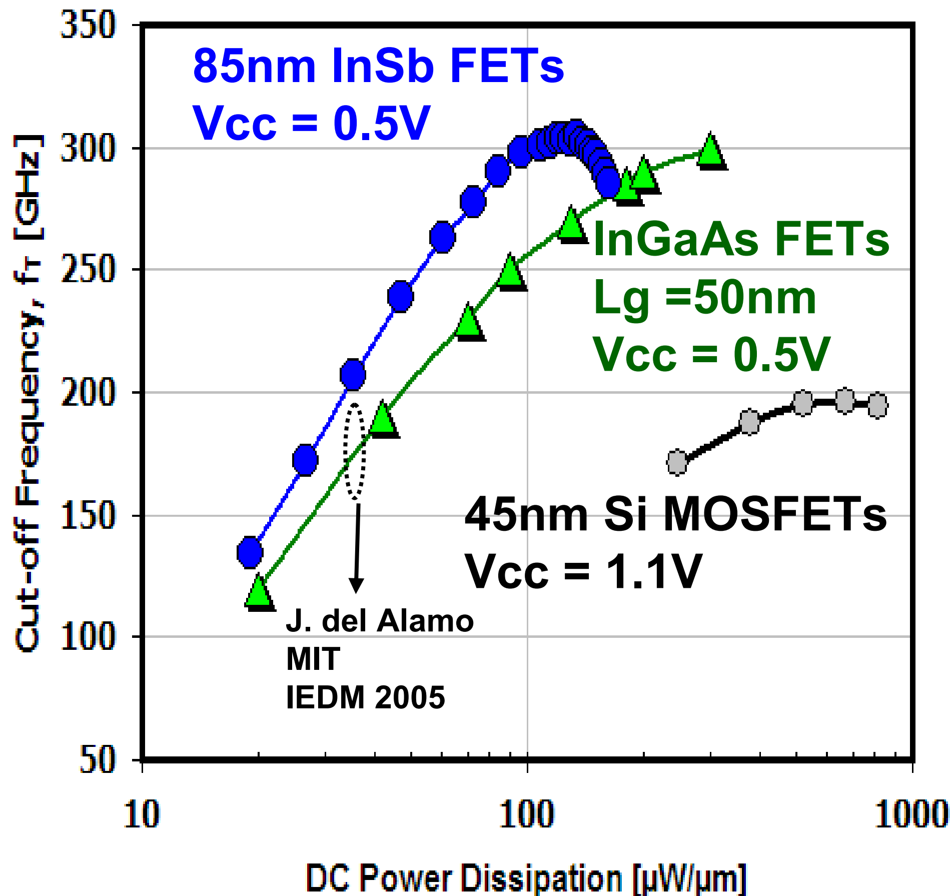
D. Kim, J. Alamo etal., IEDM 2006

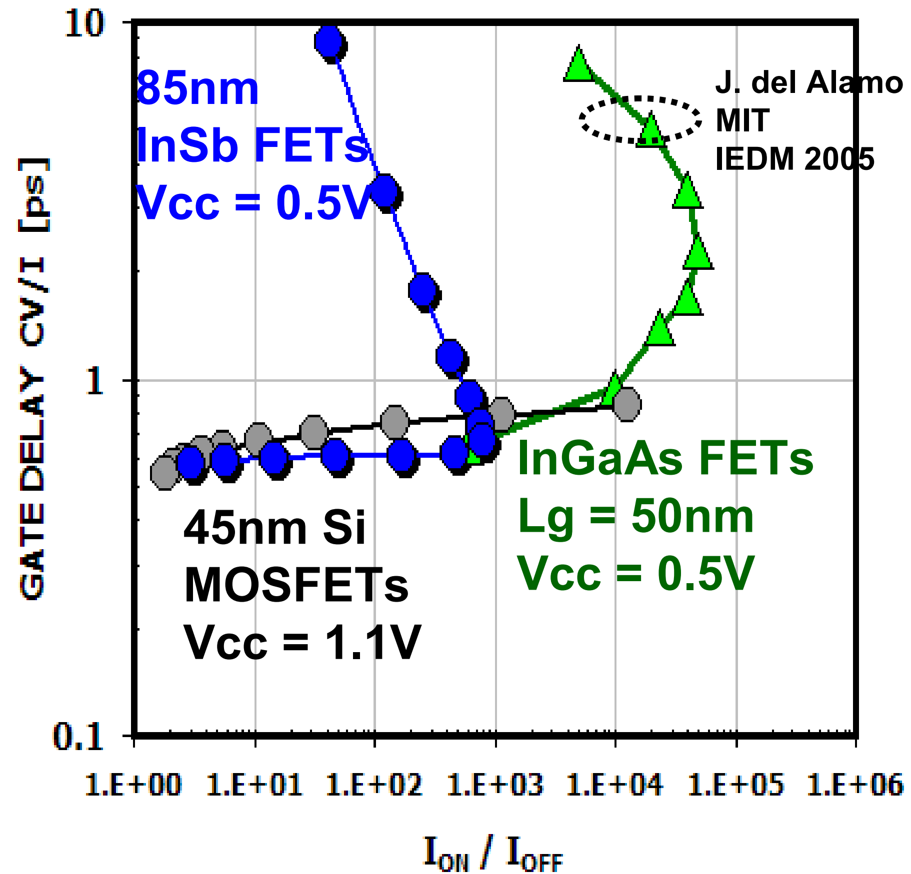
@V_{dd}=0.5 V	L_g (nm)	I_{on} (mA/mm)	I_{leak} (nA/mm)	S (mV/dec)	DIBL (mV/V)	V_t (V)
InGaAs HEMT	60	370	300	88	93	-0.02
65 nm CMOS (low power)	55	150	300	90	80	0.5

For the same I_{leak}, 60 nm InGaAs HEMT yields 45% more I_{ON} than 65 nm CMOS

Logic Suitability of InGaAs HEMT

MIT - J. Alamo





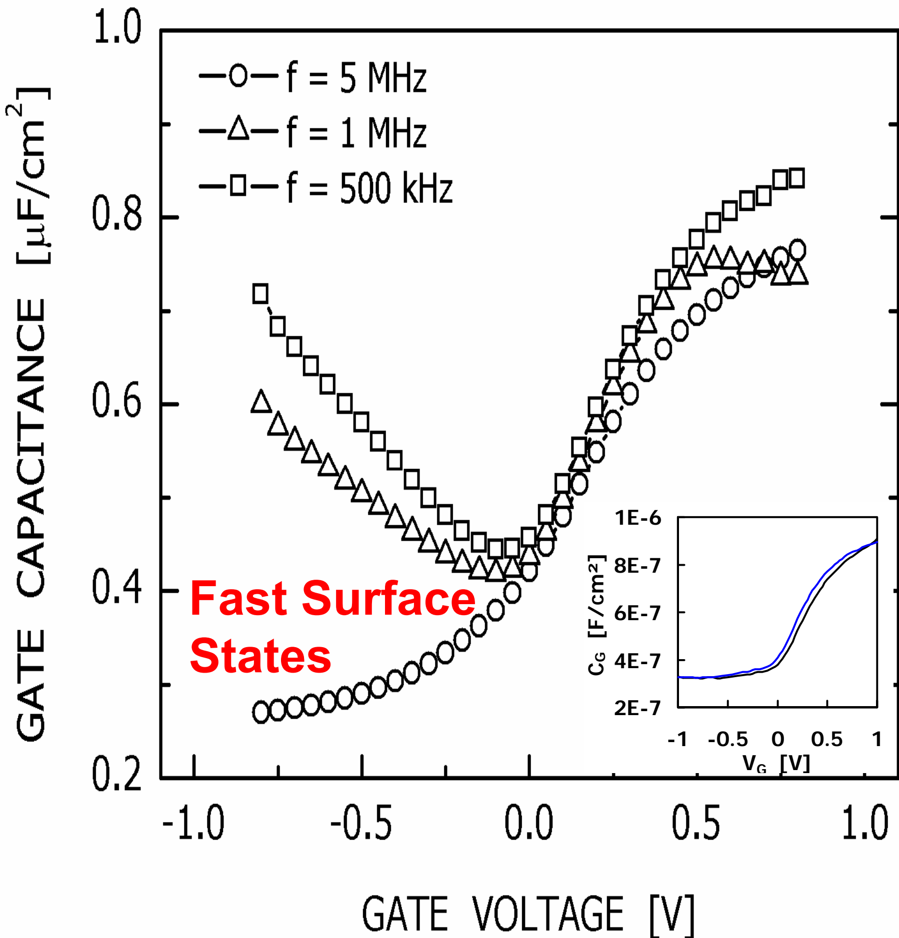
- **III-V QW devices show very high performance at low Vcc (0.5V), compare favorably with 65 nm Si CMOS**

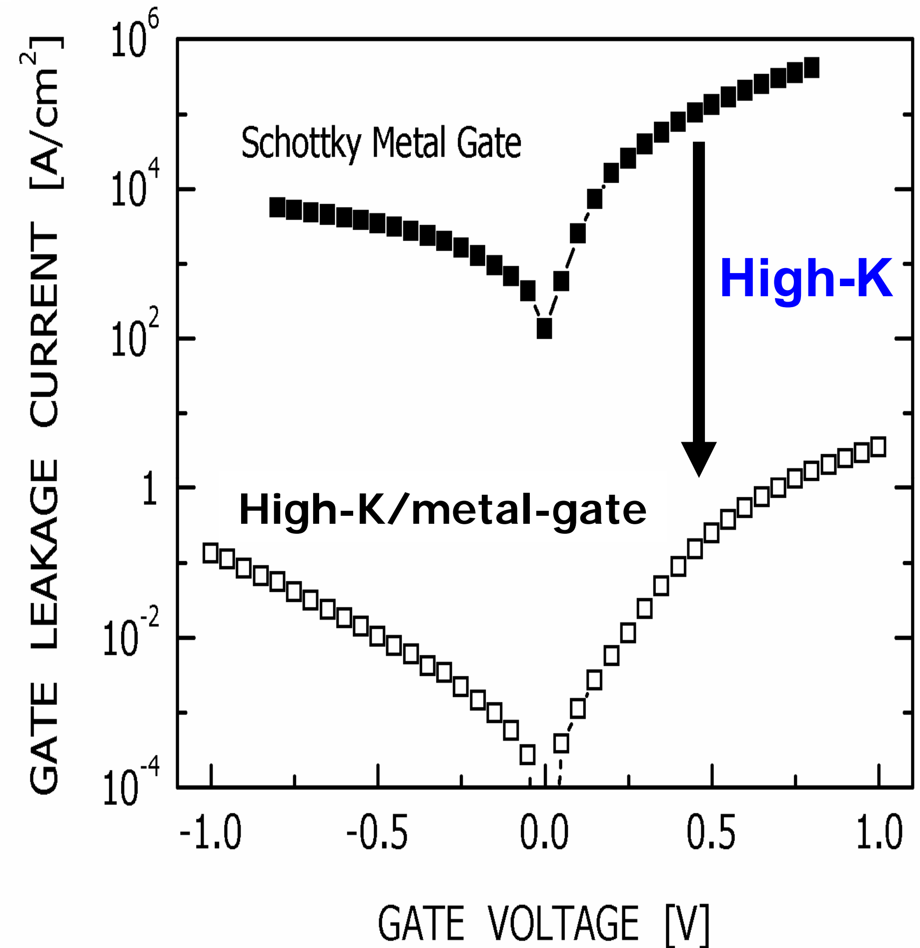
R. Chau, DRC Conf, 6-2006

Grand Challenge in III-V Nanoelectronics:

Compatibility of III-V and High-K/Metal-gate Stack

AlInSb/High-K/metal-gate



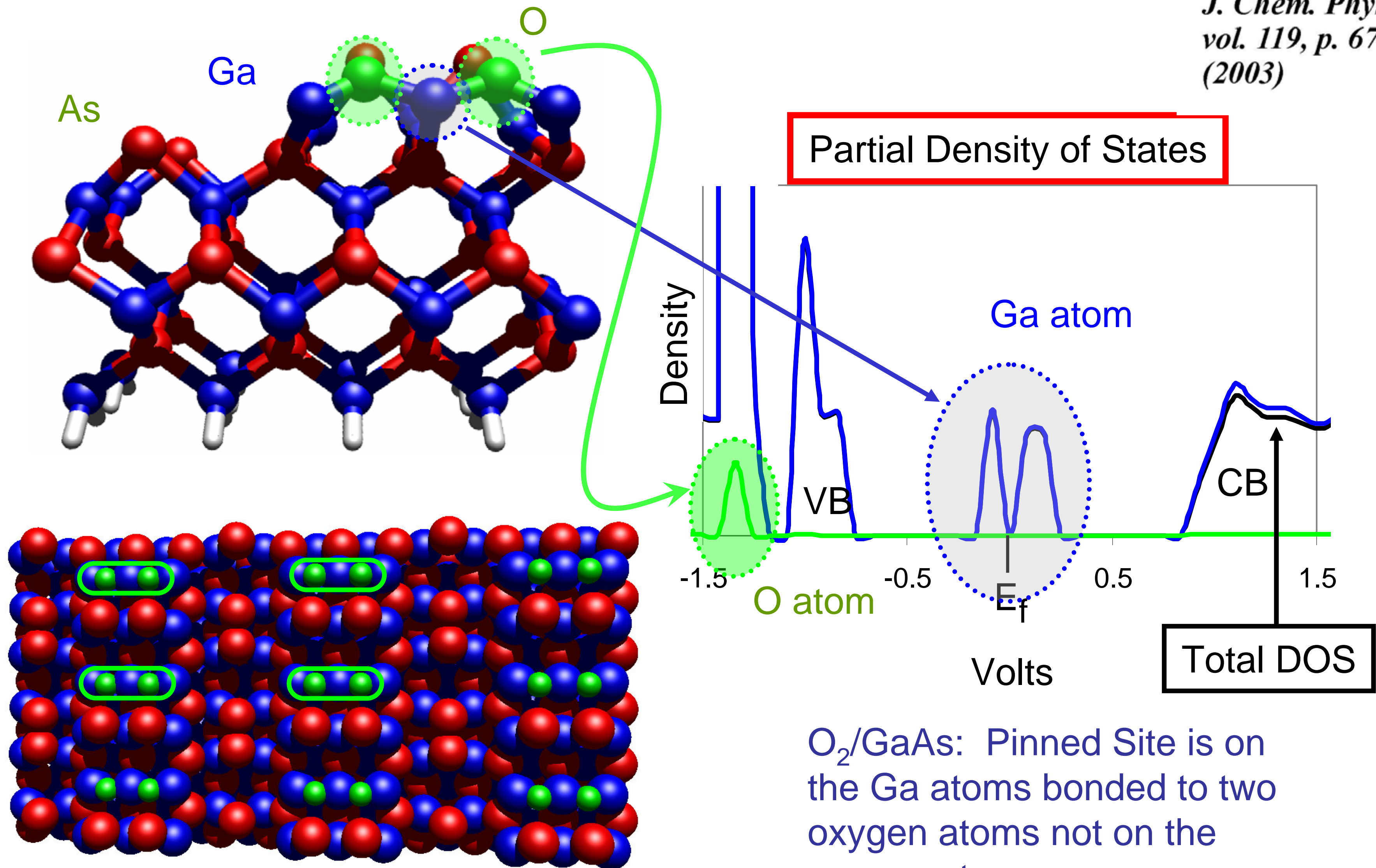


R. Chau , INFOS, Leuven 6/05

Fermi level pinning at insulator can turn off underlying enhancement mode channel and increases large resistances, it is critical to understand the underlying mechanism….

DFT Calculation of DOS and PDOS for O_2/GaAs

M.J. Hale et al. J. Chem. Phys. vol. 119, p. 6719 (2003)



O_2/GaAs: Pinned Site is on the Ga atoms bonded to two oxygen atoms not on the oxygen atoms or excess arsenic

A. Kummel, UCSD

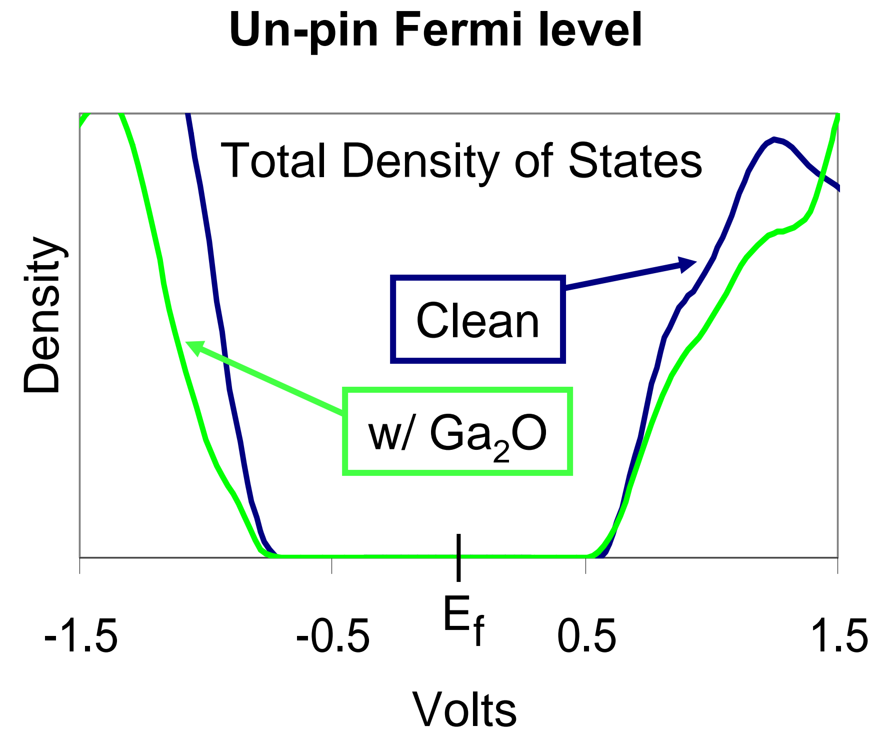
DFT Calculation of DOS of Ga_2O/GaAs Interface

Ga_2O

O

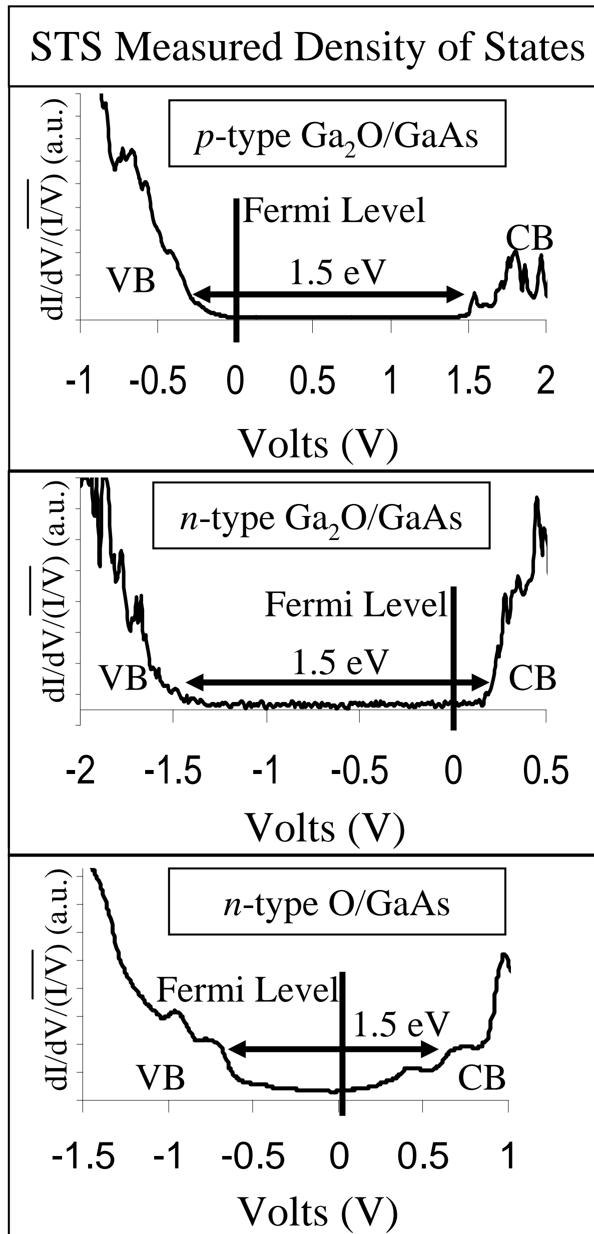
Ga

As



Ga_2O/GaAs: The oxygen bonded Ga has no states in the bandgap

A. Kummel, UCSD



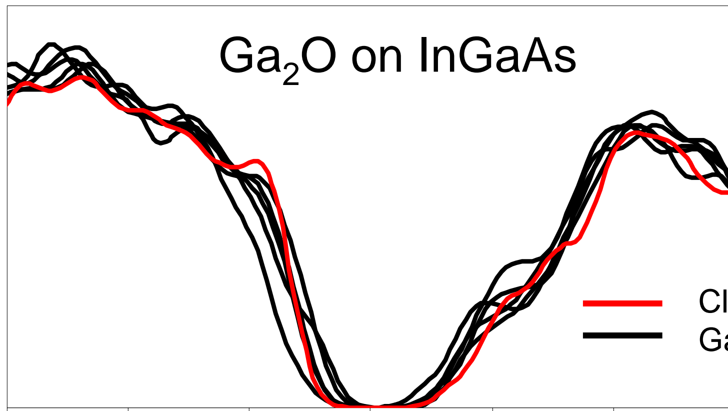
STS (dI/dV)/I/V Studies to show Fermi level pinning and unpinning

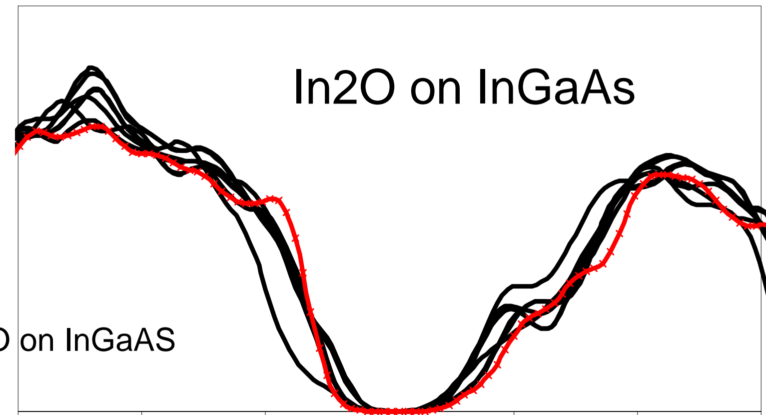
- O_2 or O dosing pins the Fermi level. The OV position is mid-gap for both n-type and p-type wafers
- The Ga_2O deposition leaves the surface unpinned. The OV position moves from the valence to the conduction band edge when comparing p-type and n-type wafers

A. Kummel, UCSD

Ga2O & In2O on InGaAs(100)

A. Kummel, UCSD





- DFT shows that Ga2O and In2O on InGaAs(100) to be un-pinned. STM experiments in progress.

Side View

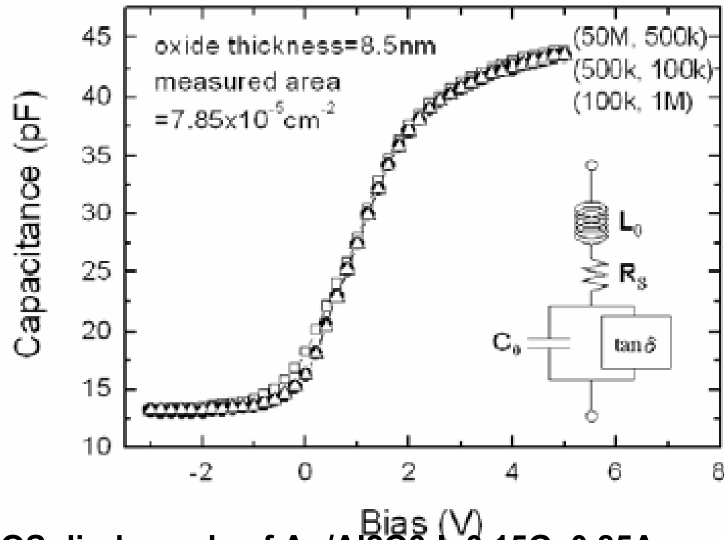
Top View

As
Ga
In
O

Ga$_2$O on InGaAs

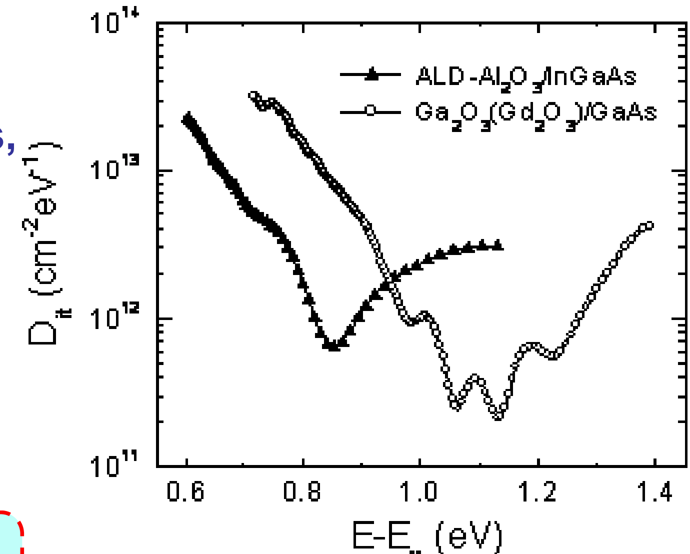
$Ga_2O_3(Gd_2O_3)$ and JVD (MAD) Si_3N_4 on InGaAs

Tsinghua- M. Hong, J. Kwo, Yale – T.P. Ma, Intel- J. Zheng

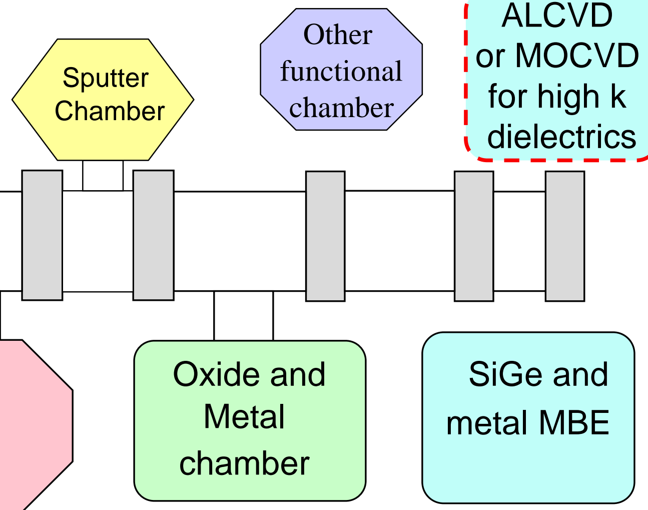


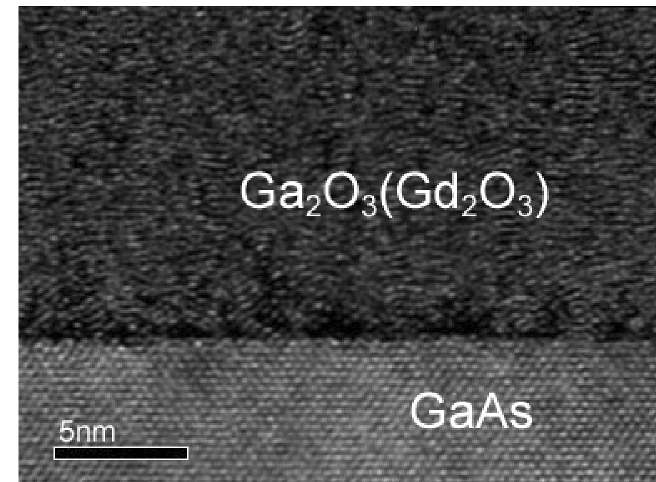
MOS diode made of Au/Al2O3-In0.15Ga0.85As

M. Hong etal., ECS, Los Angeles, 2005



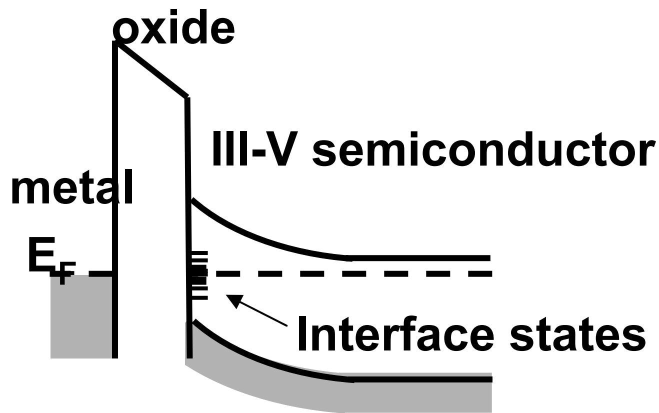
Dit's for ALD-Al2O3/InGaAs and for UHV deposited Ga2O3 (Gd2O3) on GaAs

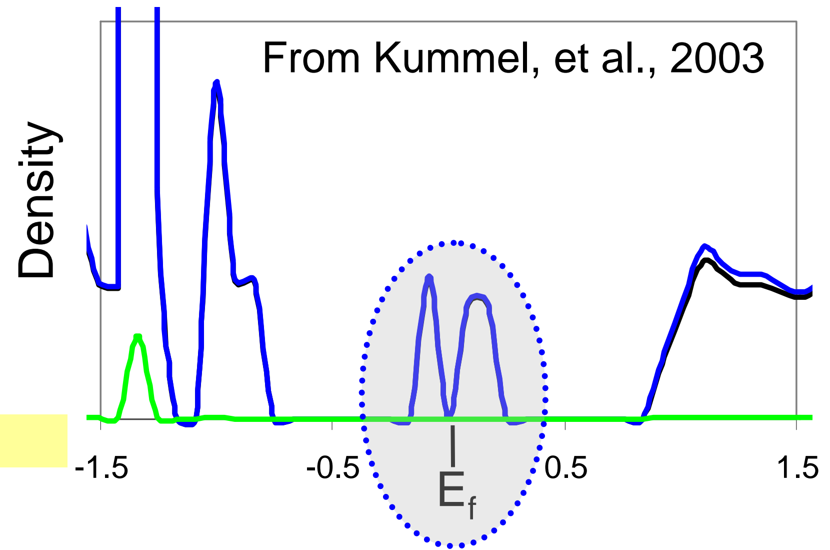




In-situ Fabrication: UHV Integrated MBE IIIV-high k

Fermi Level Pinning Issue

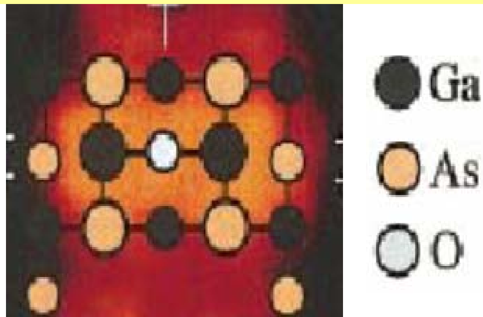




O_2 or O dosing pins the Fermi level in mid-gap

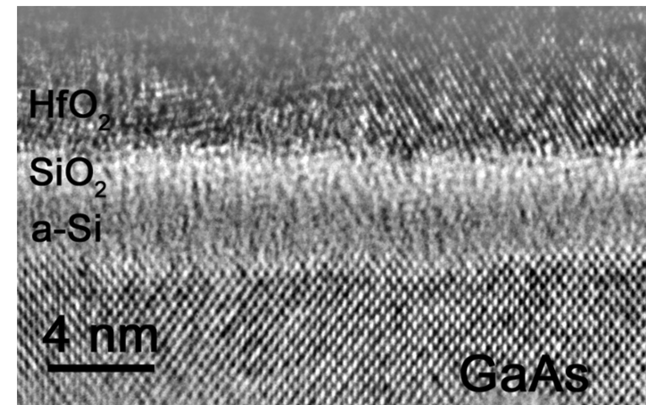
Fermi level control options:

Control of interface atomic structure
(e.g. "good" Ga_2O)



From Kummel, et al., JCP, 2003

Prevention of interface oxidation
(e.g. passivation with Si)



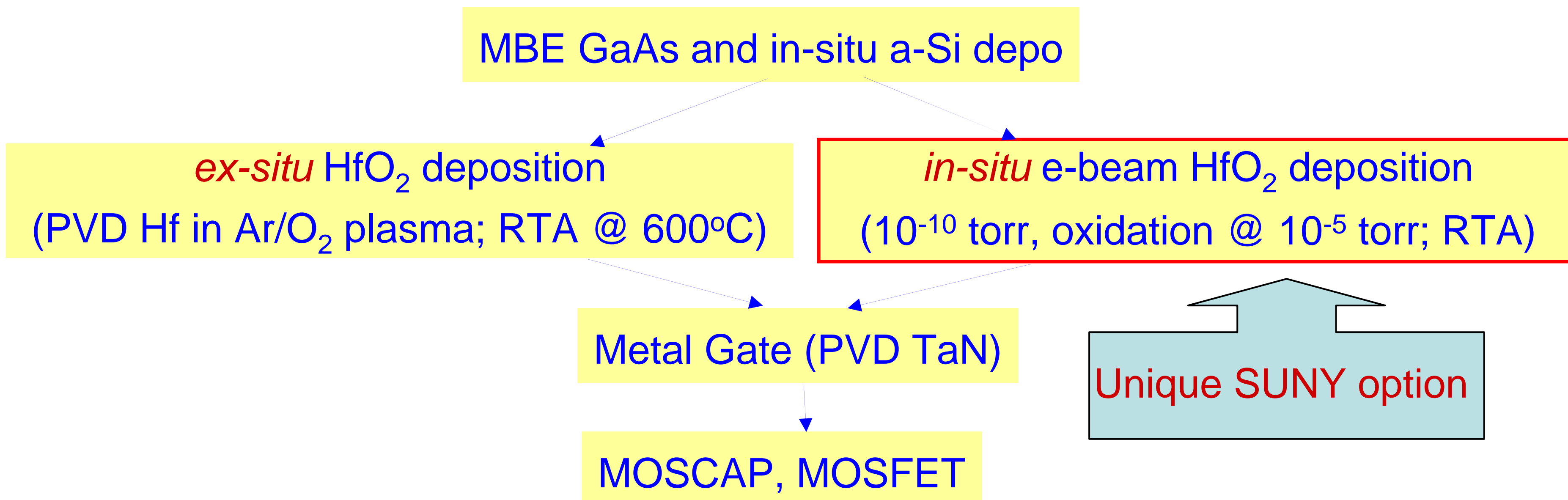
approach 1

1. MBE *in-situ* passivation with α-Si (SUNY):

- MBE of α-Si near room temperature (high As content in a-Si)
- Si remains amorphous even at high temperatures (up to 800°C)

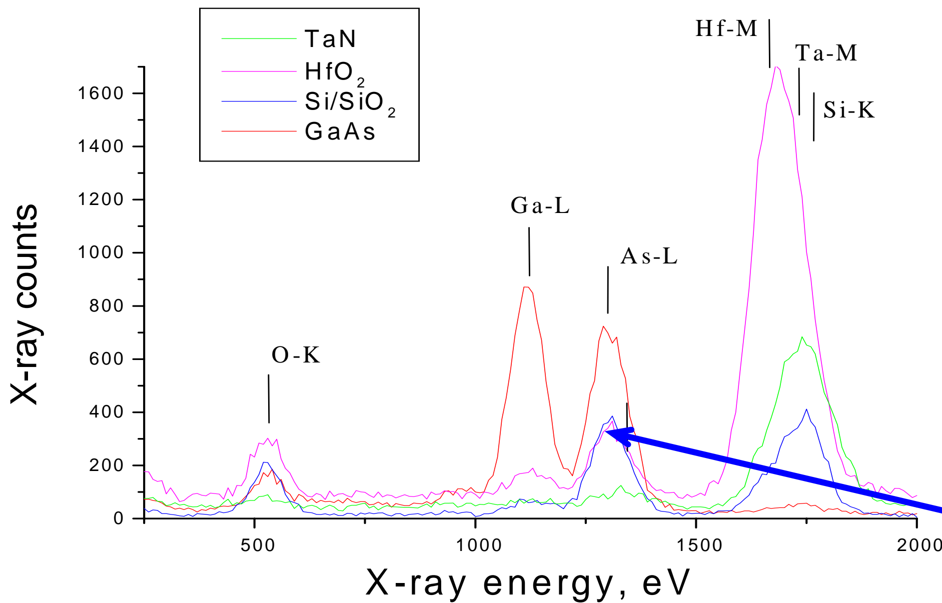
Published: S. Oktyabrsky, V. Tokranov, M. Yakimov, R. Moore, S. Koveshnikov, W. Tsai, F. Zhu, and J.C. Lee, "High-k gate stack on GaAs and InGaAs using in situ passivation with amorphous silicon." Materials Sci. Eng. B, **135** 272-276 (2006).

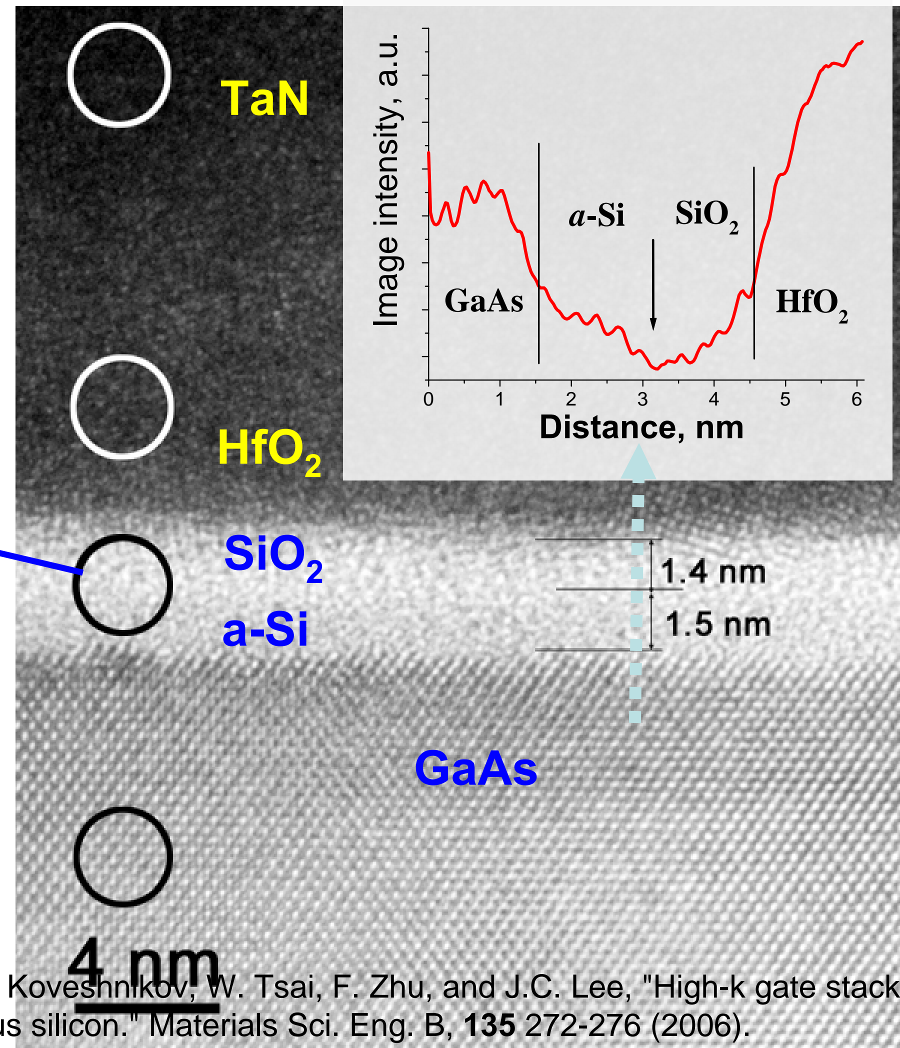
High-k Deposition Options:



GaAs with MBE Si and *ex-situ* HfO_2 gate stack

- 2.5 nm *a*-Si layer and 10 nm PVD HfO_2
- 3 days air exposure prior to PVD





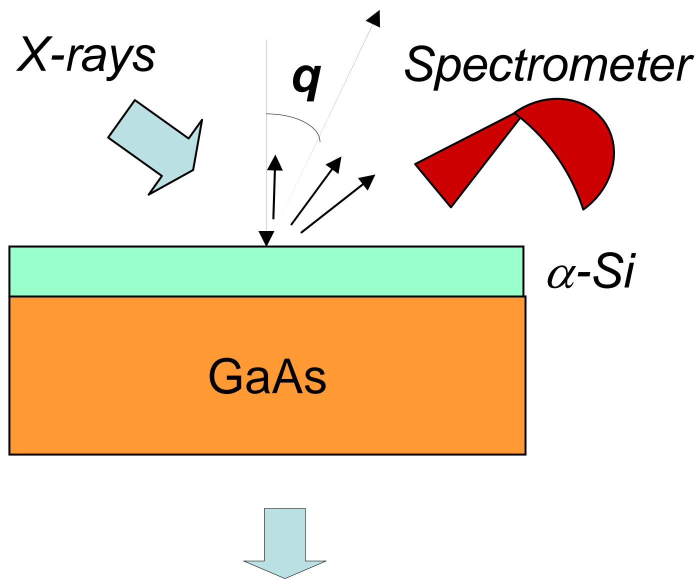
- Sharp GaAs/Si interface
- Si layer is partially oxidized
- High As content in Si layer

Published: S. Oktyabrsky, V. Tokranov, M. Yakimov, R. Moore, S. Koveshnikov, W. Tsai, F. Zhu, and J.C. Lee, "High-k gate stack on GaAs and InGaAs using in situ passivation with amorphous silicon." Materials Sci. Eng. B, **135** 272-276 (2006).

Role of α-Si in preventing Fermi level pinning

- GaAs samples without and with Si
- 20 minutes sample transfer from MBE to XPS

Angle-resolved XPS:



- XPS at glancing angle gives ~30-50 at. % of As
- $AsSiO_x$ in Si is different from AsO_x in GaAs
- Si layer is partially oxidized

$AsSiO_x$ in Si

AsO_x in GaAs

AsO_x As

0 Å Si

surface

$AsSiO_x$

15 Å Si

surface

Intenity, a.u.

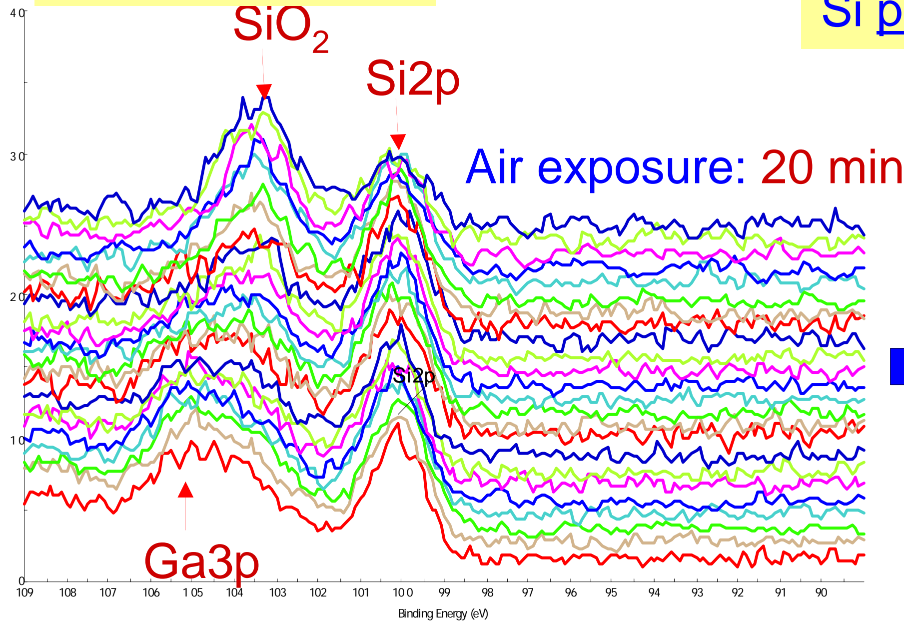
Angle to sample-normal

1330 1325 1320

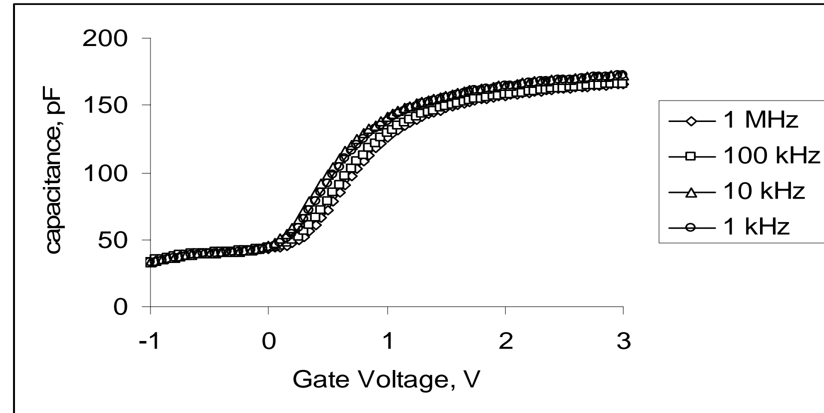
Binding energy, eV

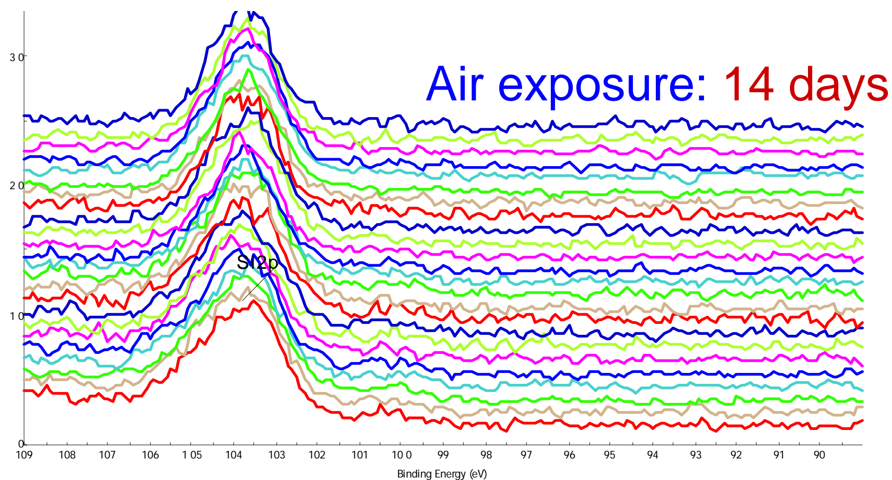
Published: S. Oktyabrsky, V. Tokranov, M. Yakimov, R. Moore, S. Koveshnikov, W. Tsai, F. Zhu, and J.C. Lee, "High-k gate stack on GaAs and InGaAs using in situ passivation with amorphous silicon." Materials Sci. Eng. B, 135: 272-276 (2006).

Role of α-Si in preventing Fermi level pinning

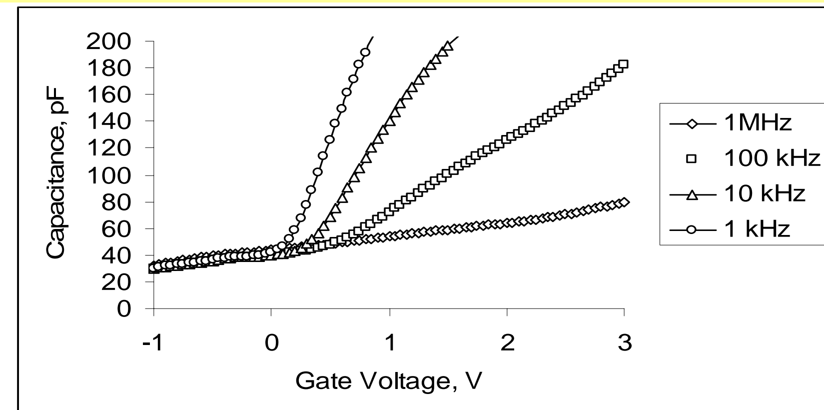


Si partially oxidixed – Fermi level is **not** pinned





Si is fully oxidixed – Fermi level is pinned

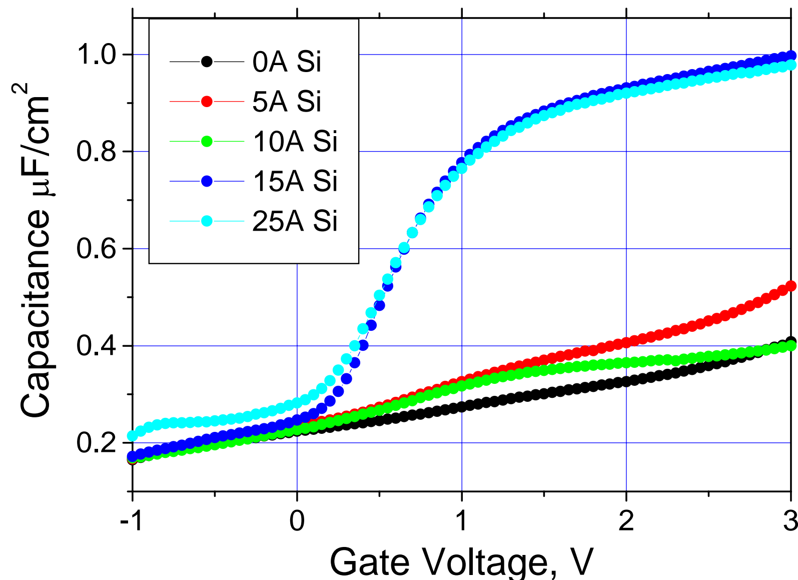


S. Koveshnikov, W. Tsai , I. Ok and J.C. Lee, V. Torkanov, M. Yakimov, and S. Oktyabrsky, " Metal-Oxide-Semiconductor Capacitors on GaAs with High-k Gate Oxide and Amorphous Silicon Interface Passivation Layer." Appl. Phys. Lett., 88, 02210

Scaling of *in-situ* α-Si and *ex-situ* HfO_2

α-Si scaling (10nm HfO_2)

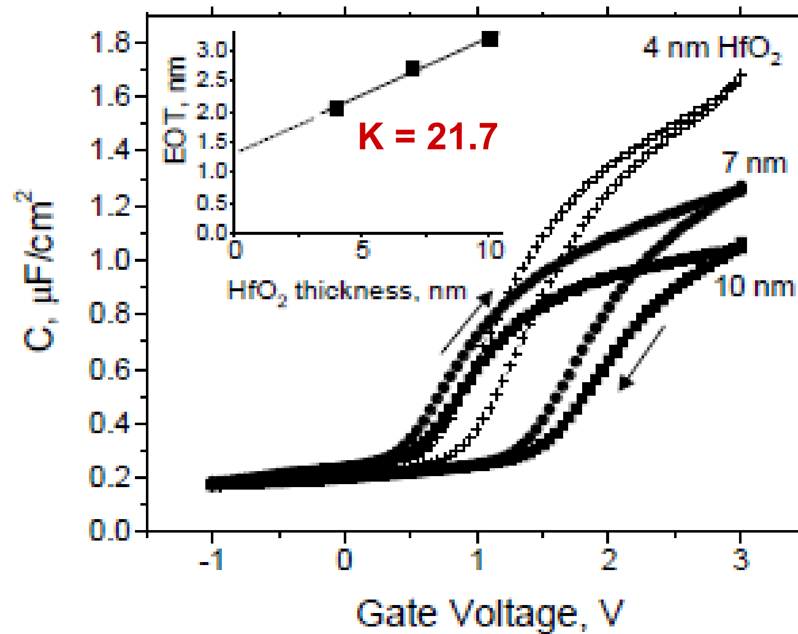
- *ex-situ* HfO_2 by PVD in Ar/O_2 plasma
- PDA at 600°C/5min in N2
- TaN as a metal gate

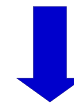


Minimum Si Cap thickness to prevent Fermi level pinning is ~1.5 nm

HfO_2 scaling (1.5 nm Si)

Hysteresis dependence on HfO_2 thickness in n-MOSCap



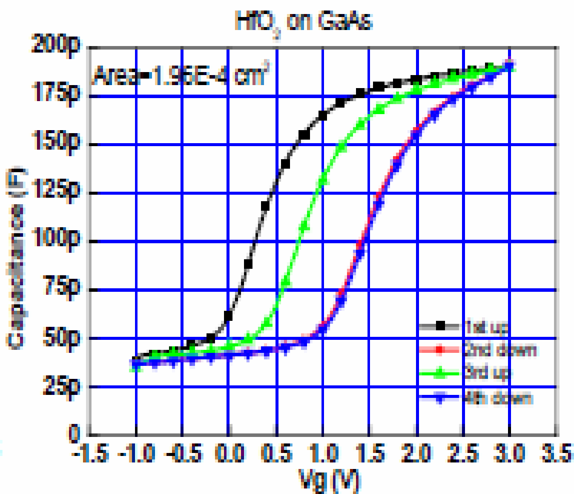


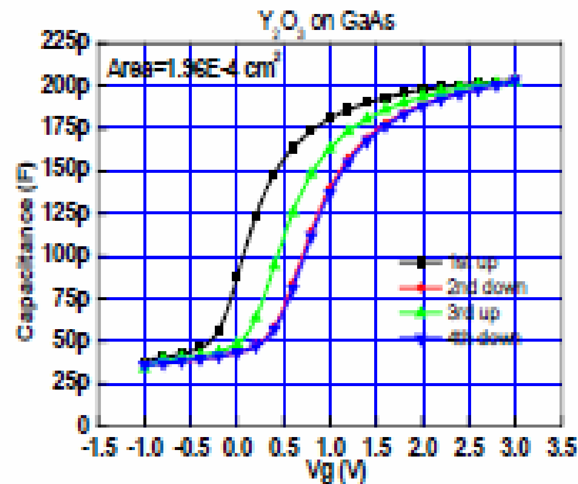
- k-value of the HfO_2 gate oxide ~21-22
- Oxidized Si is a part of gate stack
- Hysteresis increases with HfO_2 thickness

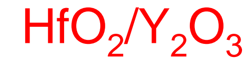
S. Oktyabrsky, V. Tokranov, M. Yakimov, R. Moore, S. Koveshnikov, W. Tsai, F. Zhu, and J.C. Lee, Materials Sci. Eng. B, **135** 272-276 (2006).

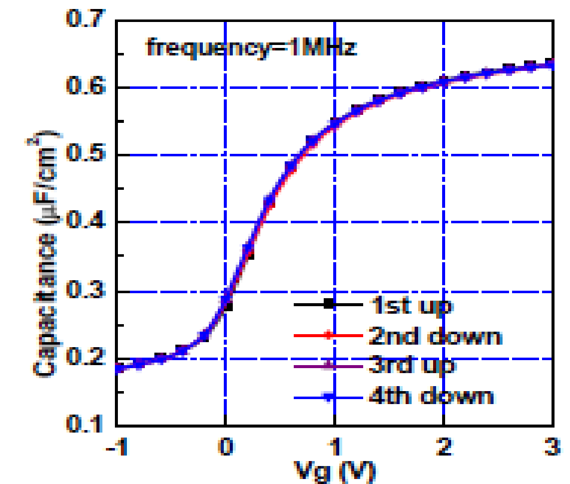
Alternative High-k dielectric to reduce oxide charge

Published: F. Zhu, S. Koveshnikov, I. Ok, H.S. Kim,V. Tokranov, M. Yakimov, S. Oktyabrsky, W. Tsai and J. C. Lee , “Enhancement and Depletion-mode GaAs N-MOSFETs with stacked HfO2/Y2O3 gate dielectric,” Device Research Conference, 83 (2006)









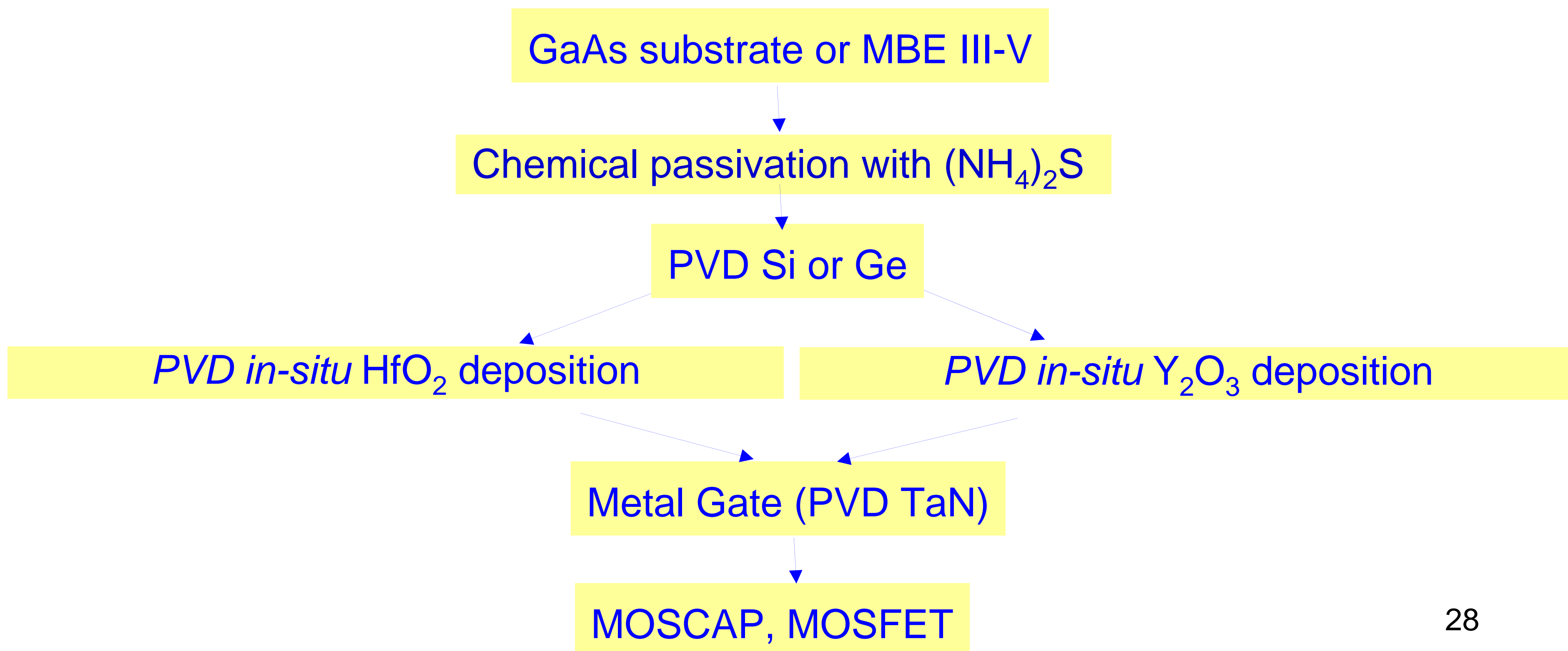
- Reduced hysteresis for Y2O3 based High-k
- Negligible hysteresis suppressed charge trapping occurring in HfO_2/Y_2O_3 high-κ gate stack.

Our approach 2:

2. PVD *ex-situ* passivation with Si, Ge, or Si/Ge (UT):

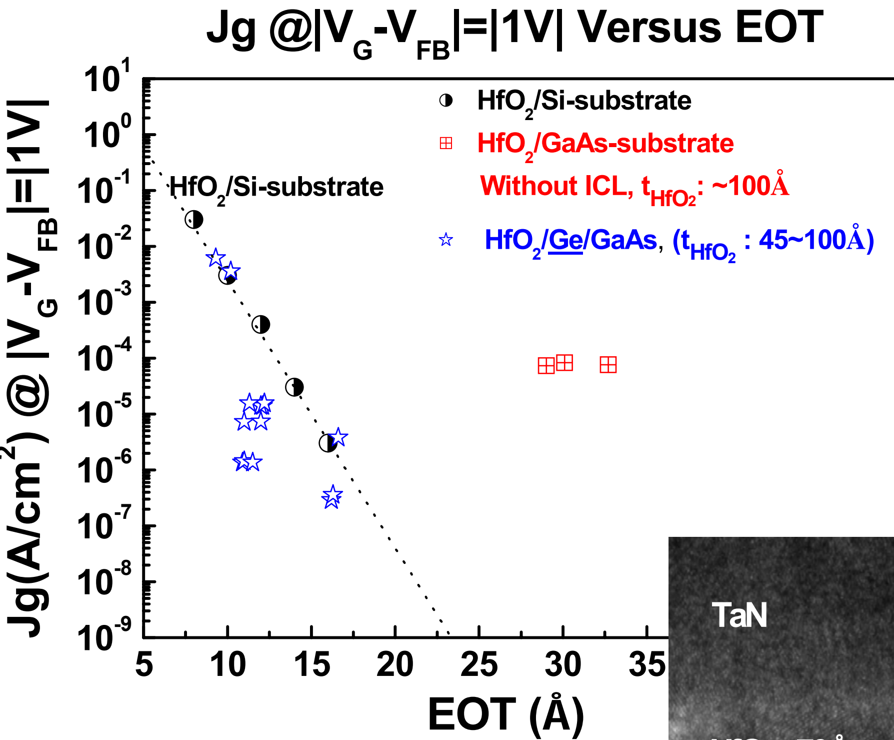
- Chemical passivation of III-V with **$(NH_4)_2S$**
- PVD of Si or Ge at 400°C
- PVD High-k deposition without exposure to air

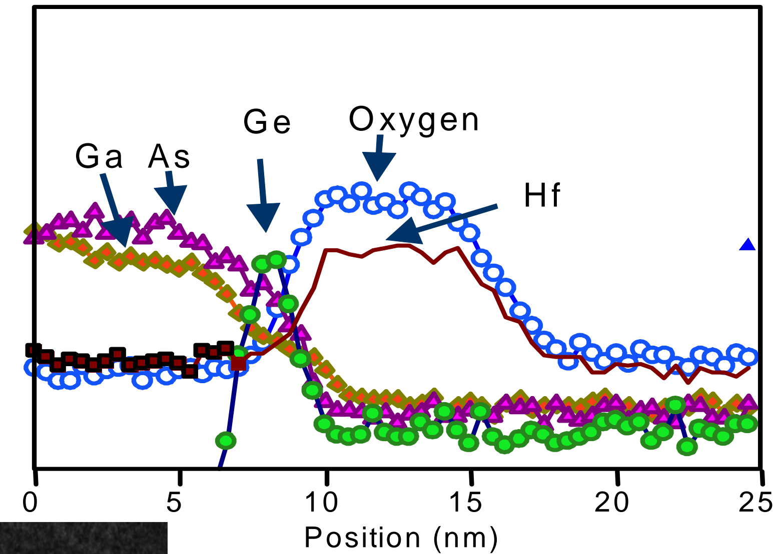
High-k Deposition Options:

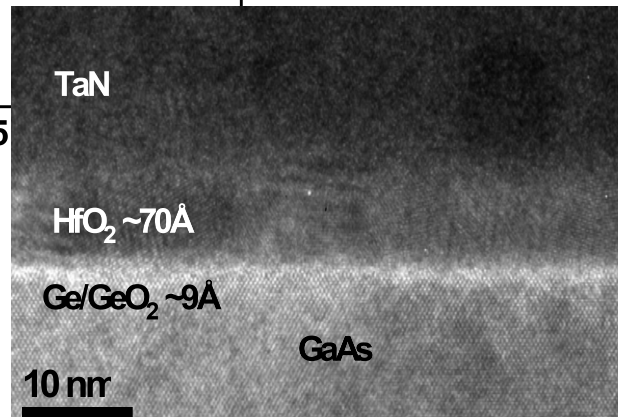


PVD HfO_2 / Si, Ge Passivated GaAs and InGaAs

UT Austin- J. Lee, SUNY- S. Obtyabrsky, Intel-S. Koveshnikov

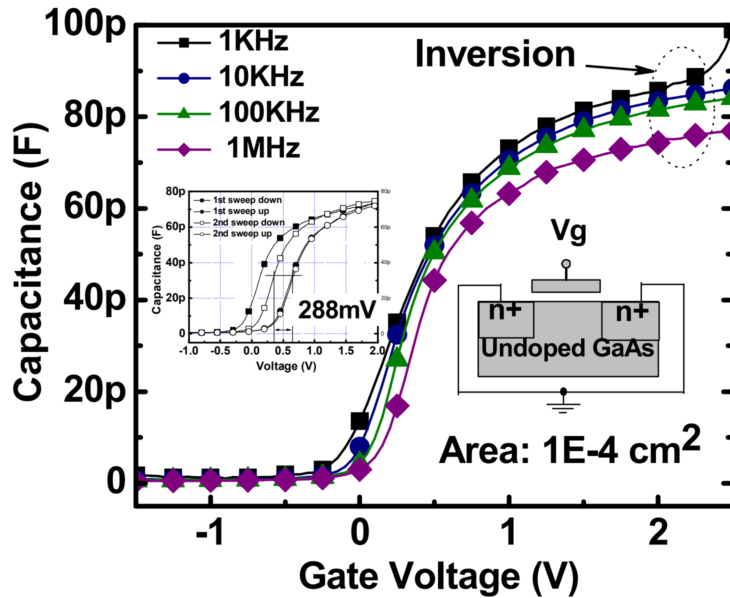


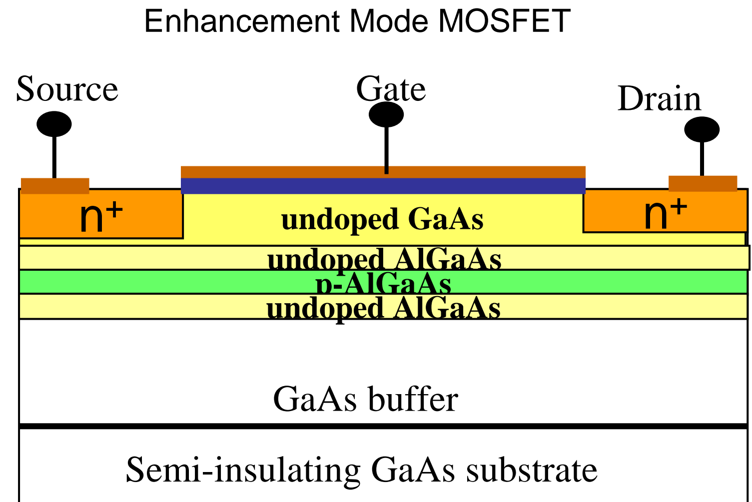


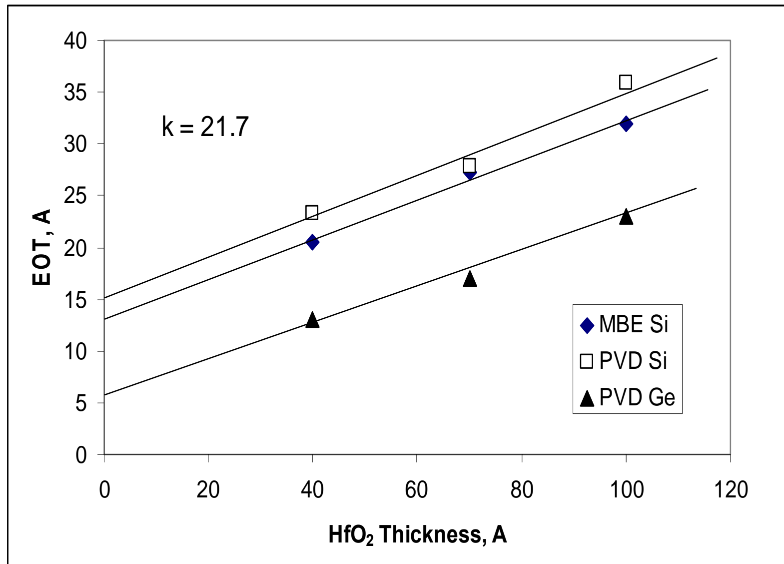


H. Kim, J. Lee etal ,DRC Conference 2006
I. Ok, J. Lee etal., IEDM 2006

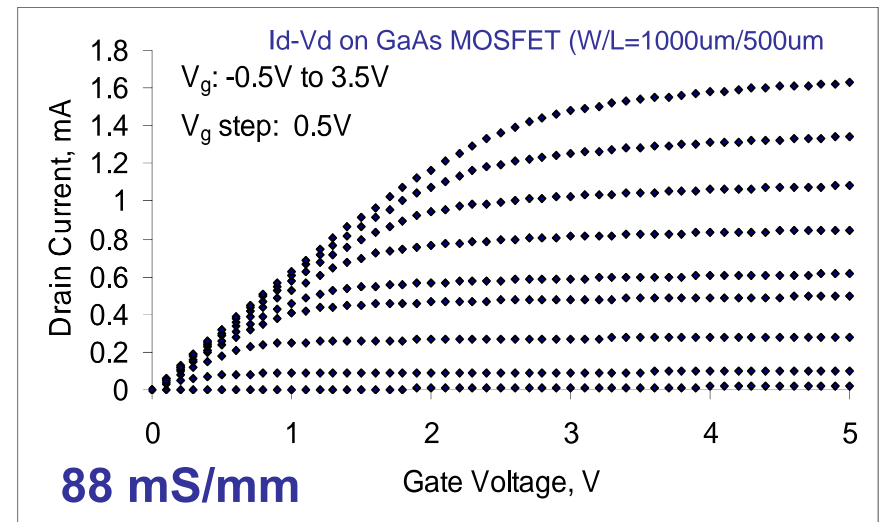
- Various interface layer (a-Si, SiGe, Ge) have been shown to un-pin IIIV surfaces.
- Ge IPL: EOT of ~ 11Å and leakage current ~ 10^{-6} A/cm^2 with 70Å thick HfO_2 layer.
- self aligned inversion n and p HfO2-GaAs MOSFET with low Dit, ~5% frequency dispersion with 900C PMA demonstrated.







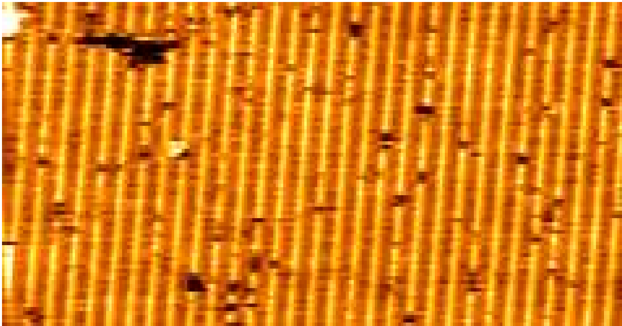
EOT vs HfO2 thickness



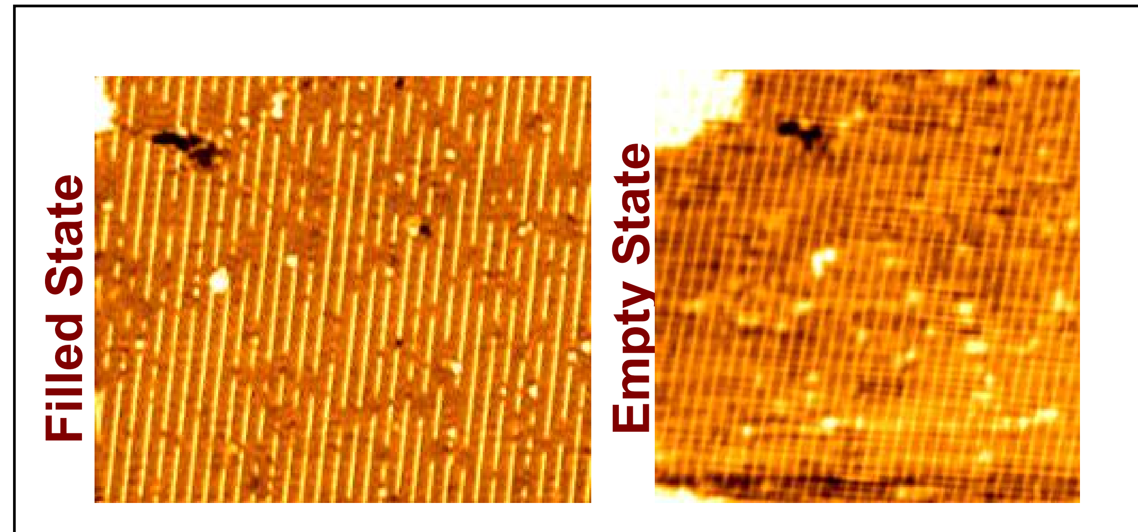
ALD high k on IIIV- Termination/Passivation

UCSD: A. Kummel, Stanford: J. Harris, Intel: N. Goel

Filled State



Cl/InAs(100)-4x2, In-rich reconstruction



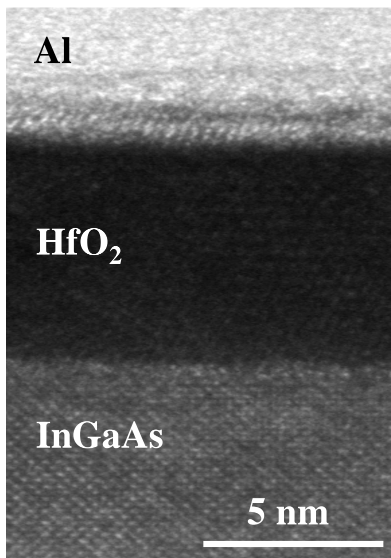
- On InAs(100)-4x2, filled state (DOS) STM shows Cl bonds to the In-In row dimers – dark spot in filled state STM
- Empty state STM shows Cl doesn't etch the InAs(001)-4x2 –empty state STM looks clean
- Cl termination may be beneficial for initiating ALD.

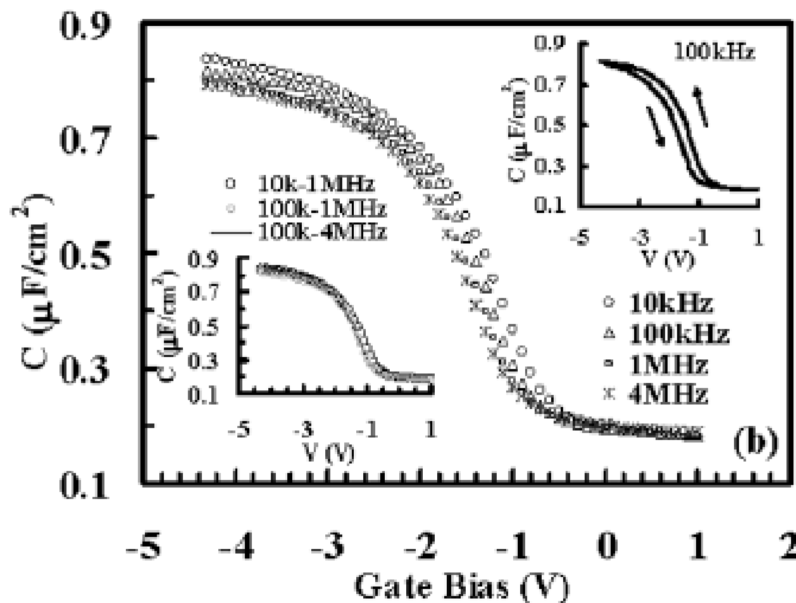
Winn, Shin, Kummel/ UCSD : Cl/InAs(001)-(4x2)

ALD high-κ dielectrics

- ALD dielectric deposition on *exsitu* chemically precleaned III-V surface is attractive and relatively easier to integrate into current production facility
- Low D_{it}, hysteresis and frequency dispersion needed
- ALD dielectrics (eg: Al_2O_3 and HfO_2) integration on III-V samples is feasible with optimized precleaning techniques and conditions like annealing **N. Goel, W. Tsai, et. al. Appl. Phys. Lett. 89, 163517 (2006)**

Un-pinned InGaAs interface with ALD HfO2



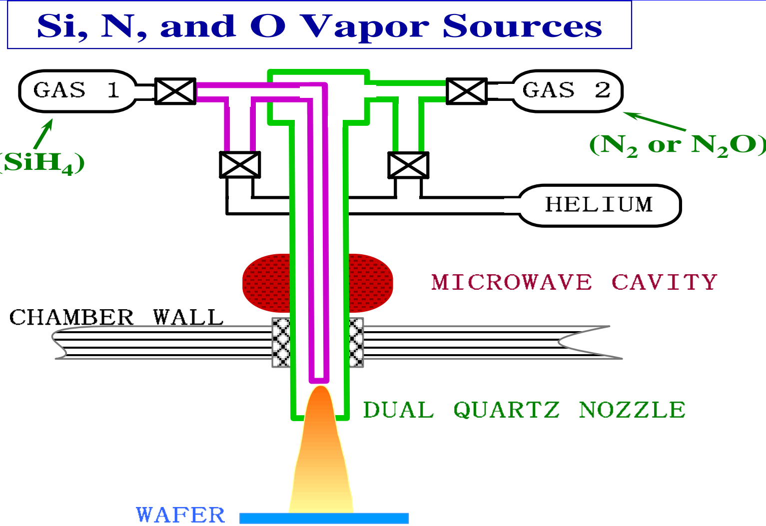


<u>ALD HfO_2 on wet chemical precleaned InGaAs</u>

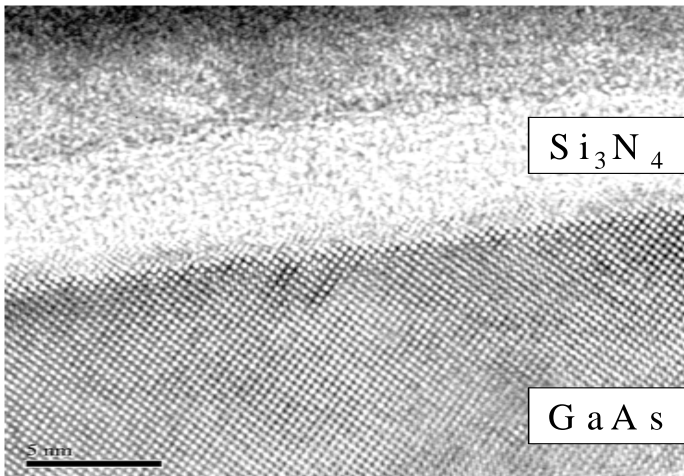
Frequency dispersion
< 3% per decade
Hysteresis
~ 100 mV
Interface state density, D_{it}
~ 8×10^{11} $cm^{-2}eV^{-1}$
(near midgap)

Un-pinnind SiN/GaAs Interface for Enhancement-Mode MISFET

T.P. Ma -Yale , Intel: J. Zheng



MAD (Molecular and Atomic Deposition)



Cross-Section of MAD Si_3N_4 on GaAs

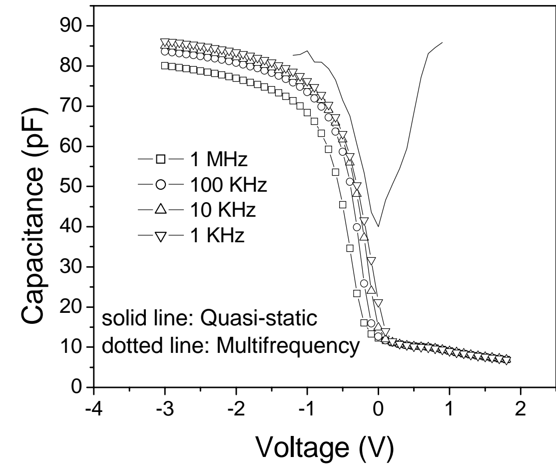


Fig.1 Quasi-static and multi-frequency CV on p type GaAs MIS capacitor; device area: 8.1×10^{-5} cm^2

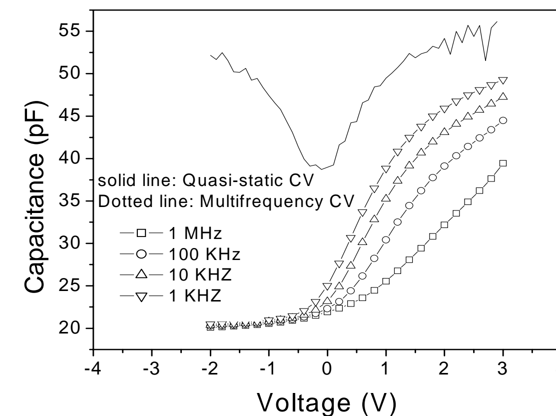
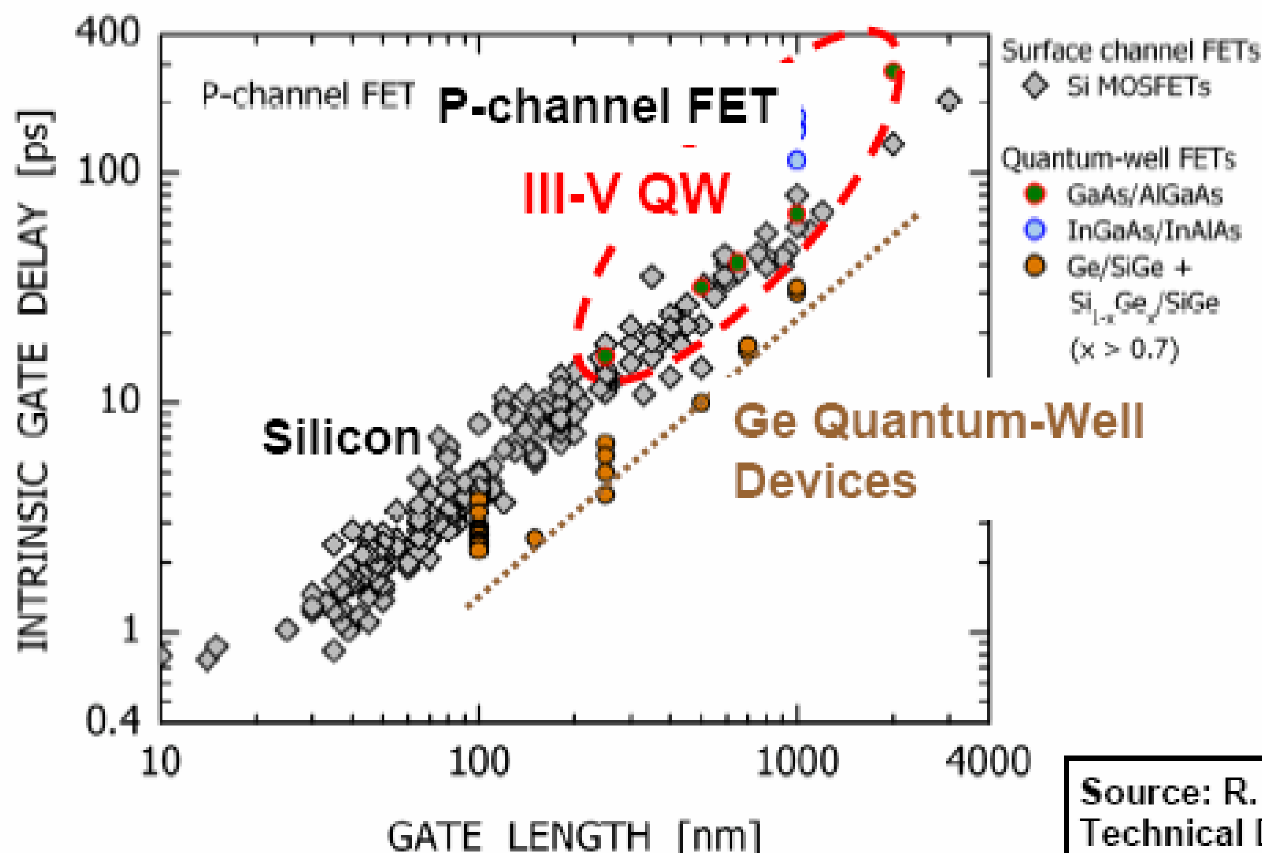


Fig. 2 Quasi-static and multifrequency CV on n type GaAs MIS capacitor, device area: 1.26×10^{-4} cm^2

Weipeng Li, TP. Ma *et al*, SISC 2005

Questions ?

How About Hole Mobility and P-ch FET ?

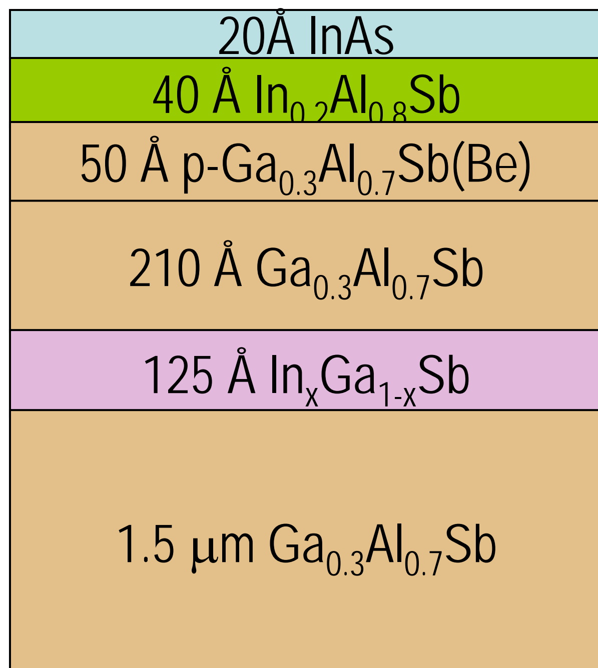


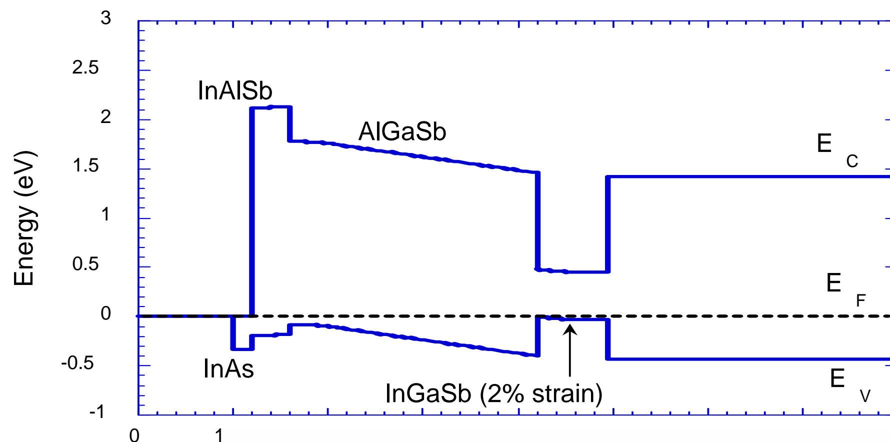
Source: R. Chau, S. Datta, A. Majumdar, Technical Digest, CSICS 2005, pp. 17-20

- III-V materials show hole mobility comparable to Si
- Improve hole mobility in III-V via compressively strained III-V quantum wells and/or other means (???)
- Find the right p-ch FET using other materials for the CMOS (?)

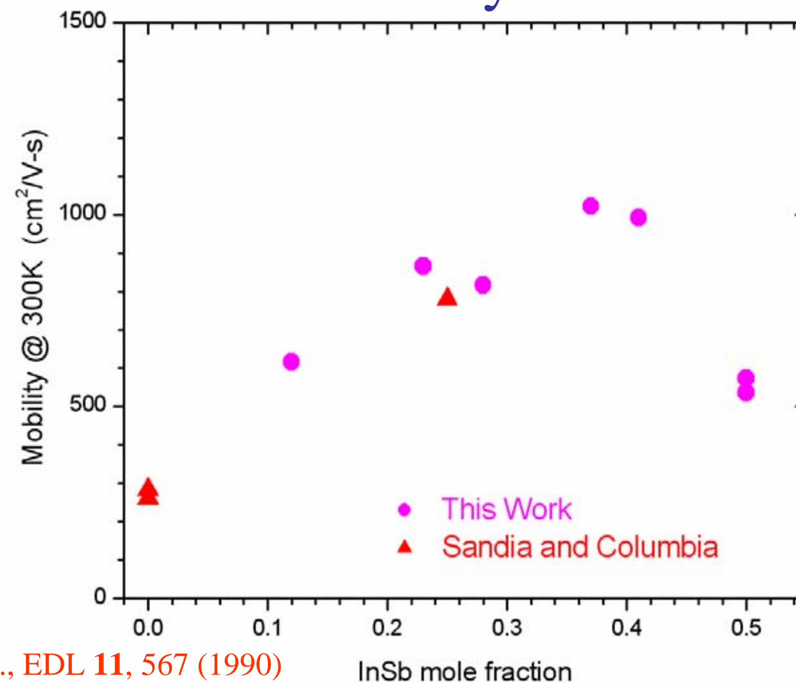
Strained InGaSb quantum wells for IIIV p-FET

NRL-B. Boos, B. Bennett





Quantum Well Mobility at 300 K



Initial p-mobility~1000-1500 cm2/Vs, will need to reduce dislocation density in the channel. (1e12 cm^{-2})

B. Bennett etal., EMC Conference, 2006

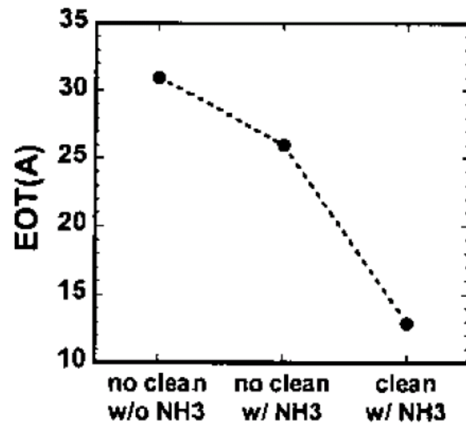
Luo et al., EDL **11**, 567 (1990)
Klem et al., JEM **22**, 315 (1993)

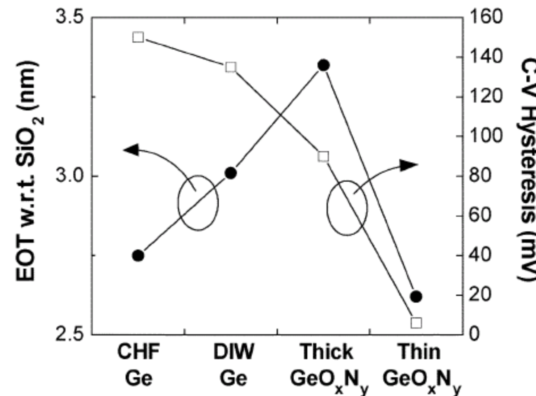
Challenges of Germanium Devices

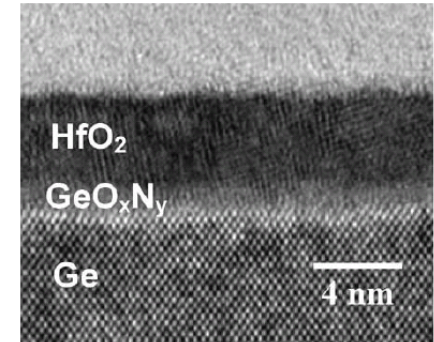
- Substrate/Dielectric Interface Passivation and High-k Compatibility
  - Differences between ALD, PVD, and MBE high-k?
  - Sufficient fundamental understanding on the atomic scale?
- NMOSFET Demonstration
  - Practical or fundamental barrier?
  - Ge PMOS + III-V NMOS?
- Short Channel Device Demonstration
  - Detrimental BTBT in short Lg with low Eg?
  - Hole mobility gain in long Lg repeatable in short Lg?

High-k on Ge Interface Engineering

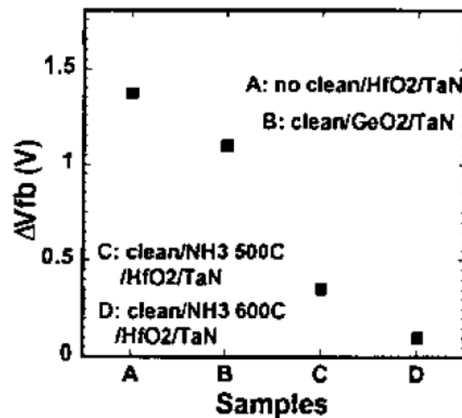
- Proper interface engineering should be exercised to optimize performance (e.g. NH_3, SiH_4, PH_3, AlN etc.)



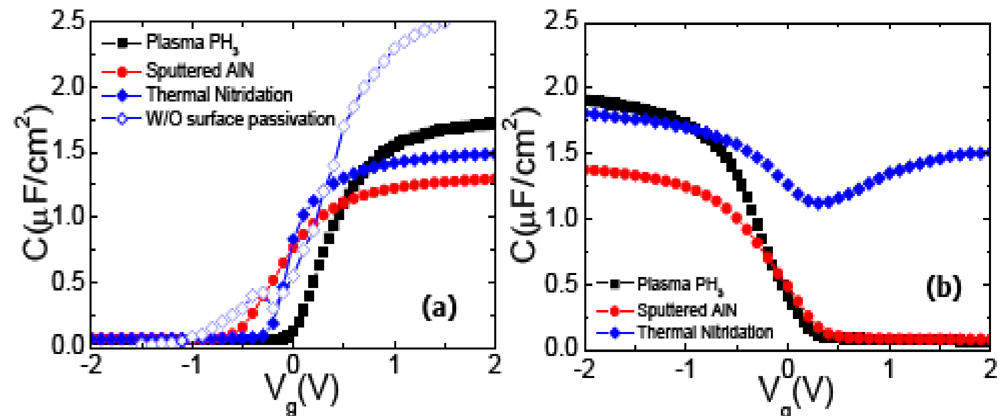




(Chui *et al.*, *IEEE EDL*, **25**, 274 (2004))

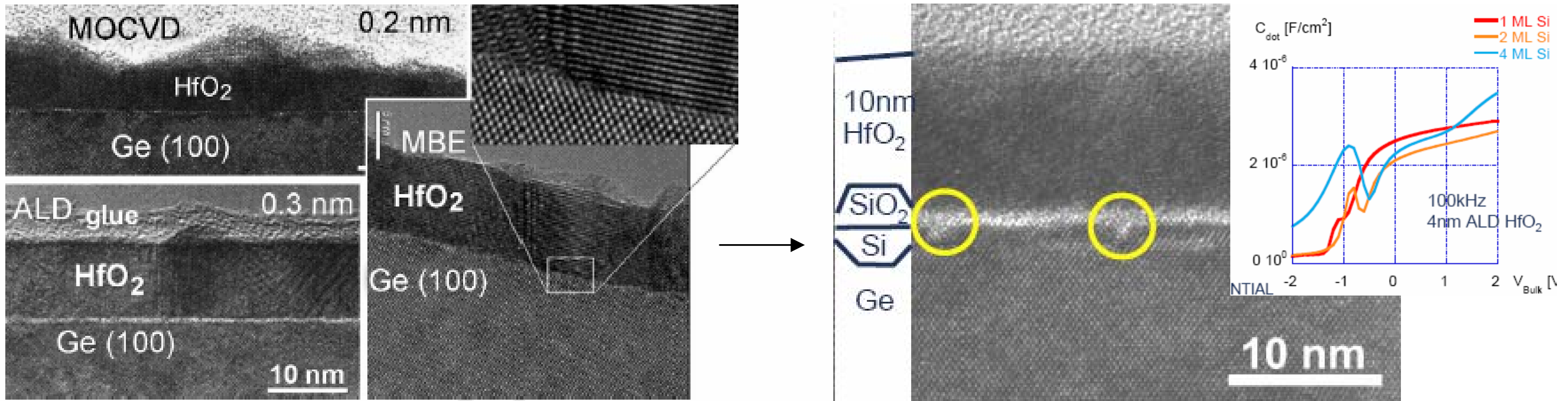


(Bai *et al.*, *VLSI Symp.*, 121 (2003))



(Whang *et al.*, *IEEE IEDM*, 307 (2004))

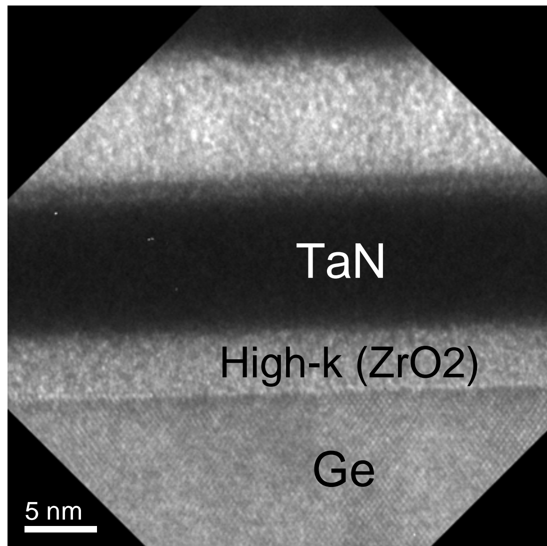
M. Caymax et al. / Materials Science and Engineering B xxx (2006) xxx–xxx



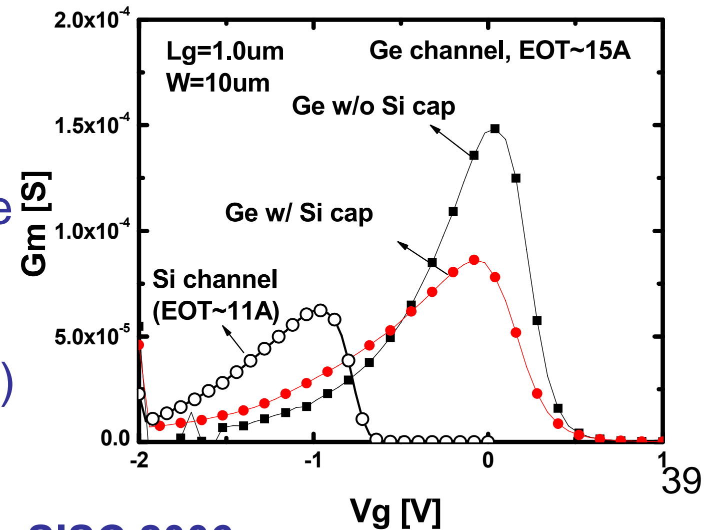
ig. 4. x-TEM images of HfO_2 layers on Ge, deposited by MOCVD, ALD and MBD. The interfacial layer thickness is also indicated.

M. Caymax etal, e-MRS, 06

- Si passivation → major improvement



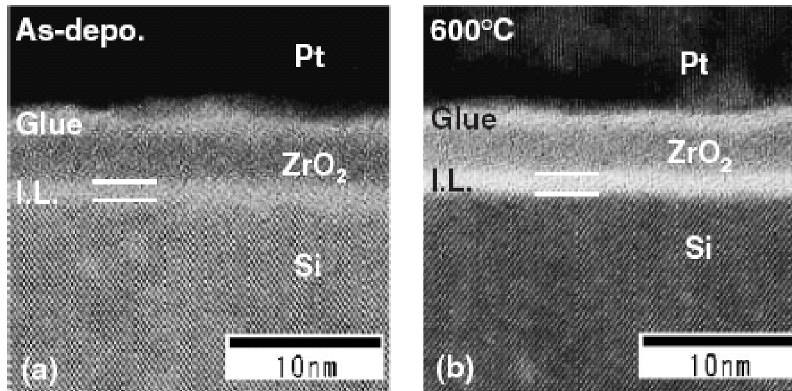
Excellent interface control w/o alternate passivation (NH3)

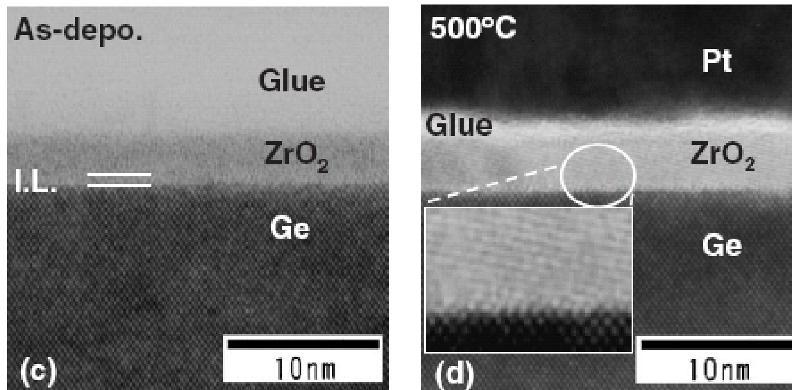


J. Oh, P. Majhi etal., SISC 2006

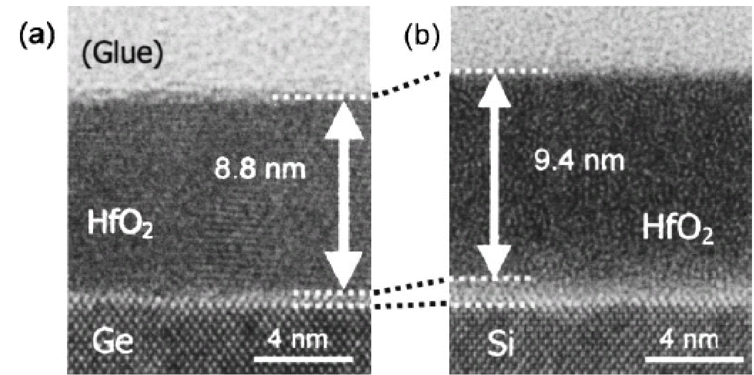
Better EOT Scalability vs. High-k on Si

- Thinner interfacial layer achievable with the same high-k gate stacks on Ge

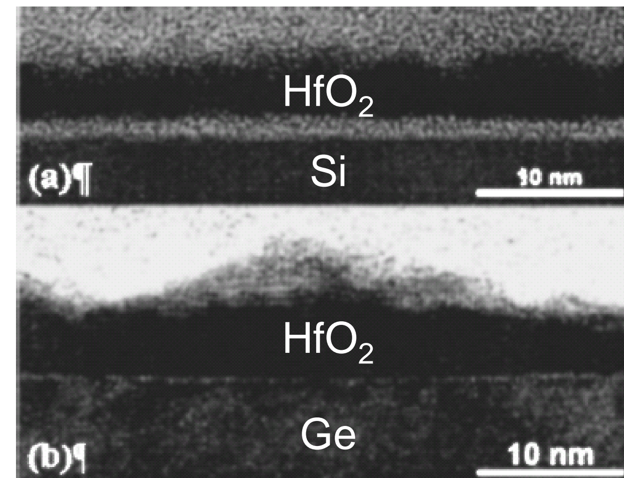




(Yamata *et al.*, *JJAP*, 44, 2323 (2005))



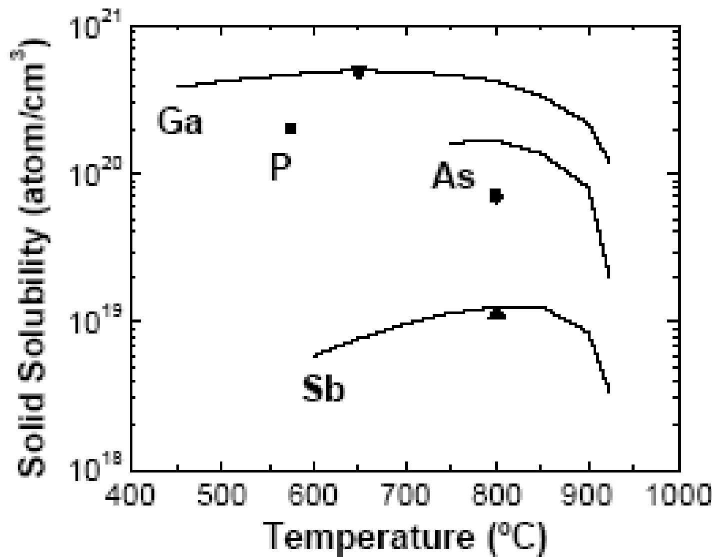
(Kita *et al.*, *APL*, **85**, 52 (2004))

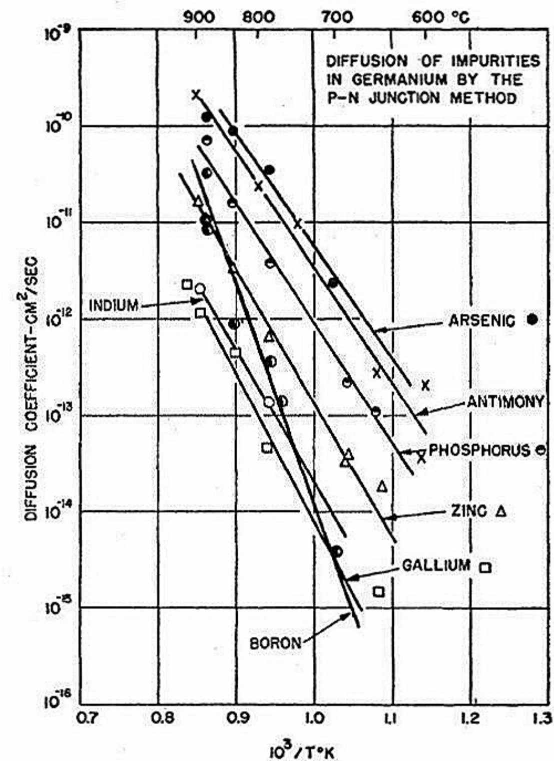


(Van Elshocht *et al.*, *APL*, **85**, 52 (2004))

Facts About *N*-type Dopants in Ge

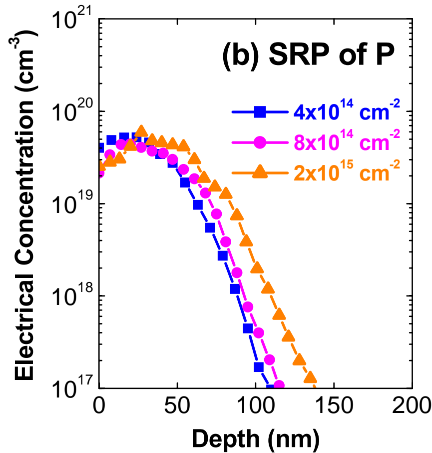
- Lower solid solubility for *n*-type dopants in Ge than in Si
  - P (~ 2×10^{20} cm^{-3}), As (~ 1×10^{20} cm^{-3}), and Sb (~ 1×10^{19} cm^{-3})
- Higher dopant diffusivities in Ge than in Si
  - *P*-dopant diffuses much slower than *n*-type dopants, opposite trends vs. Si

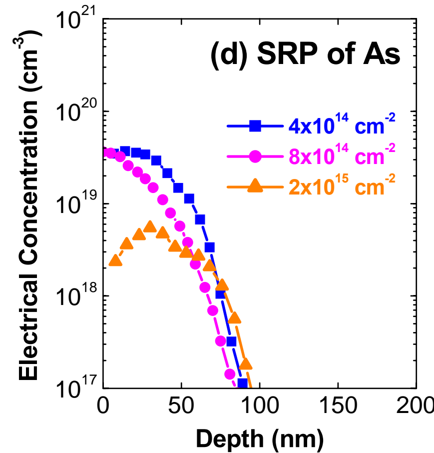


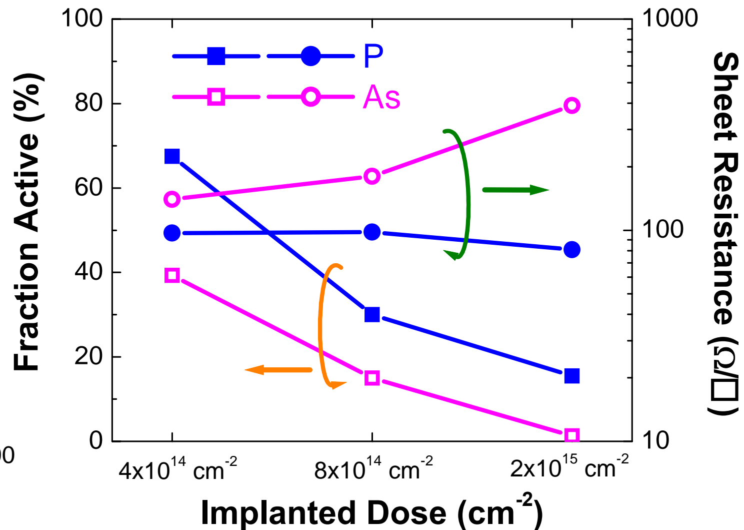


(Dunlap, *Phys. Rev.*, **94,** 1531 (1954))

Fundamental Issues of Ge N-MOSFETs







Key results: Poor Ge n-FET results explained: (i) poor n-dopant activation due to solid-solubility limit, and (ii) S/D junction over-dosage

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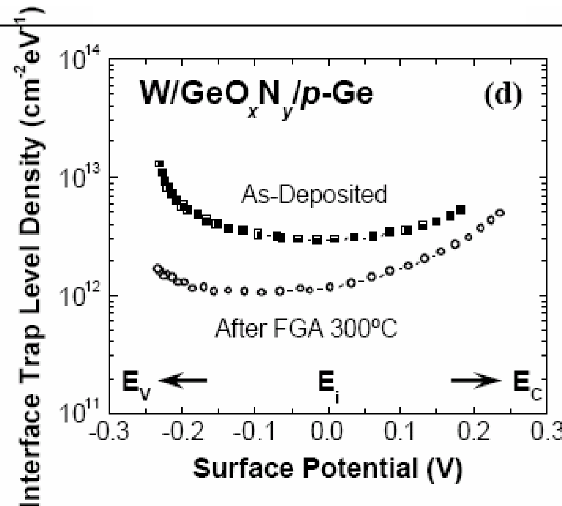
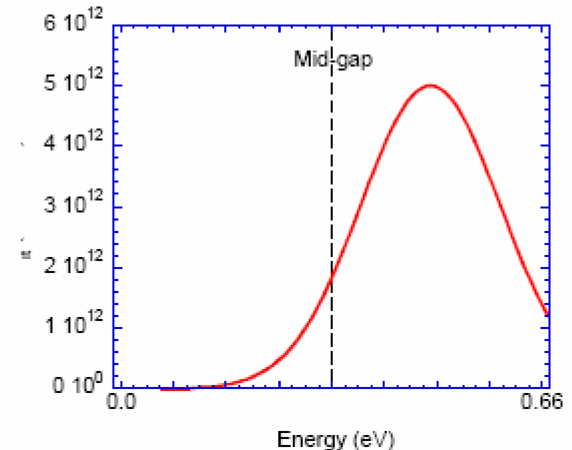
Key results: Higher D_{it} near the conduction band edge for different dielectrics

Recommendation:

Consider buried-channel structures





Stanford – K. Saraswat IMEC – M. Houssa Intel – C. O. Chui/W. Tsai

Ge NFET: Progress and Understanding

Drive-Current Enhancement in Ge n-Channel MOSFET Using Laser Annealing for Source/Drain Activation

Qingchun Zhang, Jidong Huang, Nan Wu, Guoxin Chen, Minghui Hong, L. K. Bera, and Chunxiang Zhu, *Member, IEEE*

- Performance enhancement from novel anneal method

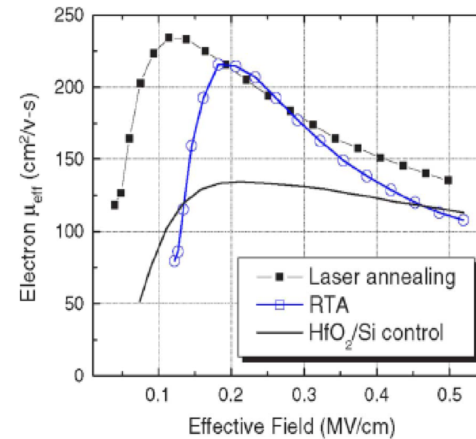


Fig. 5. Extracted electron mobility as a function of the effective electrical field for Ge nMOSFETs with LA and RTA S/D activation as well as a HfO_2/Si control device.

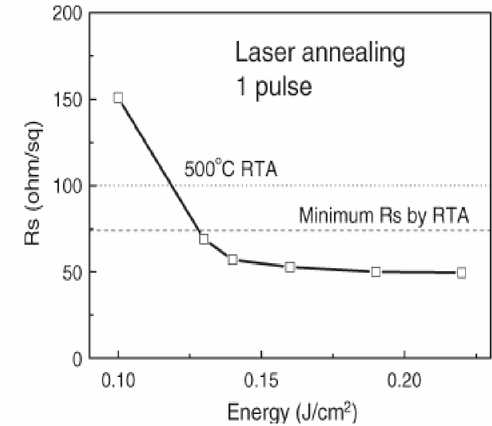


Fig. 1. Sheet resistance (Rs) variation after LA with different laser energies.

The Electrical Properties of HfO_2 Dielectric on Germanium and the Substrate Doping Effect

Weiping Bai, Nan Lu, Andrew P. Ritenour, *Member, IEEE*, Minjoo Larry Lee, Dimitri A. Antoniadis, *Fellow, IEEE*, and Dim-Lee Kwong, *Senior Member, IEEE*

- influence of substrate type (high defects maybe extrinsic, due to interaction)

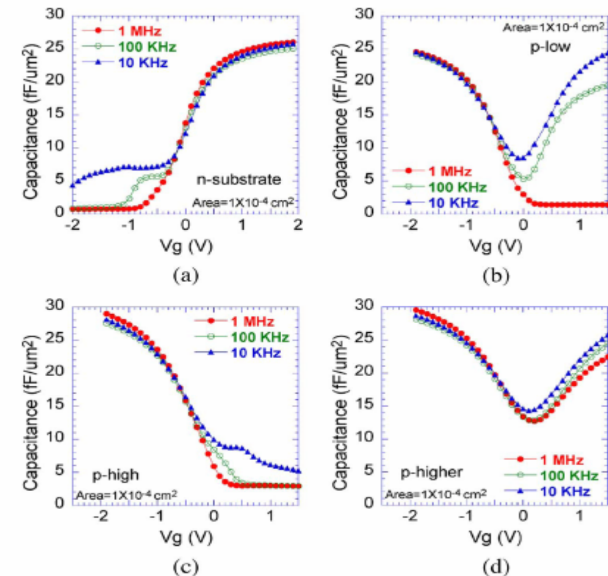
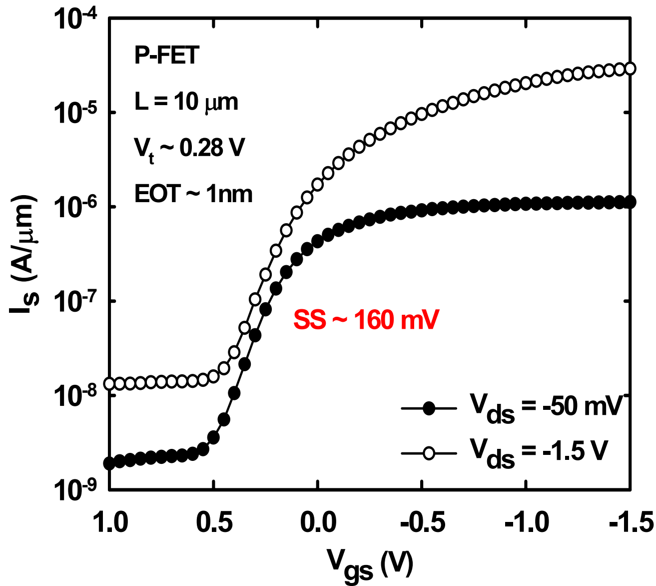


Fig. 10. C–V characteristics at 10 kHz, 100 kHz, and 1 MHz measurement frequencies for the devices on different types of substrates: (a) n-type; (b) low doped p-type; (c) high doped p-type; and (d) higher doped p-type. HfO_2 was deposited by CVD with SN treatment.

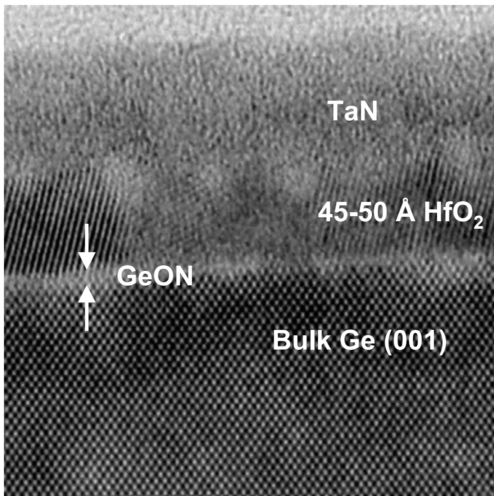
Surface-Channel Ge P-MOSFETs

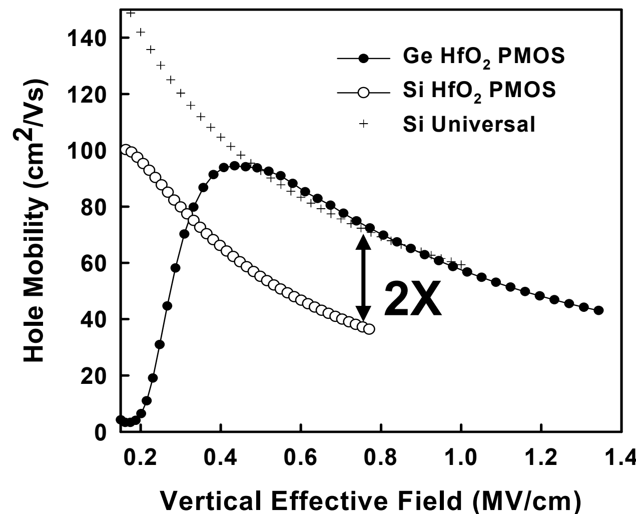
MIT- A. Ritenour, D. Antondias,
NCSR- A. Dimoulas
Intel- R. Lei, W. Tsai



- **Demonstrated EOT ~ 8 Å with QM correction; ~ 2x hole mobility enhancement over HfO_2/Si control**

Issues: ~ 4x expected, possibly due to high D_{it}

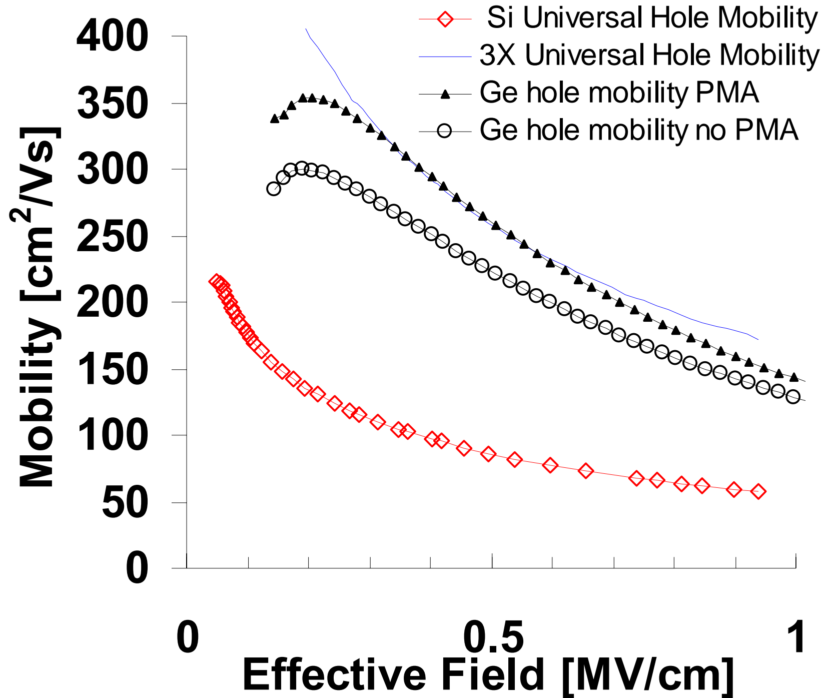




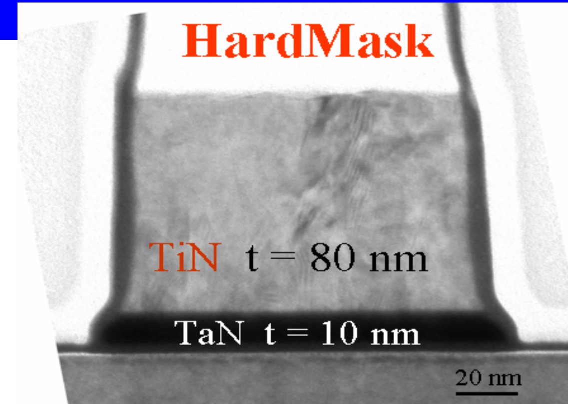
Appl. Phys. Lett. 2006

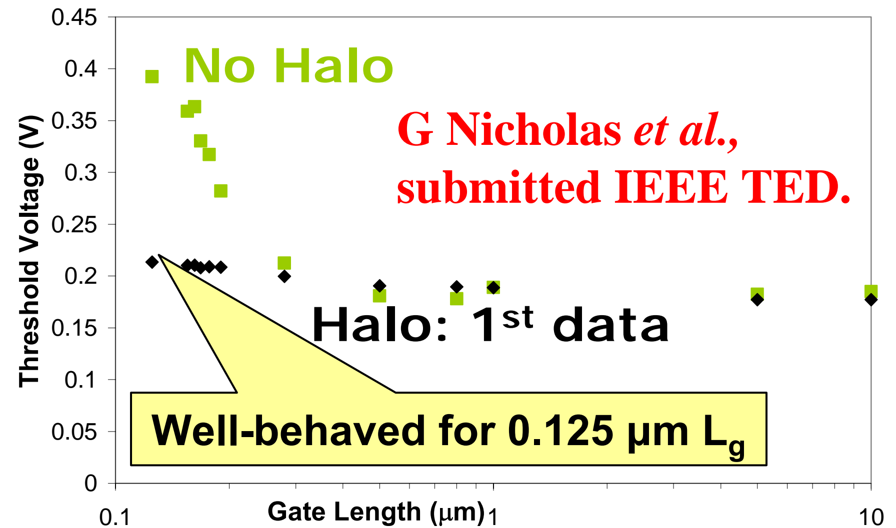
IMEC Ge pMOSFET

IMEC: M Meuris, M Heyns Intel: D Brunco, P Zimmerman



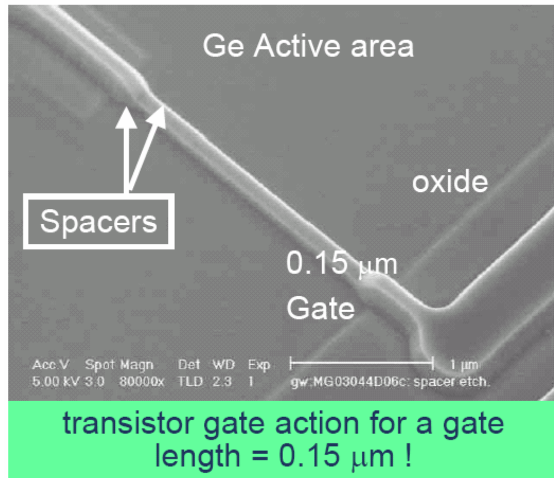
P Zimmerman *et al.*, IEDM 2006



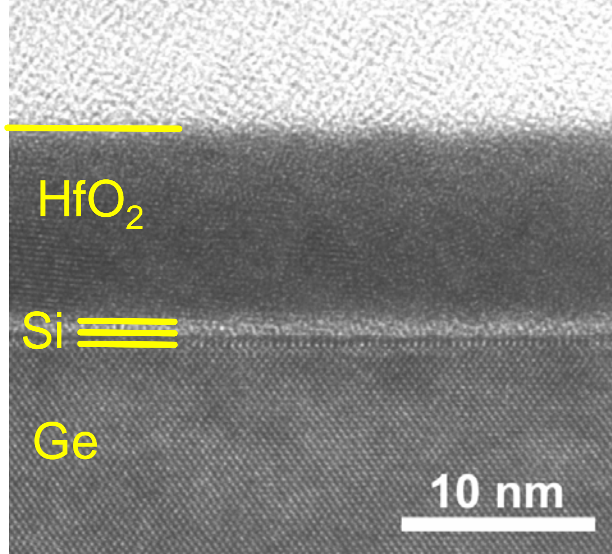


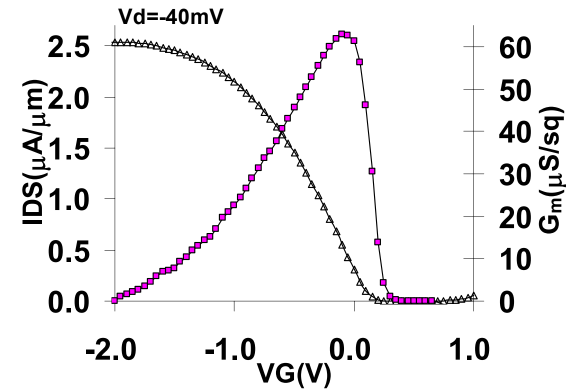
- Ge pMOS mobilities up to 358 cm²/Vs at 12 Å EOT with a gate leakage less than 0.01 A/cm² at V_t + 0.6 V. (6 ML of Epi-Si)
- High performance Ge pMOS transistors with L_g from 10 to 0.125 μm. (future target L_g to 50 nm)

IMEC-M. Heyns,
Intel-D. Brunco, P. Zimmerman

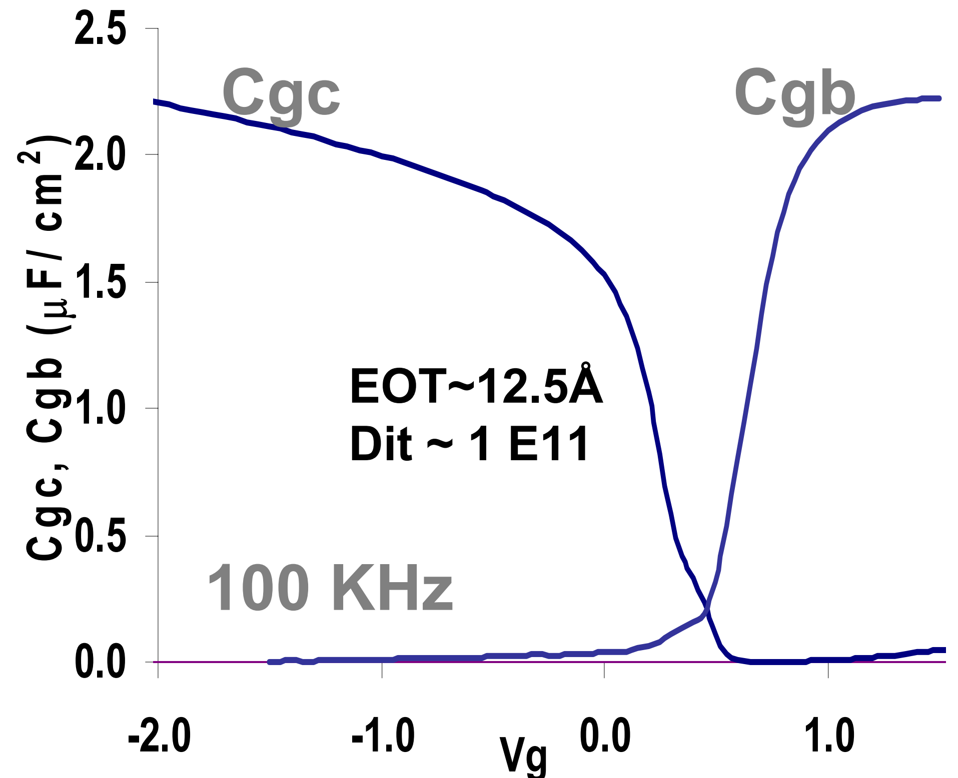


transistor gate action for a gate length = 0.15 μm !



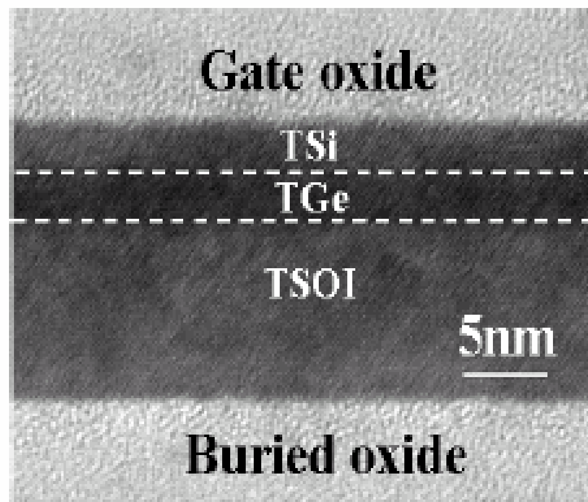


Key results: Sub-micron GOI n- and p-FETs demonstrated; high drive current in p-FET

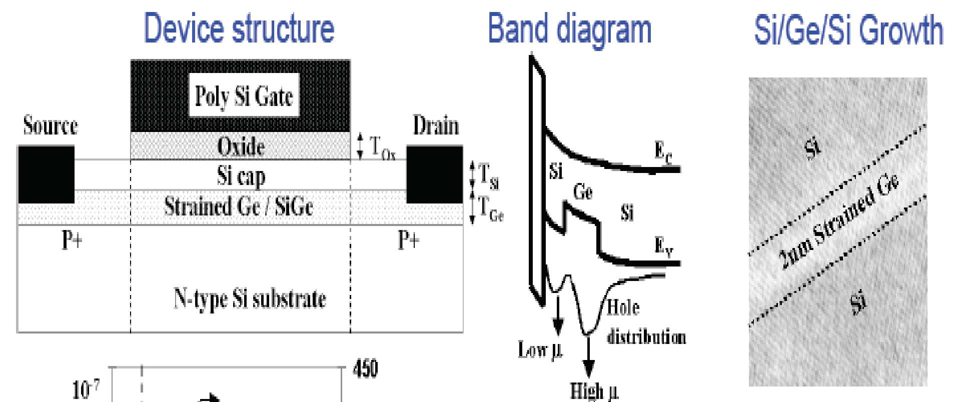


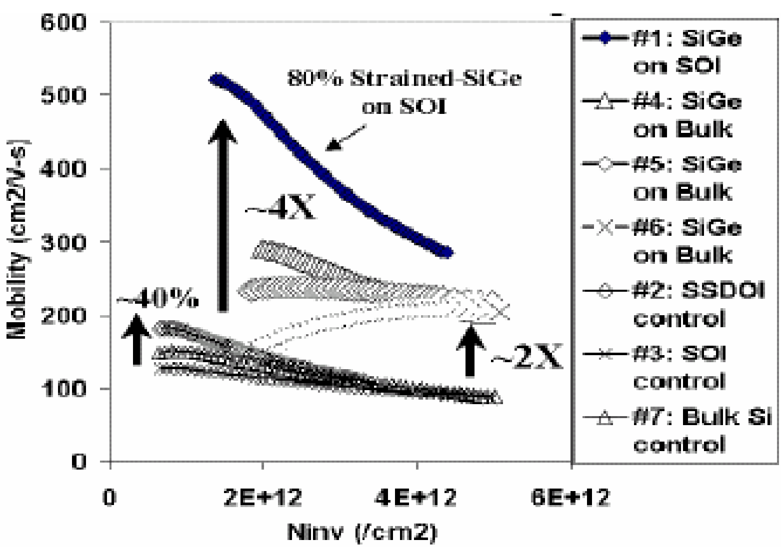
Ge Heterostructure MOSFET to improve transport and electrostatics , Stanford: K. Sarawat

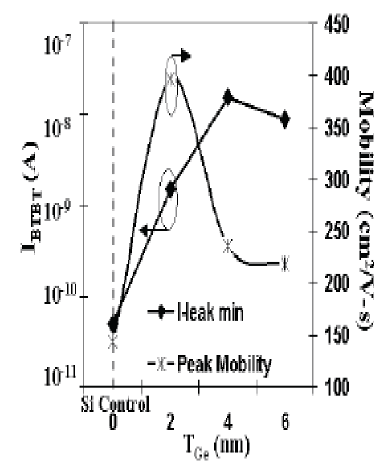
Key results: Strained QW Si/SiGe/Si channel p-FET demonstrated with 4x hole mobility boost



Strained-Ge Bulk PMOS on Relaxed Si







High mobility due to:

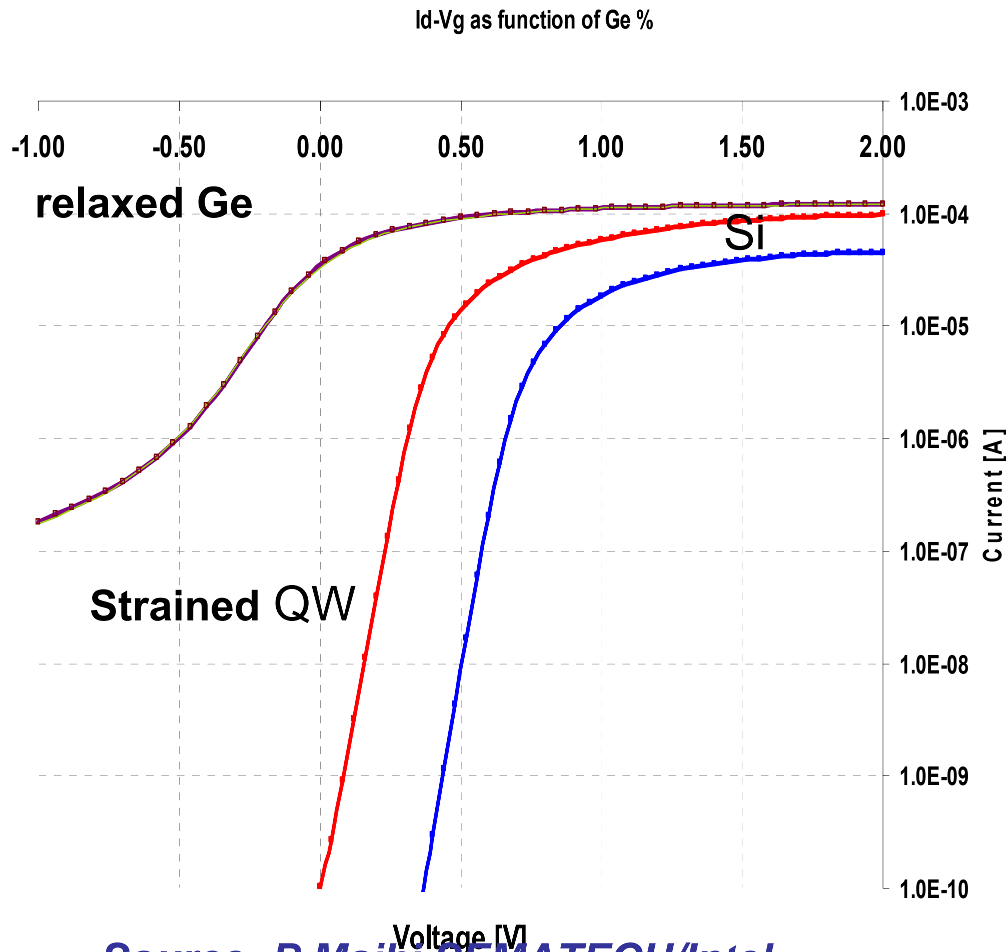
- ✓ Strain in Ge
- ✓ Reduced scattering due to
  - – reduced E-field in Ge
  - – channel being away from the interface

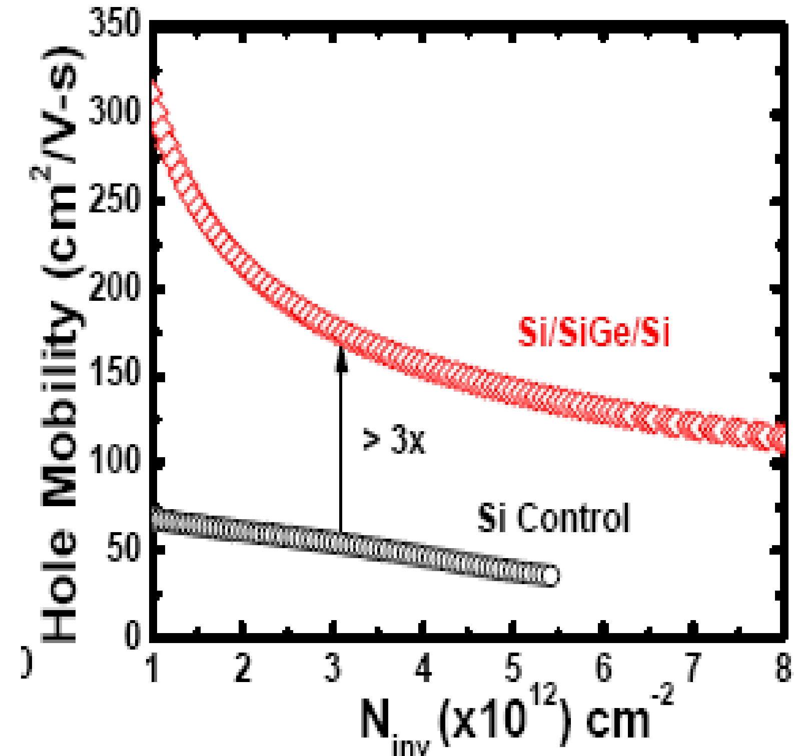
Low S/D leakage due to:

- ✓ Reduced E-field in Ge
- ✓ E_g ⇑ due to confinement of Ge film

Krishnamohan, Krivokapic, Uchida, Nishi and Saraswat, IEEE Symp. on VLSI Tech., June 2005.

SEMATECH Results on Strained Quantum Wells



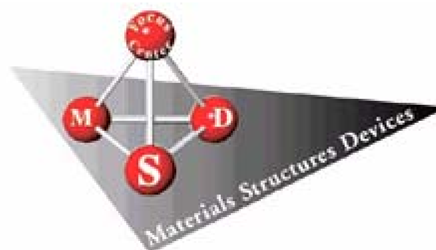


Source: P.Majhi SEMATECH/Intel

- Low Ioff while maintaining high mobility demonstrated in strained QW’s

Summary

• Non-Si channels is critical to CMOS extension and will require a collective efforts within universities , research consortia and device communities to address the various fundamental challenges.



Materials Structures and Devices Focus Center

2006 MSD Focus Center Theme II Kickoff Workshop

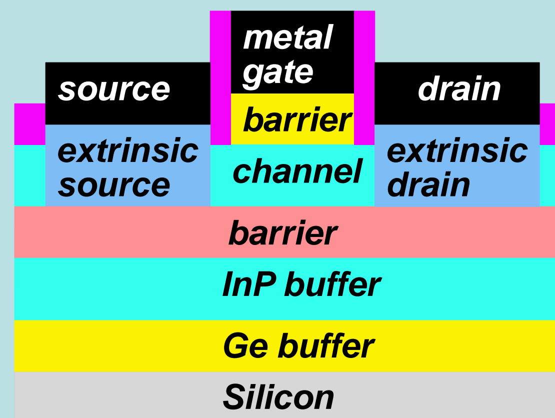
SRC Nonclassical CMOS Research Center

High-K Dielectrics

gate barrier:
permittivity,
surface states,
channel mobility.

Device Design & Modeling

channel:
mobility,
velocity,
density of states,
tunneling,
wavefunction depth,
confinement.



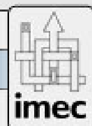
Fabrication: Sub-22 nm MOS Development

contacts:
self-alignment,
resistivity,
reaction depth.

extrinsic S/D:
self-alignment,
resistivity,
activation,
profile.

Materials Integration

substrate: III-V growth on Si



IMEC and RIBER collaborate on Ge and III-V devices for the sub-22nm node

17-05-2006 - Rueil-Malmaison, France - Leuven, Belgium -- Riber, a world-leading supplier of MBE products and services to the compound semiconductor community, joins IMEC's Industrial Affiliation Program (IIAP) on Germanium (Ge) and III-V devices for CMOS beyond the 22nm node. The availability of a unique

• **DARPA's COSMOS Compound Semiconductor on Si**

Accelerating the next technology revolution.