Novel Contact Technology in Metal/Ge Schottky Junction for Metal Source/Drain Ge NMOSFET Application

M. Kobayashi*, A. Kinoshita, K. Saraswat, H. –S. P. Wong and Y. Nishi

Stanford University

ERC Teleseminar July 10th 2008

Outline

- Introduction
  - Ge MOS technology and issues
- Motivations and Objectives
  - Metal/Ge Shottky junction
- Experimental results and discussions
  - Schottky barrier modulation
- Conclusions

Introduction: Ge MOS technology

- Ge channel is one of the promising technology booster beyond 32nm node
  - *High electron/hole mobility* → CMOS integration
  - *Smaller E_g* → Possible voltage scaling
  - *Low melting point* → Low process temperature
  - *Compatible with silicon VLSI technology*

Material→ Property↓	Si	Ge	GaAs	InAlAs	InSb
Electron mobility	1600	3900	9200	40000	77000
Hole mobility	430	1900	400	500	850
Bandgap (eV)	1.12	0.66	1.424	0.36	0.17
Dielectric constant	11.8	16	12.4	14.8	17.7

Introduction: Challenging issues

- **Superior Ge PMOSFETs* are reported, while Ge NMOSFET is not**
  - **Challenging issues for Ge NMOSFET**
    - **Interface property of Ge gate stack**
      - **High Dit near conduction band degrades electron mobility by Coulombic scattering****
    - **Not so high mobility gain without strain**
    - ***Low activation of n-type dopant***
      - ***Increase S/D resistance and junction leakage***
      - ***Shallow junction formation is also challenging***

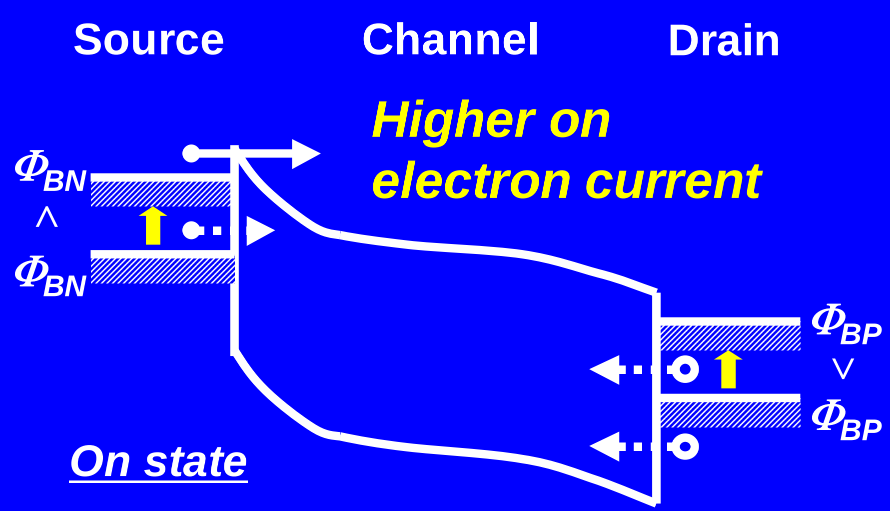
*P. Zimmerman et al., IEDM 2006, T. Yamamoto et al., IEDM 2007

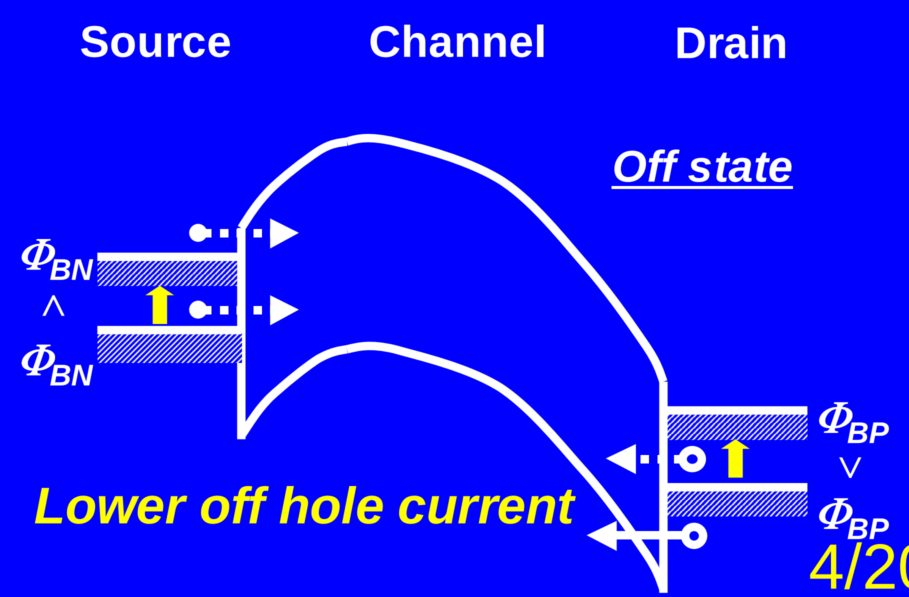
**D. Kuzum et al., IEDM 2007

Motivation

- **Metal S/D can be a key break-through**
  - **Reduce S/D series resistance, shallow junction and possible solution for source-starvation***
  - **Design parameter: Schottky barrier height**
- **However, *Fermi-level pinning* at metal/Ge Schottky junction is a big obstacle**

*M. V. Fischetti et al., IEDM2007





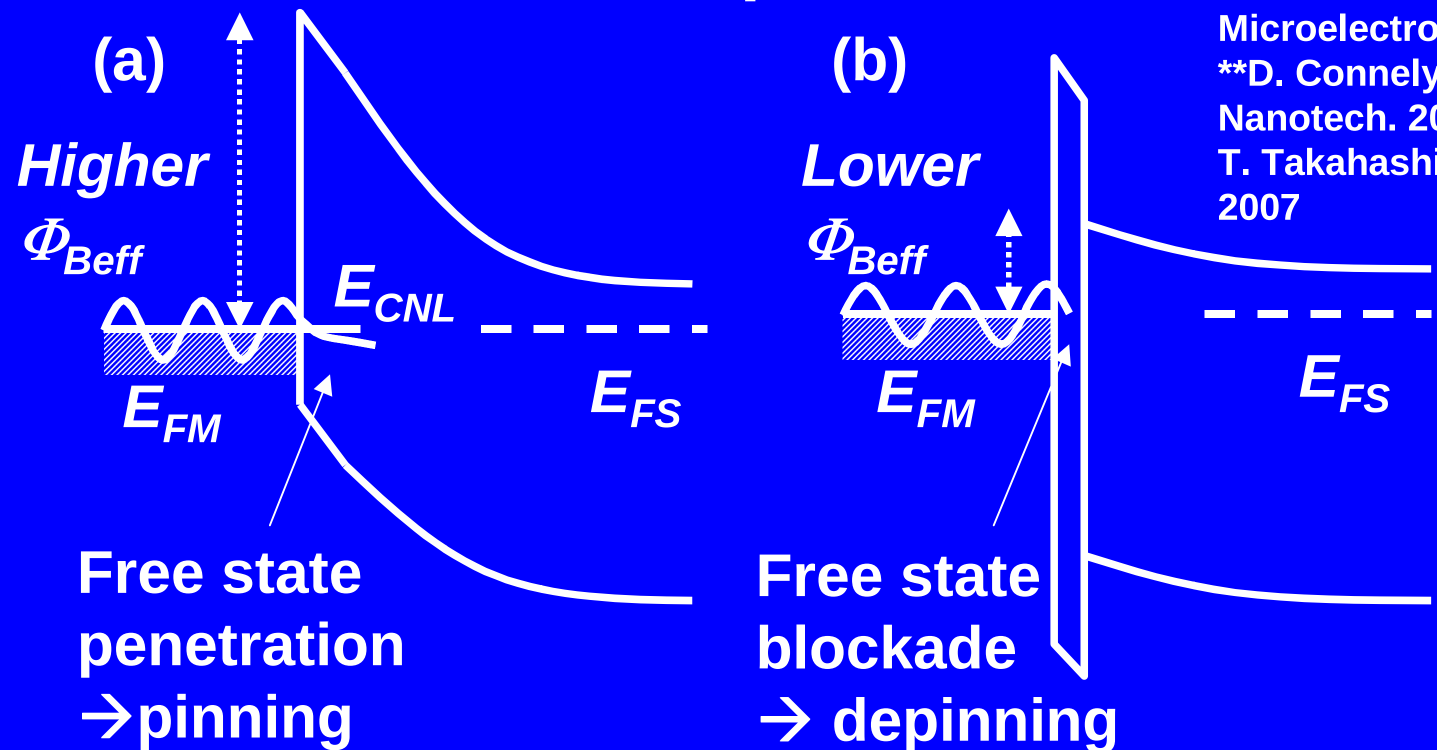
Objectives

- Systematic study on the characteristics of metal/Ge Schottky junction
- Develop the new technique to mitigate Fermi-level pinning by using interfacial layer
- Metal S/D Ge NMOSFET implementation

Fermi-level pinning in metal/Ge Schottky junction

- **Small E_g Ge suffers from high MIGS density**
  - **Pin metal Fermi-level near charge neutrality level***
- **Ultrathin interfacial layer can prevent free electron wavefunction penetration****

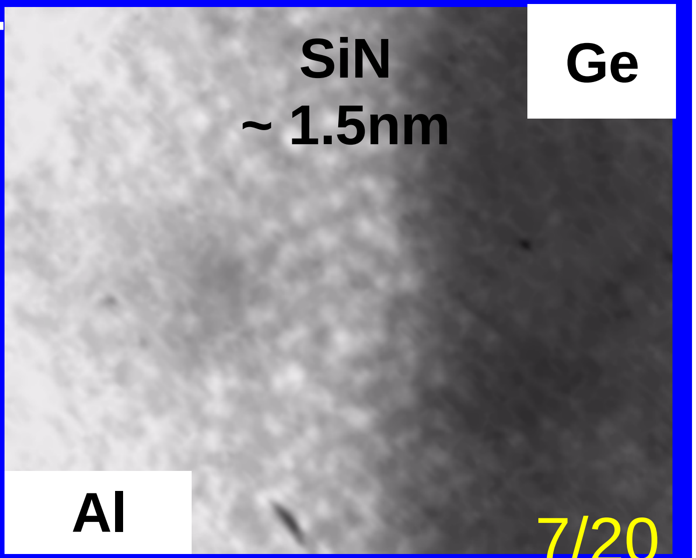
***D. Han et al., Microelectron. Eng., 2005**
****D. Connely et al., IEEE Nanotech. 2004,**
T. Takahashi et al., IEDM 2007



Schottky diode fabrication

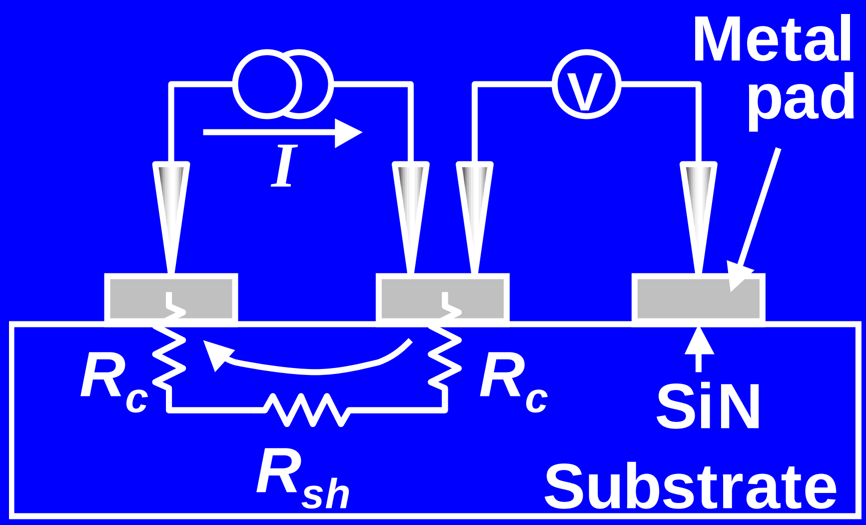
Schottky diode process flow

- Starting wafer: Ge $1x10^{15}cm^{-3}$ doped
- O2 plasma and HF/HCl cyclic clean/passivation
- Sputter SiN deposition
  - In-situ high vacuum annealing in sputter system
    - Depassivation of Cl termination
    - Desorption of GeOx
  - SiN sputter in N ambient
    - Uniform and fully amorphous
- Metal deposition



Measurement

- **Simple I-V measurement**
- **4 terminal measurement**
  - **Use for specific contact resistance**



Schottky barrier height estimation

- **Thermionic emission model with ideality factor**

Schottky barrier height extraction method

$$J = A^* \exp\left(-\frac{\Phi_B^{eff}}{k_B T}\right)\exp\left(\frac{eV}{nk_B T}\right)\left[1-\exp\left(-\frac{eV}{k_B T}\right)\right]$$

Transform ↓

$$\ln\frac{J}{1-\exp\left(-\frac{eV}{k_B T}\right)} = \ln\left(A^* T^2 \exp\left(-\frac{\Phi_B^{eff}}{k_B T}\right)\right) + \frac{eV}{nk_B T}$$

→ **Obtain *n* from slope**

Take J intercept as B ↓

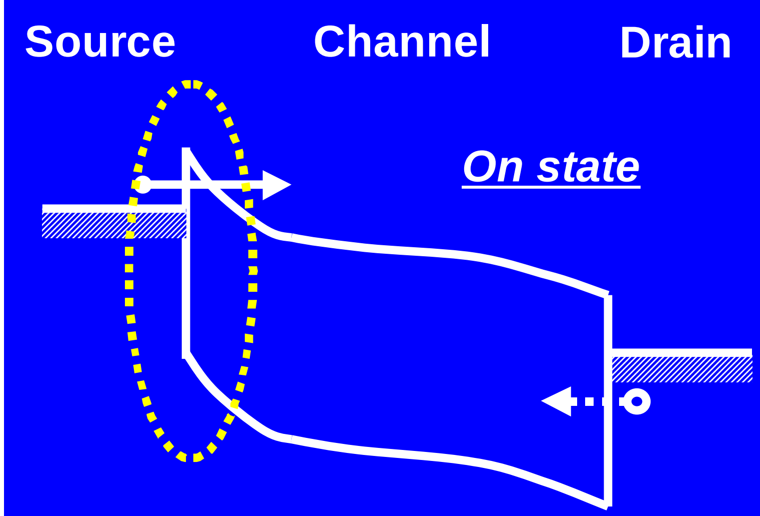
$$B - \ln T^2 = \frac{\Phi_B^{eff}}{k_B T} + \ln A^*$$

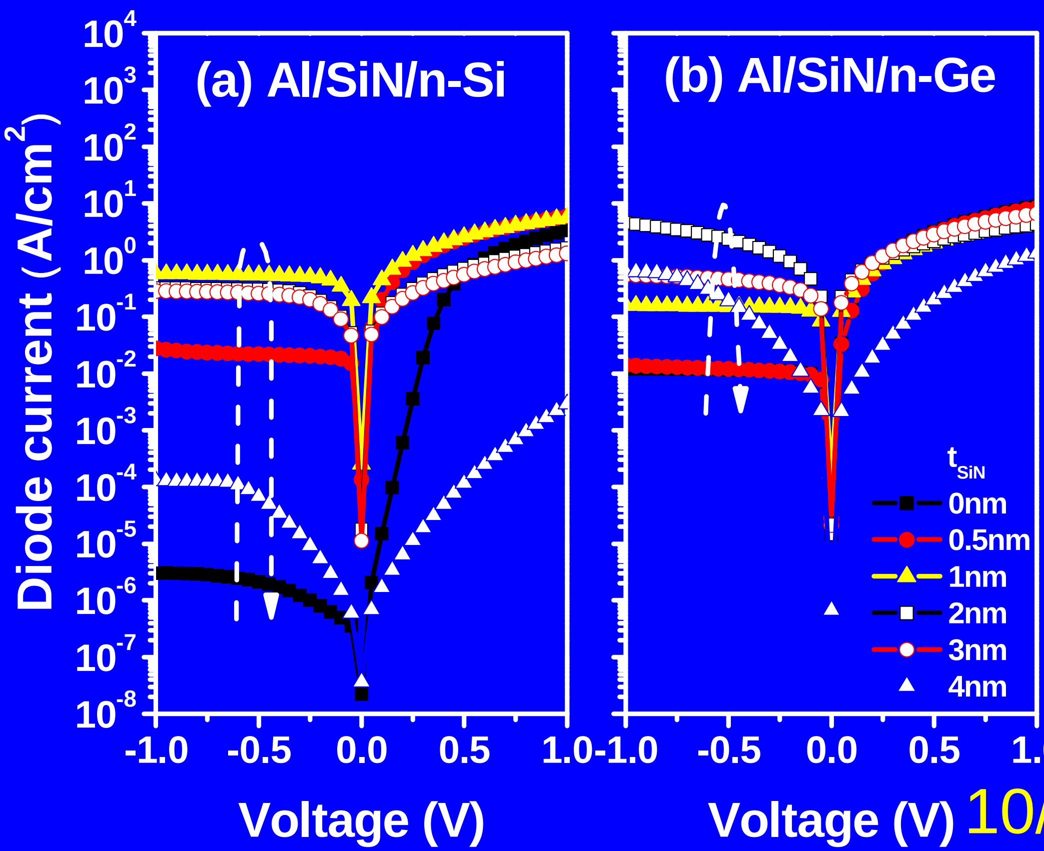
Arrhenius plot ↓

$$\underline{\Phi_B^{eff}}$$

Al/SiN/n-Ge Schottky diode (1)

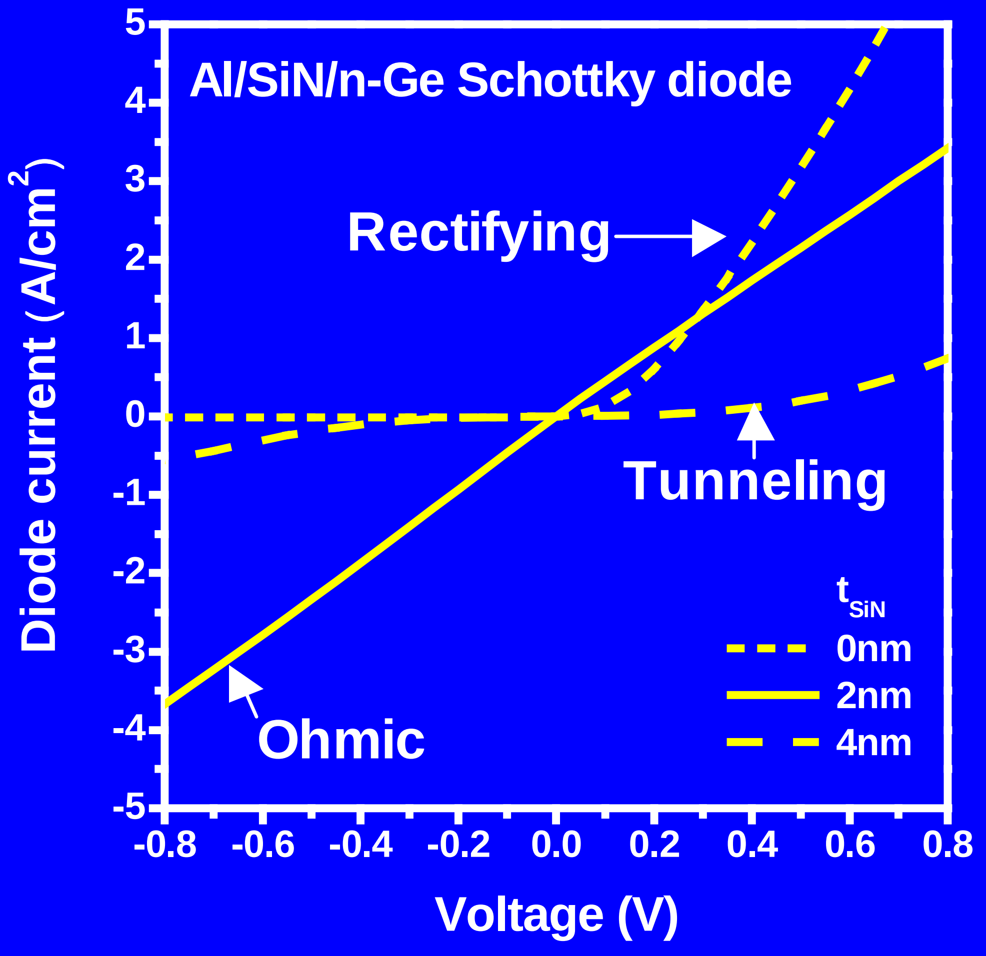
- **Junction between S/D and n-inv. channel**
- **Reverse bias diode current has maximum**
  - **Due to Φ_{BNeff} lowering**





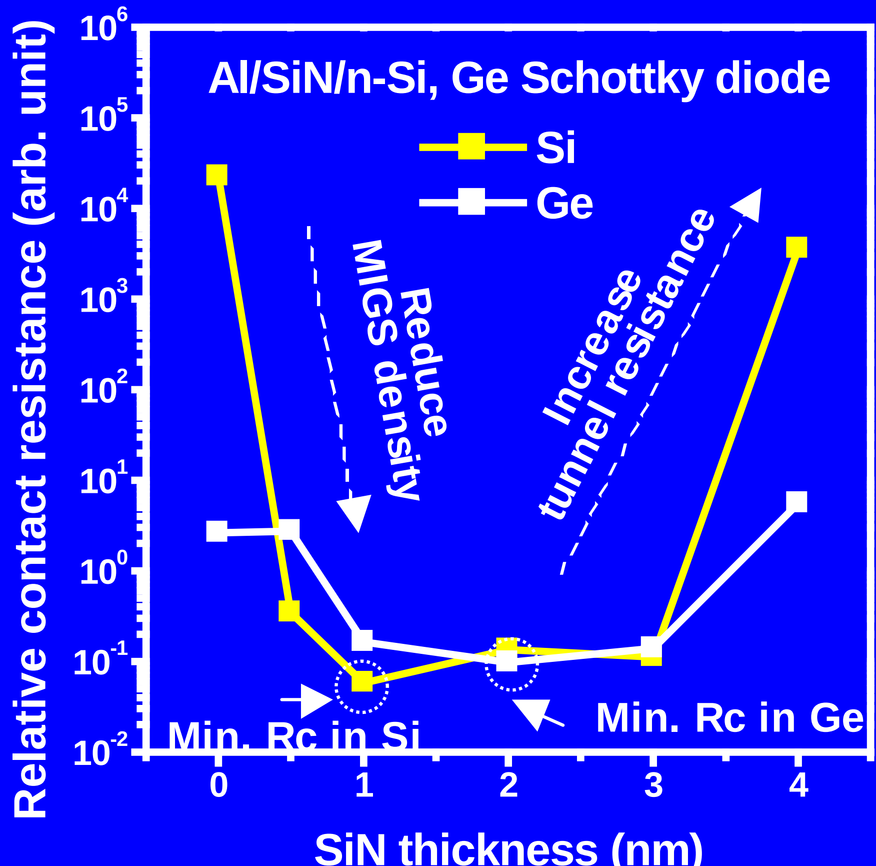
Al/SiN/n-Ge Schottky diode (2)

- **Transport mechanism changes from rectifying, ohmic and to symmetric tunneling**



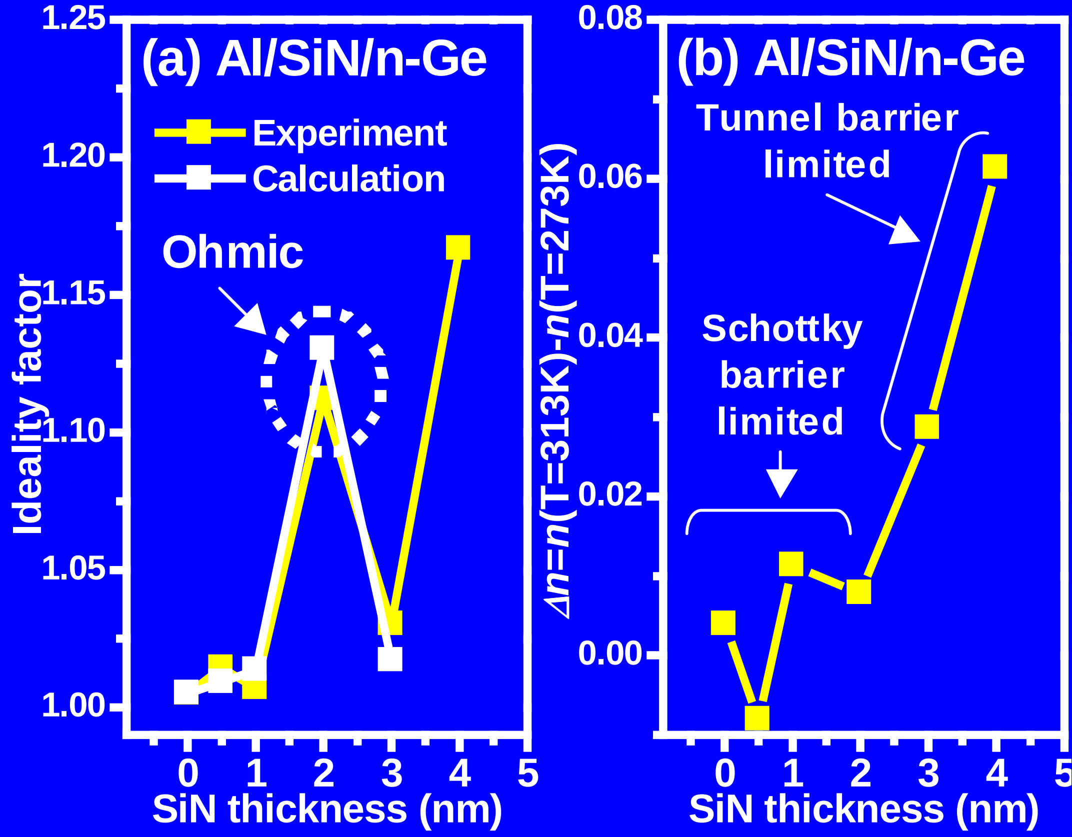
Al/SiN/n-Ge Schottky diode (3)

- **Contact resistance has minimum**
  - **Two mechanisms are competing**
    - **MIGS density reduction and tunnel resistance**



Al/SiN/n-Ge Schottky diode (4)

- **Ideality factor is largely deviated from ideal 1.01 at minimum Rc**
  - **Analytical calculation result agrees with experiment**
  - **Transport mechanism is dominated by ohmic**



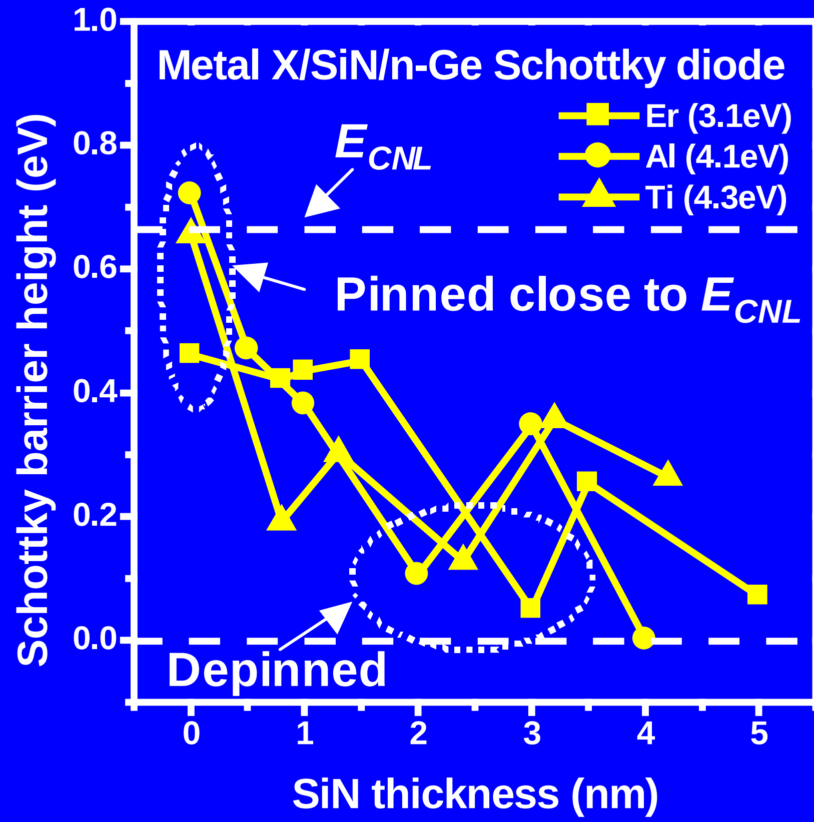
$$n_{if} = \left(1 - \frac{\delta\Phi_{BN}^{eff}}{4\left|V_i^0\right|}\right)^{-1}$$

$\delta\Phi_{BN}^{eff}$: Zero bias Φ_{BN} lowering

V_i^0: Zero bias band bending

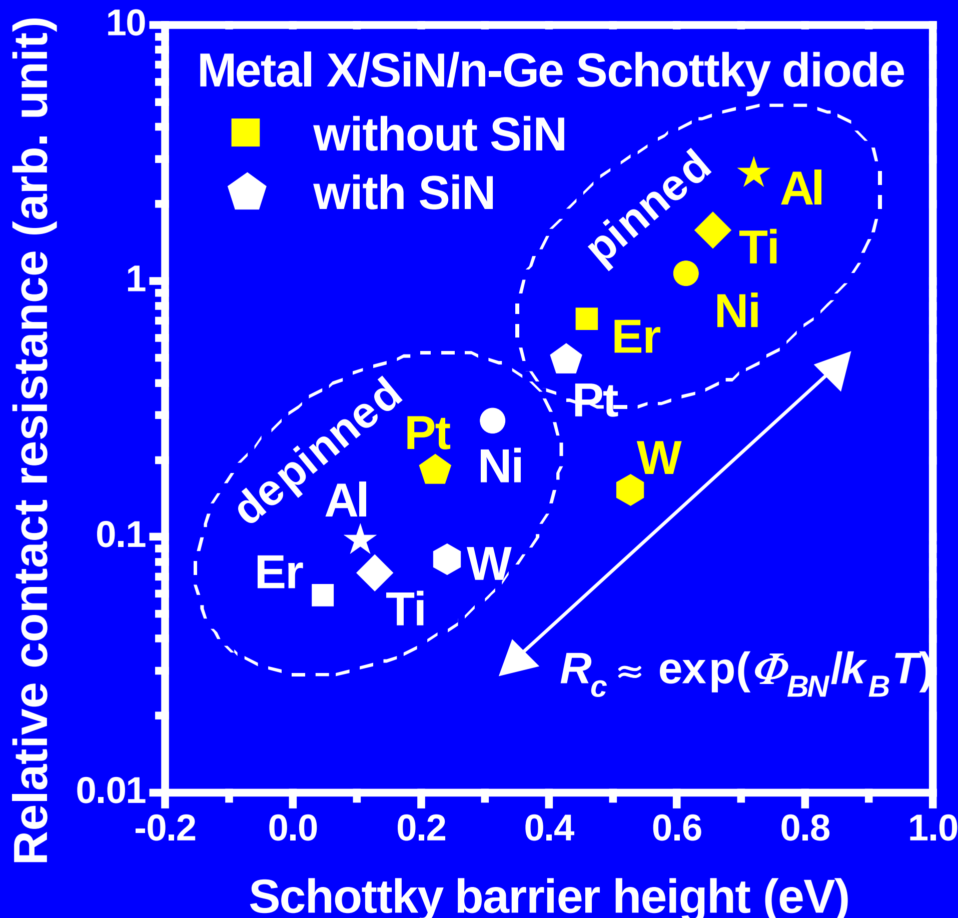
Schottky barrier height modulation

- **Schottky barrier height has minimum**
  - Next increase is due to finite SiN tunnel barrier
  - Subsequent decrease is probably due to Poole-Frenkel emission and model is corrupted



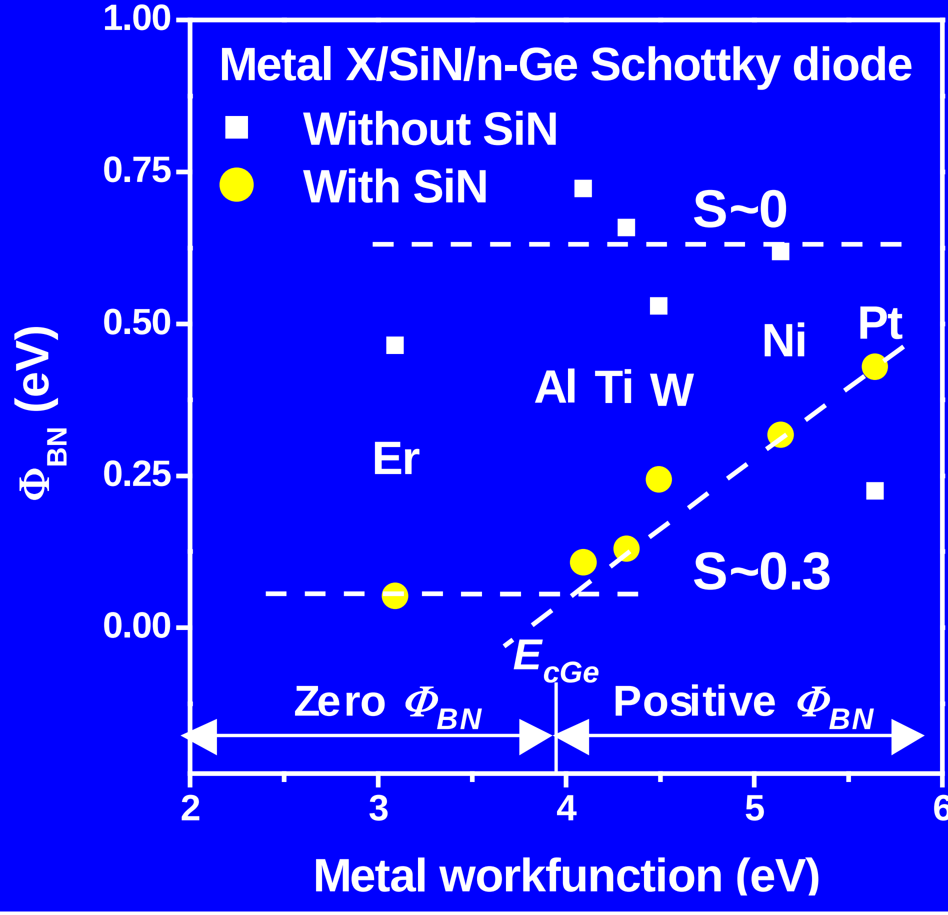
Schottky barrier height modulation

- **Contact resistance / Schottky barrier height**
  - **Good exponential correlation between Rc and Φ_{BNeff}**



Schottky barrier height modulation

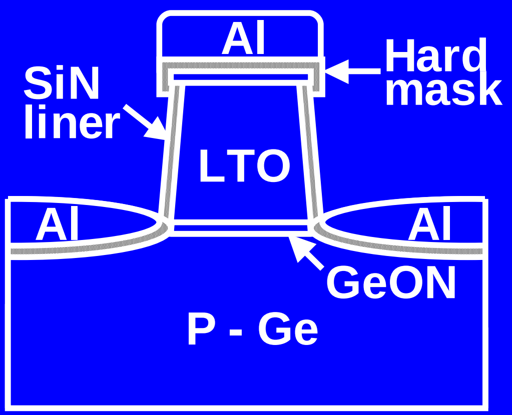
- Pinning factor S: $\Phi_{BNeff} = \underbrace{\Phi_{CNL}}_{\text{Bardeen limit}} + \underbrace{S\,(X_m - X_s)}_{\text{Dipole term}}$
  - Experimentally S=0.3, close to analytical S=0.4



Metal S/D Ge NMOSFET

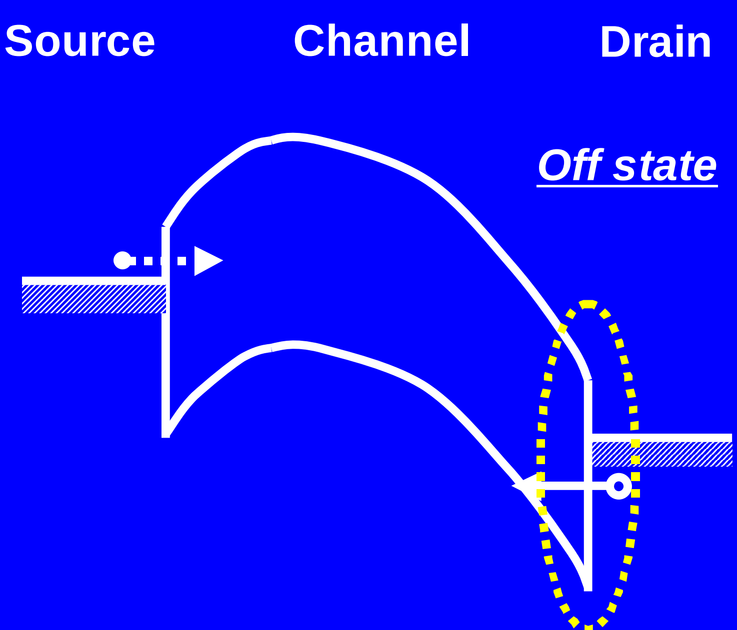
Fabrication process flow

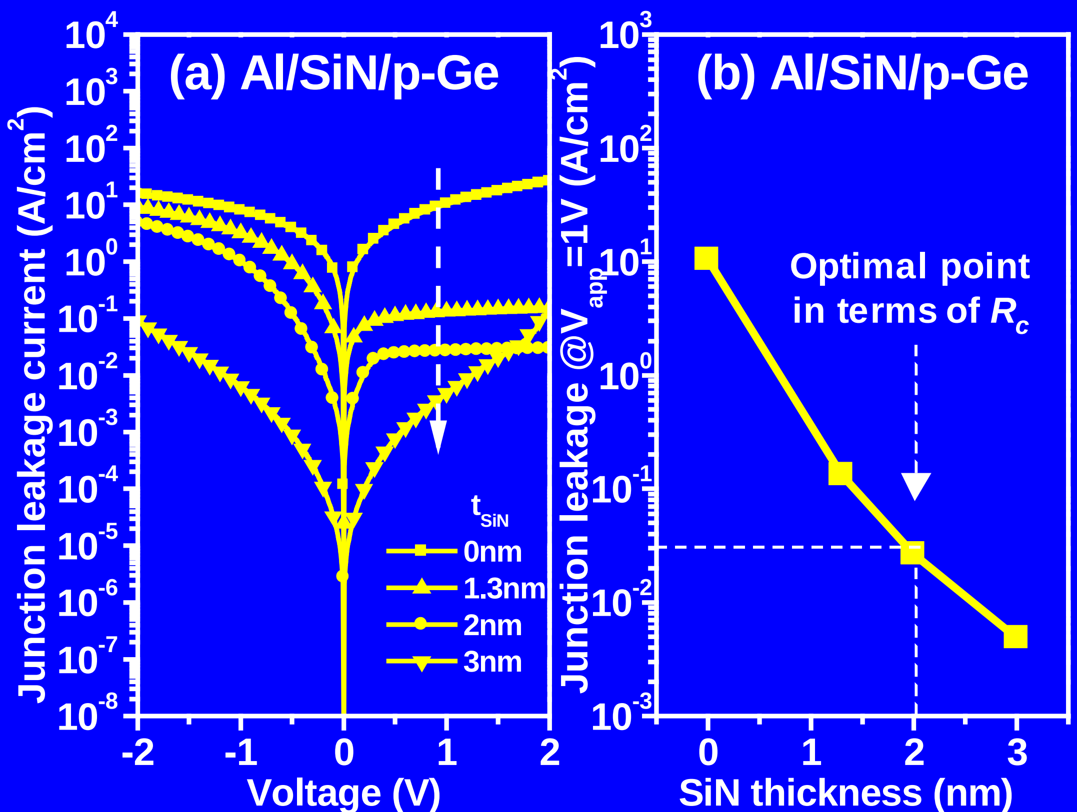
- O2 plasma and HF/HCl cyclic clean/passivation
- Thermal oxinitridation at 600ºC
- LTO and hard mask deposition
- Hard mask anisotropic etch
- LTO/GeON isotropic etch
- Wet treatment
- SiN liner deposition
- Al metal gate and S/D deposition



Metal S/D Ge NMOSFET

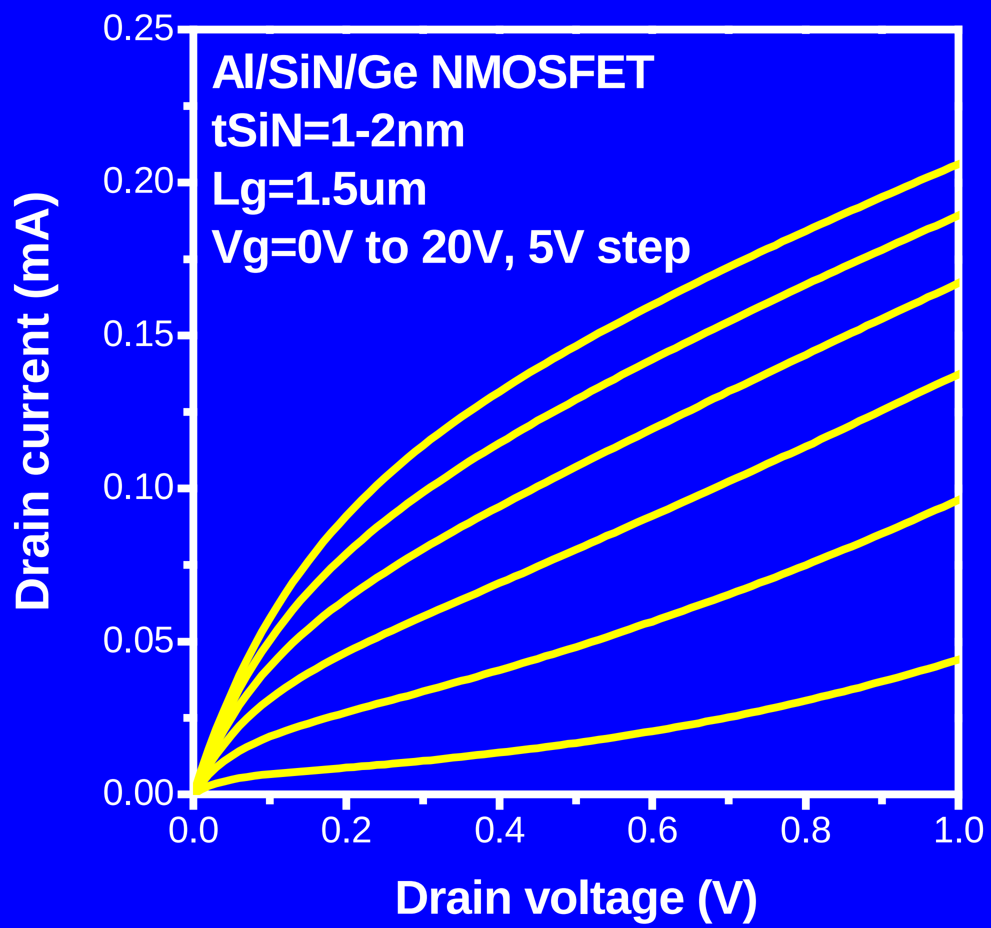
- **Junction leakage characteristics**
  - Ambipolar leakage is a serious problem
  - Achieve low junction leakage due to high Schottky barrier height <u>for hole</u>





Metal S/D Ge NMOSFET

- I_d-V_d characteristics
  - No significant S/D series resistance



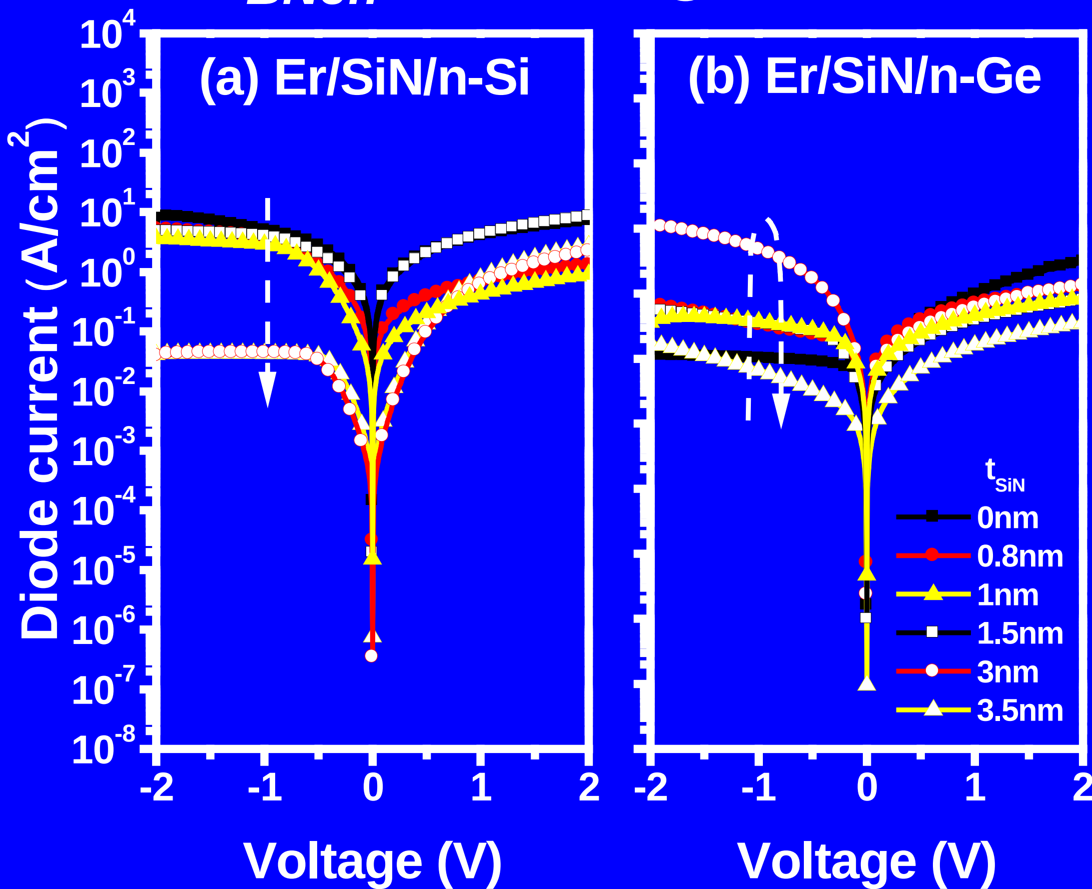
Conclusions

- **Characterize metal/SiN/Ge Schottky diode**
- **Ultrathin interfacial layer effectively release Fermi-level pinning and lower Schottky barrier height**
- **Demonstrate well-behaving metal S/D Ge NMOSFET**
- **This technology is feasible to high-k /metal gate and 3D IC system which require low thermal budget**

Supplement

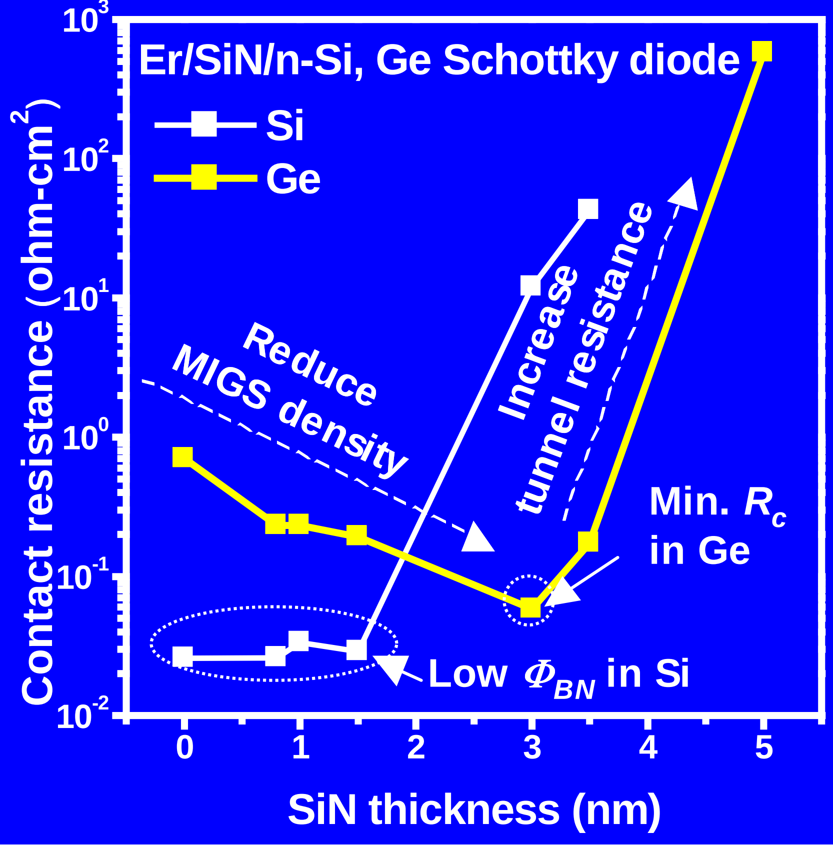
Er/SiN/Ge Schottky diode (1)

- Reverse bias diode current has maximum
  - Due to Φ_{BNeff} lowering



Er/SiN/Ge Schottky diode (2)

- Contact resistance has minimum
  - Two mechanisms are competing
    - MIGS density reduction and tunnel resistance



Er/SiN/Ge Schottky diode (3)

- **Potential injection velocity enhancement due to negative Schottky barrier height**