# Fundamental Challenges for Lithographic Roadmap

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## Intel Lithography Roadmap



193nm lithography ramping & planned through 45nm node
EUV planned for 32nm node (~50nm ½ pitch) and beyond

## Line Width Roughness



LWR: variation in cd impacts loff, ldsat
Origins: PSF, material, etch

# Roughness







←\_50nm→

## Speed Vs. Roughness



Material improvements <u>key</u> to reach targets
 193nm <2nm (45nm node)</li>
 EUV <1.5nm required (32nm node), 2mj/cm<sup>2</sup>



# No Au Au

Tapping mode AFM of resist surface
Gold Coating highlights larger topology
Finer structure and texture obscured
At high resolution, complex structures revealed

d INL NO





Dense line/space patterns tend to collapse at small CDs
 Critical Aspect Ratio for Collapse > 3 & undercut worsen
 Substrate-resist compatibility key
 Concerns raised for sub-50nm CD density variation



Defects size shrinking with CD
Challenging metrology- size, frequency, pattern
Non-uniform dissolution of material
Early engagement for materials improvement



Polymer has discrete volume
PAG addresses volume over catalytic cycle
Sum of addressed polymers in cycle are a limit
Small regular pixels uniformly distributed is trend



A < 2.5 to reach 88° side wall; higher A results in...</li>
Negative tone systems re-entrant: signal loss, collapse
Positive tone systems suffer ragged footing

#### **EUV Transparency**



F, O common in 248 and 193nm, high for EUV
 B < Si < C ~ P < S < Cl << O << F</li>

#### Conclusions

To meet the Intel Roadmap... 193nm extension to 45nm Node will face: Substantially tighter roughness requirements Continued reduction in defectivity EUV application to the 32nm Node will face: Even tighter roughness requirements, coupled with fast photospeed Transparency improvement Continued reduction in defectivity New materials may be key: Polymer composition, structure, control Small molecule distribution control Interfacial energy and structure

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Suppliers who fuel the factories!