Evaluation and Evolution of Low κ Inter-Layer Dielectric (ILD) Material and Integration Schemes

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Disclaimer

- **I am neither a Chemical Engineer nor a Material Scientist**
  - I am an Electrical Engineer with expertise in microfabrication process development

Outline

- Motivation and Goals
- Low κ ILD Material Trend
- Evaluation
  - Phase 1-Materials Analyses
  - Phase 2-Unit Integration Assessment
  - Phase 3-MLM Integration
    - Line-to-Line κ Value Extraction
- Conclusion and Summary

Motivation and Goals

- Interconnect RC delay and power consumption have become performance-limiting factors in ULSI.
  - Need high conductivity interconnect (Cu) and low dielectric constant (κ) ILD.
- Efficient screening of new ULκ materials for successful integration

ILD Material Trend

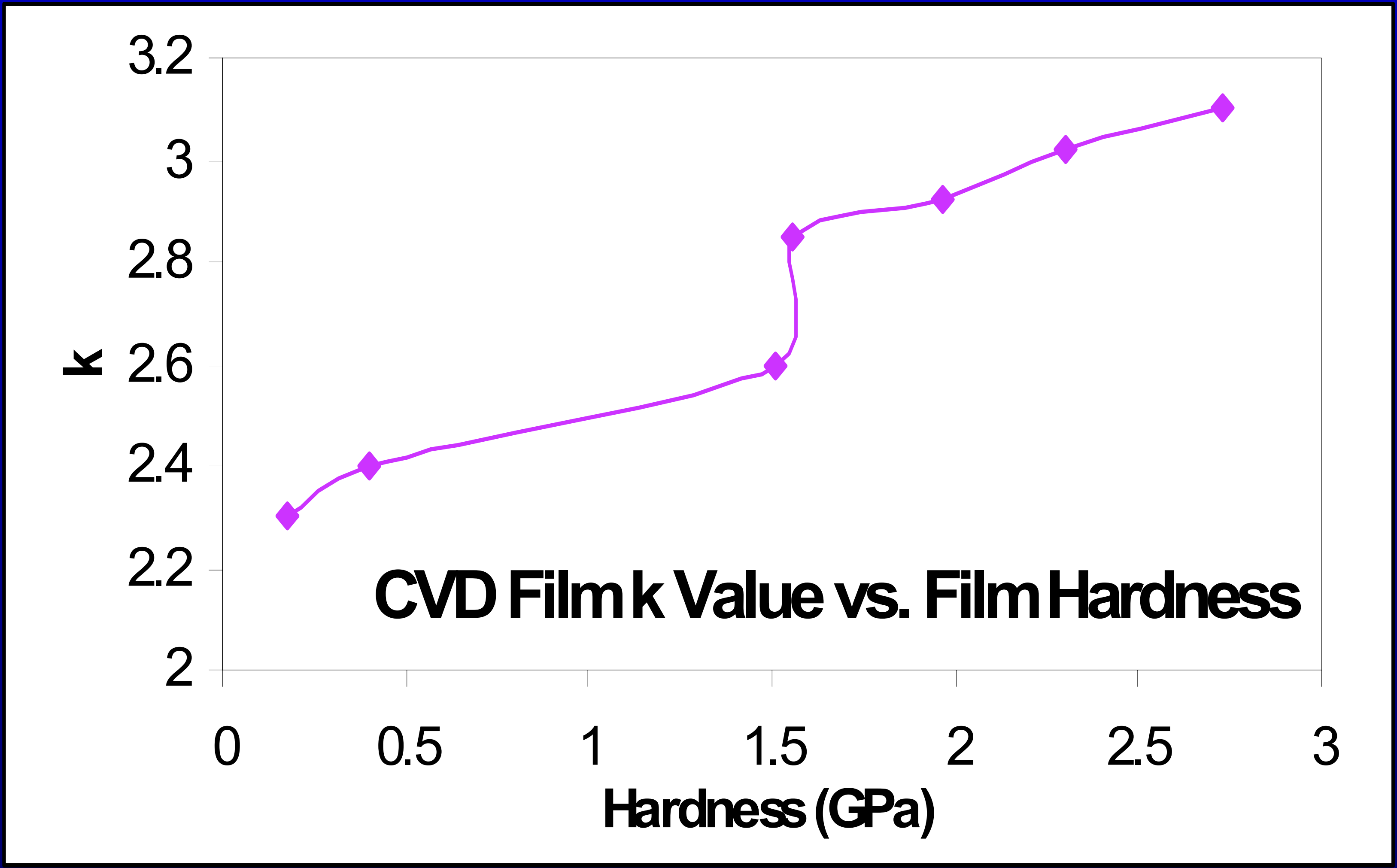
- The widely used ILD material for 0.13 μm and older technologies are PECVD SiO_2 and SiOF.

Materials/Technology	0.13 μm or 0.09 μm	0.07 μm	0.05 μm
Organic	**SiLκ™, Flare™, Paralyne-F(N),** αFC, PAE, etc.	Porous **SiLκ™, porous Flare™ OXD, etc**	Partial Air Gap, Complete Air Gap
Organosilicates	**Carbon Doped Oxide, SOG, etc.**	Porous CVD CDO, Porous SOD CDO, etc.	Partial Air Gap, Complete Air Gap
Range of κ	**2.8 to 3.0**	1.9 to 2.6	1.0 to 1.5

Decreasing the Dielectric Constant

- **Lowering the material density**
  - Add Porosity (air) or lighter elements
  - κ decreases due to κ_{air}~1
  - Thermal-Mechanical properties degrade
  - Pore size and pore connectivity is a major integration concern
- **Lowering the polarizability of bonds**
  - Reduce number of Si-O bonds
  - Include Si-F or Si-C bonds in film
  - Organic materials such as Teflon.
  - Outgassing, adhesion and other TM properties degrade.

κ Trend for Organosilicate Films



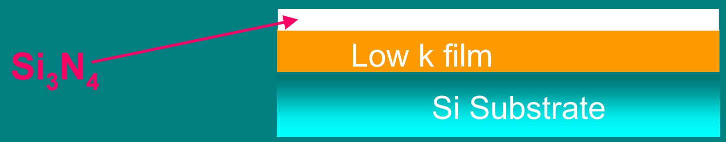
Evaluation Phases

Phase 1	Material Analyses, Material failure-GRC
Phase 2	Unit Integration Evaluation
Phase 3	MLM Integration

Phase 1 Evaluation-Material Analyses

- We propose that material/film suppliers use phase 1 evaluation methodology listed here before introducing new materials to customers.
- Understanding composition and material properties- requires 3 wafers
- Screen-out Materials with unacceptable properties

Wafer No.	*Intended Analyses*	*Film Stack/Thickness*
W1	κ measurement, film stress	500 nm low k film on low resistivity Si
W2	Thermal/mechanical and Material composition, Cracking thickness threshold	2 μm low k film on Si
W3	Outgassing and adhesion	200 nm PECVD SiN on 2 μm low k film on Si



Compositional Analyses

- Know the film before introducing it into the fab
  - Use the Best Known Method (BKM) with standards for these analyses

Analysis	**FTIR**	**Species concentration atomic%**	**Chemical Structure**	**Depth composition Uniformity**	**Density**
Technique	FTIR Spectroscopy	XPS	ToFSIMS	SIMS	XRR, weight
Purpose	Chemical bonds, composition	Chemical composition	Chemical structure of composition	Film depth and within wafer Composition uniformity	K correlation for inorganic

Thermal & Mechanical Analyses

- Avoid particle contamination in the fab

Analysis	Hardness/ Modulus	Thermal Desorption	Stress Hysteresis	Adhesion/Cohesion/ Materials Toughness	Surface Roughness	Pore Metrologyy
Technique	Nanoindentation	Thermal Desorption Spectroscopy	Stress vs. temperature	4-pt bending, Channel Cracking	AFM	EP, PALS, SANS, SAXS
Purpose	Mechanical properties	Quantification of outgassing species, thermal properties	Thermal properties	Adhesion or Cohesion assessment	Film roughness	Size, Size Distribution, Connected or close pores

Phase 1 Analyses-The κ

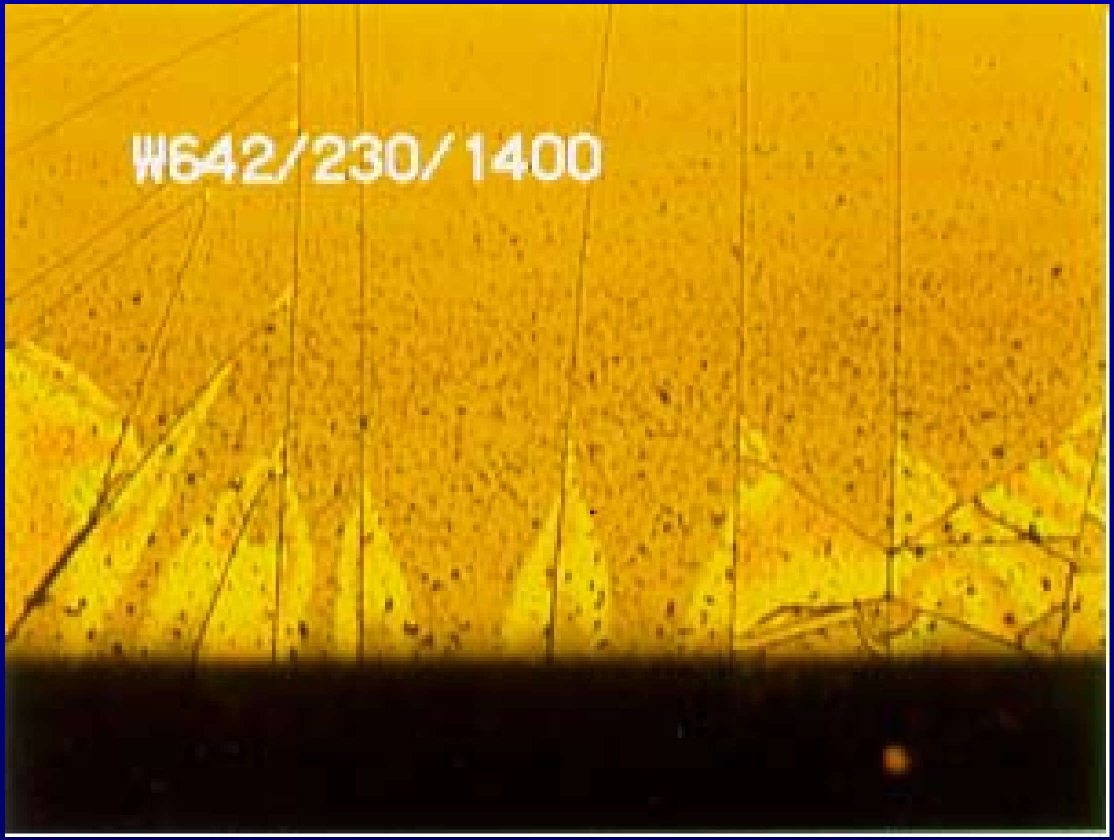
- Is κ value acceptable for the current generation of technology?
- Is there a practical roadmap to improve κ?
  - κ extendibility for the next generation

Phase 1 Analyses-Quick Turn Monitor TM

- 2 μm film cracks?
  - Film crack threshold thickness must be greater than maximum required thickness
- Film outgassing at 425 °C for 1 hour?
  - No blisters or delamination
- Chemical composition
  - Can not contaminate the down stream process tools with heavy metals, etc.
- Center-Edge chemical composition uniformity
  - Etch and CMP process WIW uniformity depends on composition uniformity
  - WIW κ uniformity

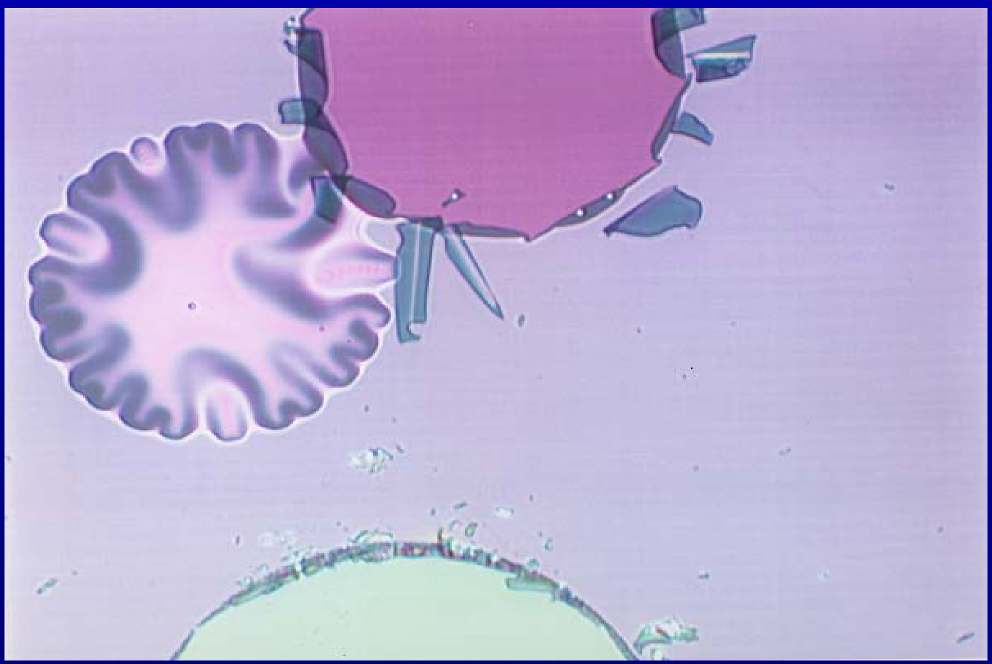
Phase 1 Analyses-Film Cracking

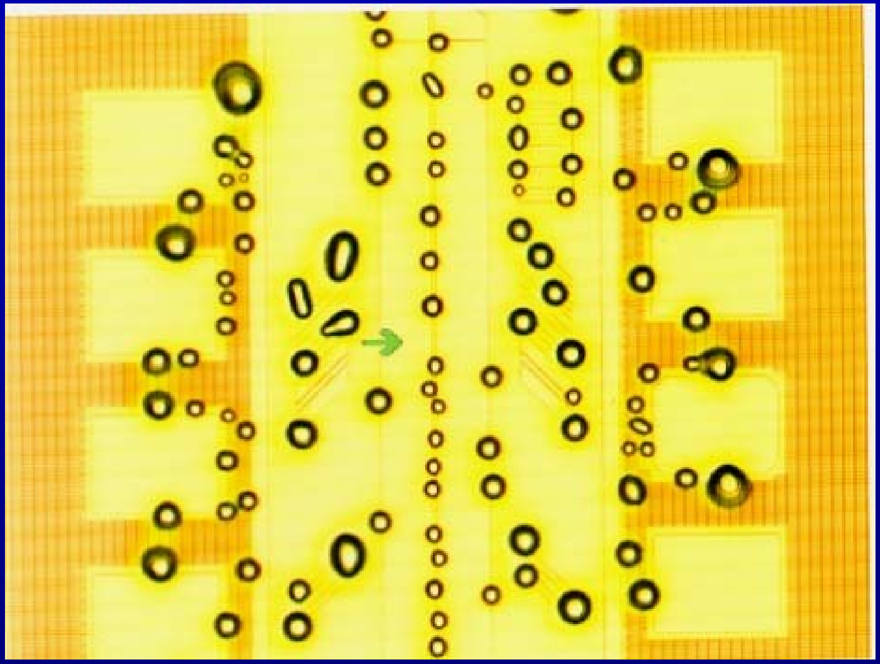
- **Film cracks at the maximum required thickness**



Phase 1 Analyses-Outgassing

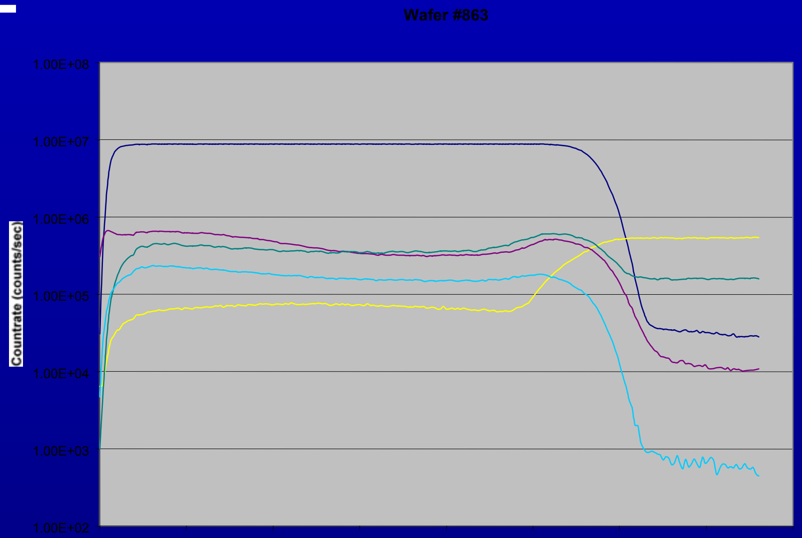
- Downstream process tool contamination

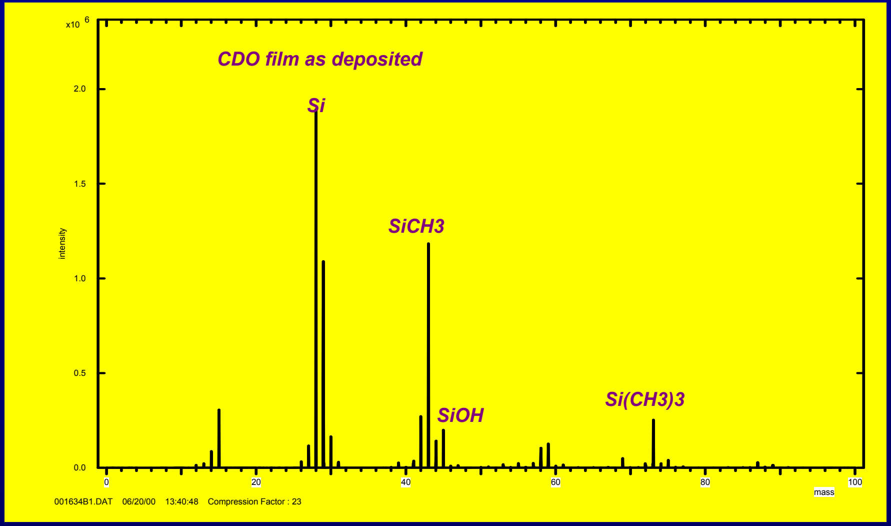




Phase 1 Analyses -SIMS and ToFSIMS Analyses

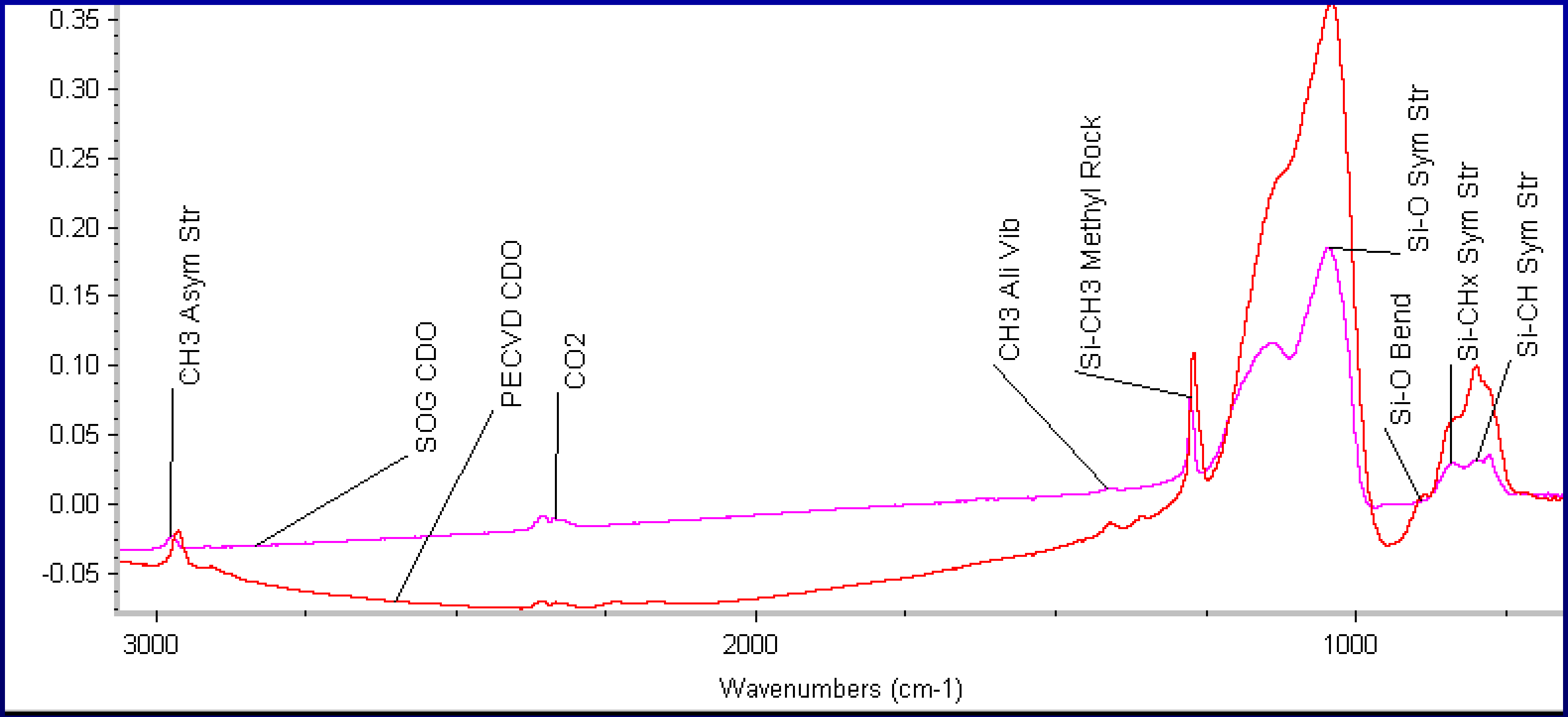
- **Compositional uniformity of the films are important, WIW and WIF**





Phase 1 Analyses-FTIR Analyses

- Chemical bonds peak area ratios can be used for process control and film consistency.



Evaluation Phases

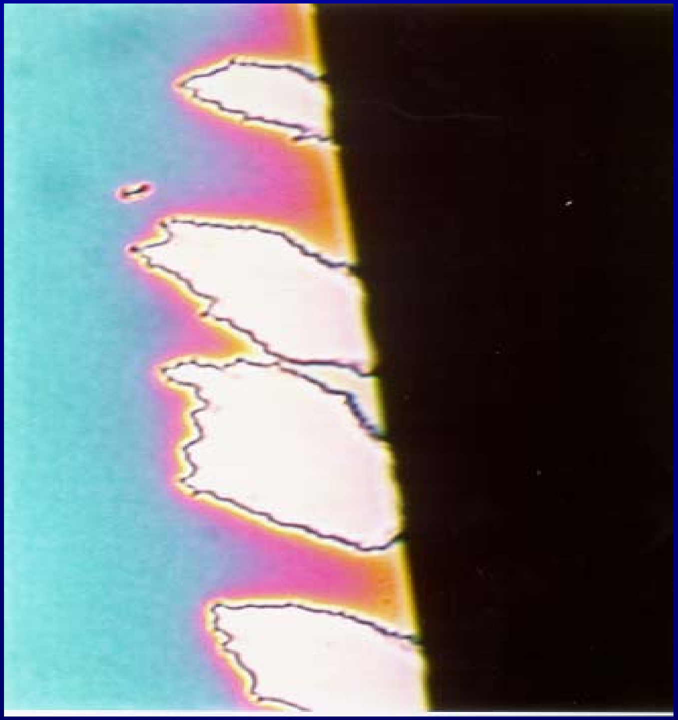
Phase 1	Material Analyses, Material failure-GRC
Phase 2	Unit Module Integration Evaluation
Phase 3	MLM Integration

Phase 2 Evaluation-Unit Module Integration Interaction

- 25 wafers with 1 μm of film needed for phase 2 evaluation
  - Low and high resistivity wafers
- CMP, Pre-Treatment, Ash, Etch process evaluation
- Analysis:
  - Etch rates, ash rates, impact to k, FTIR, SIMS, adhesion, metrology recipe development, etc.

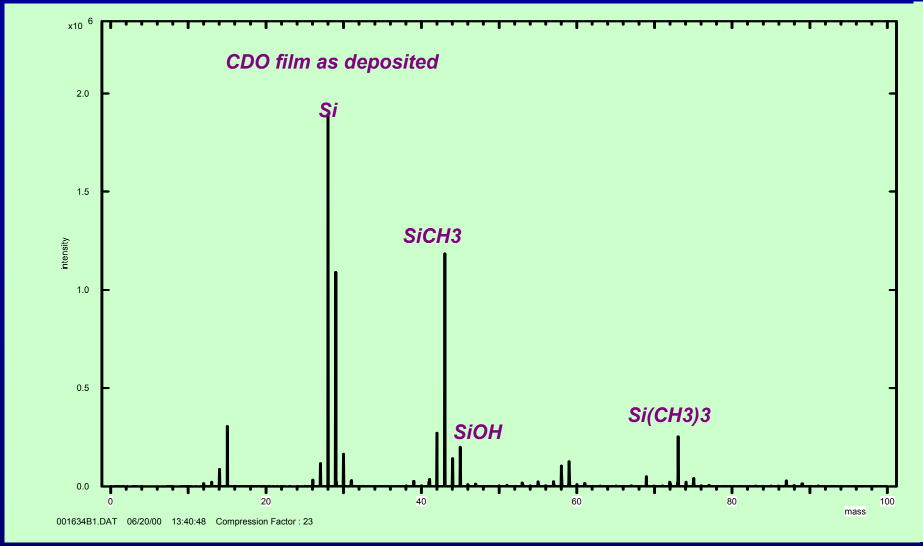
Phase 2 Evaluation-Unit Integration Module Interaction

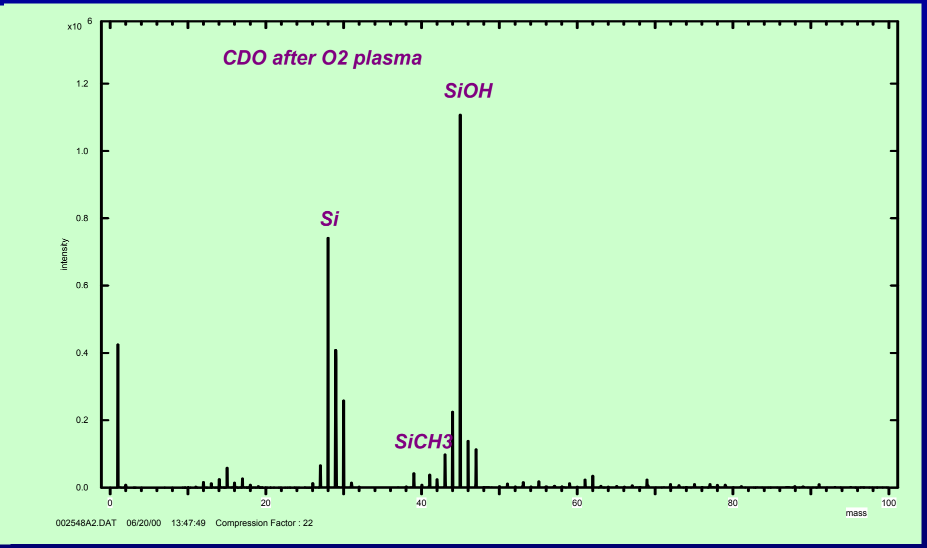
- **CMP process impact**
  - Film delamination- Wafer edge is more susceptible
  - Post CMP clean-some films are hydrophobic



Phase 2 Evaluation-Plasma impact

- **Plasma exposure impacts film**
  - Top layer is carbon depleted-CDO
  - Moisture absorption in the carbon-depleted layer
  - κ increase





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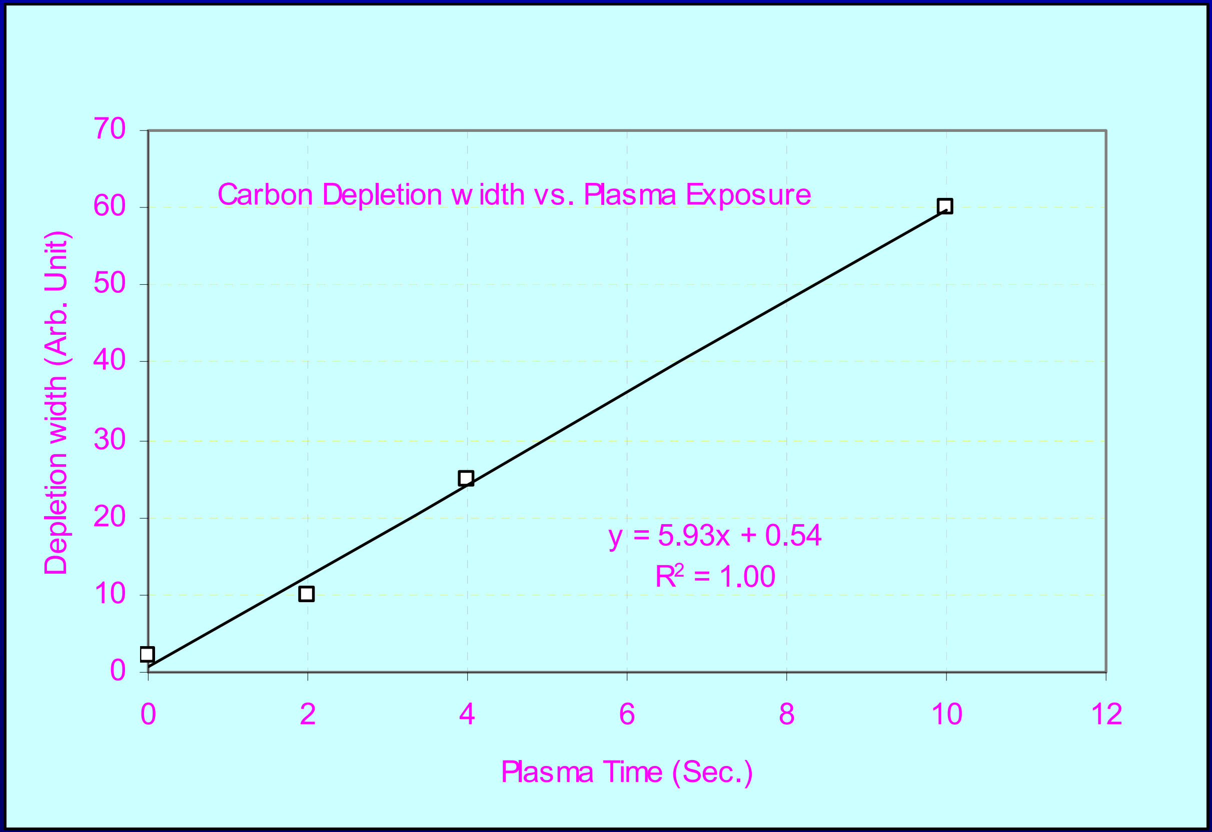
Phase 2 Evaluation-Plasma impact

- Carbon depletion depth is a function of process parameters and duration.



Phase 2 Evaluation-κ Measurement

- **Accurate k measurement is essential for material selection**
  - **Mercury probe measured κ is only a relative value. More accurate measurement is required.**
  - **CV dots deposited by shadow mask produces uncertain electrode area.**
  - **A simple subtractive metal process with multiple size square dots produces the most accurate electrode area.**
  - **Use of low resistivity wafer is recommended to avoid substrate damage by a plasma deposited film and to avoid substrate depletion capacitor complexity.**
  - **Film thickness must be measured in close vicinity of the measured dots.**
    - **New materials may require accurate SEM/TEM thickness measurement.**

Phase 2 Evaluation-Adhesion

- Adhesion of the new materials to hardmask, etch stop, and Cu diffusion barrier must be quantified with 4-pt bend.

- Plasma, thermal or wet clean (Pretreatment) is required in most cases to improve adhesion to new materials.
  - Impact of pre-treatments on κ must be investigated.
  - Avoidance of κ increase or means to restore the κ value is required.

Evaluation Phases

Phase 1	Material Analyses, Material failure-GRC
Phase 2	Unit Integration Evaluation
Phase 3	MLM Integration

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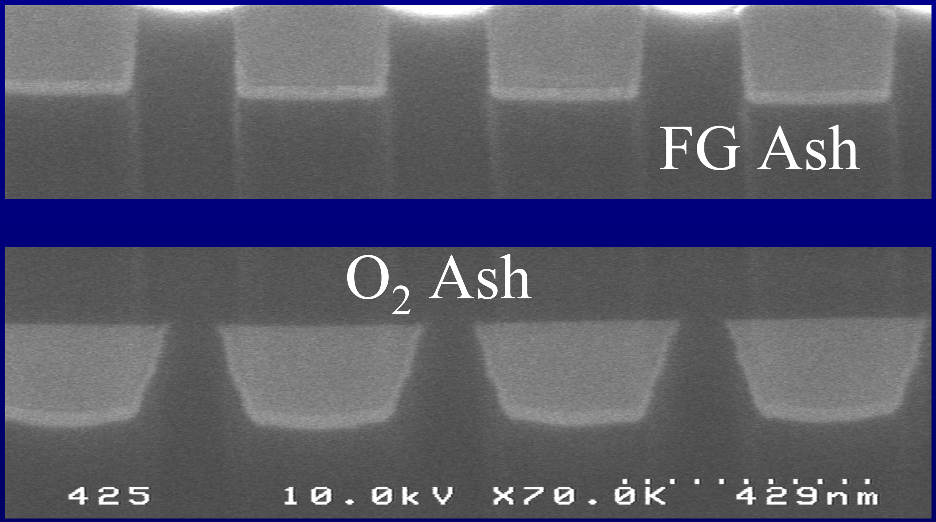
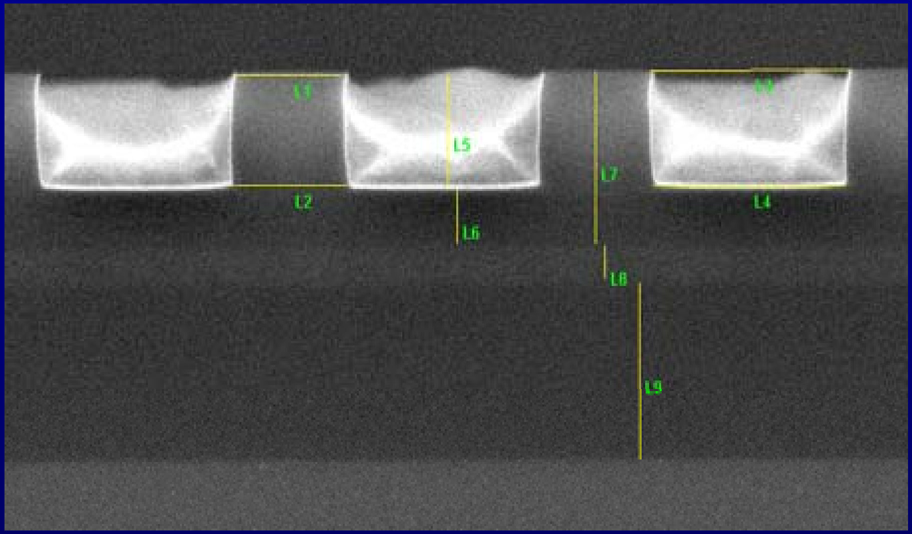
Phase 3 Evaluation-Plasma impact

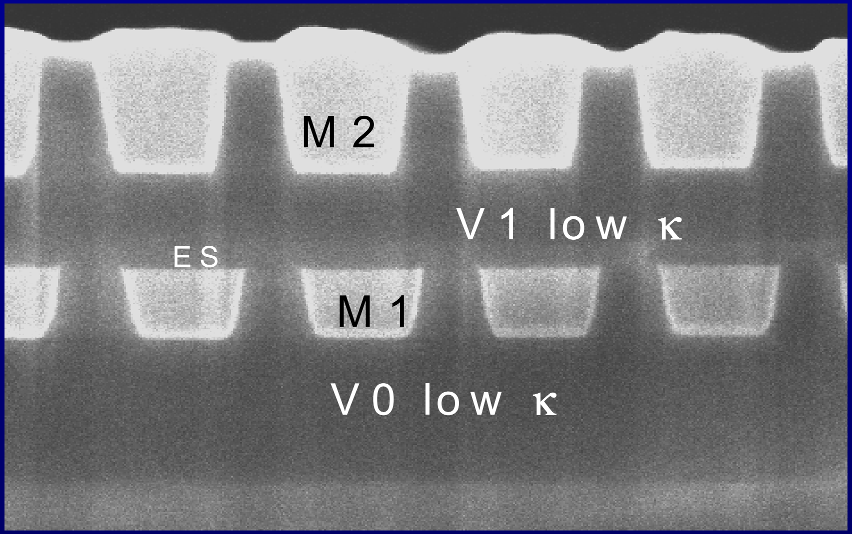
- κ **and etch profile are impacted by the ash process**
  - **The carbon depleted layer is attacked by post ash clean**
- Cu CMP process is impacted by the pattern profile



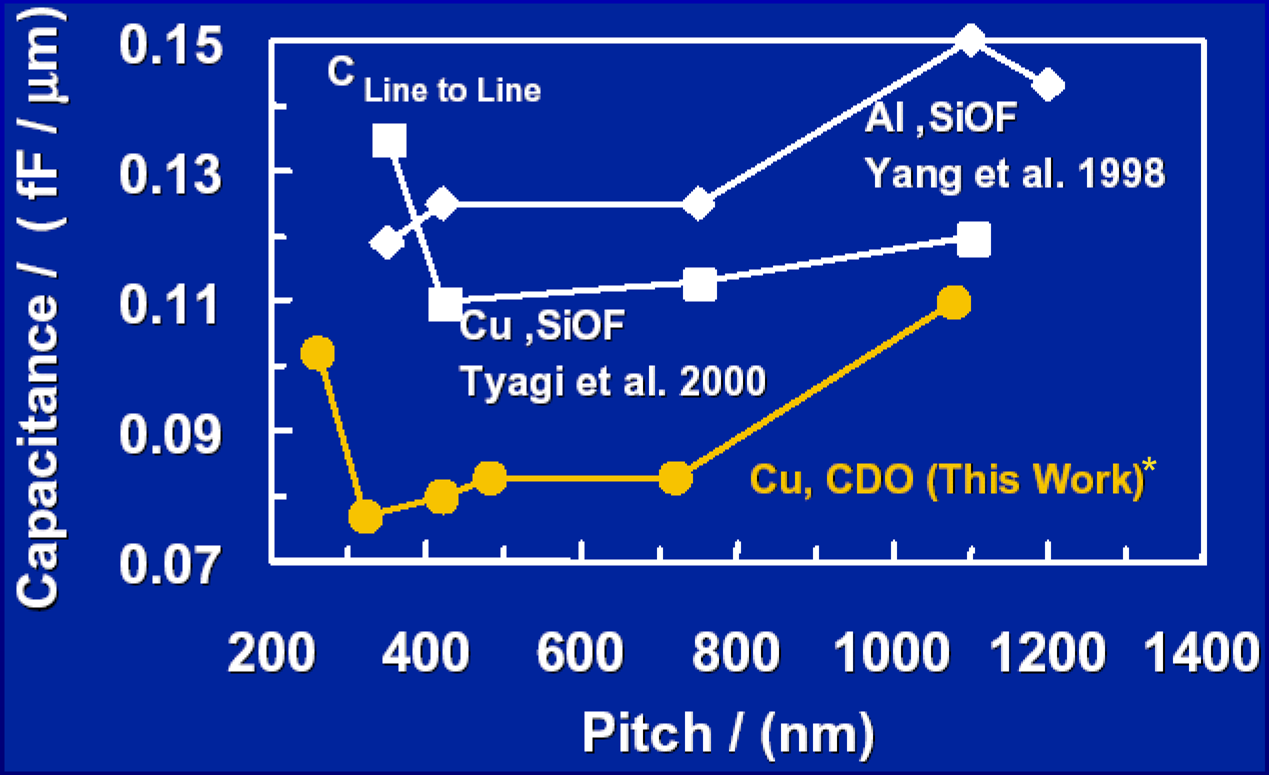
Phase 3 Evaluation-Line to Line κ Measurement

- **All dimensions must be measured to extract the line-to-line κ.**
  - **Trench profile introduce difficulty in measuring κ.**
  - **κ_{eff} measurement requires the second integrated layer.**
  - **Ultimate performance measurement is the ring oscillator f_{max}.**





Line to Line Capacitance



*Thompson et al. IEDM 2002

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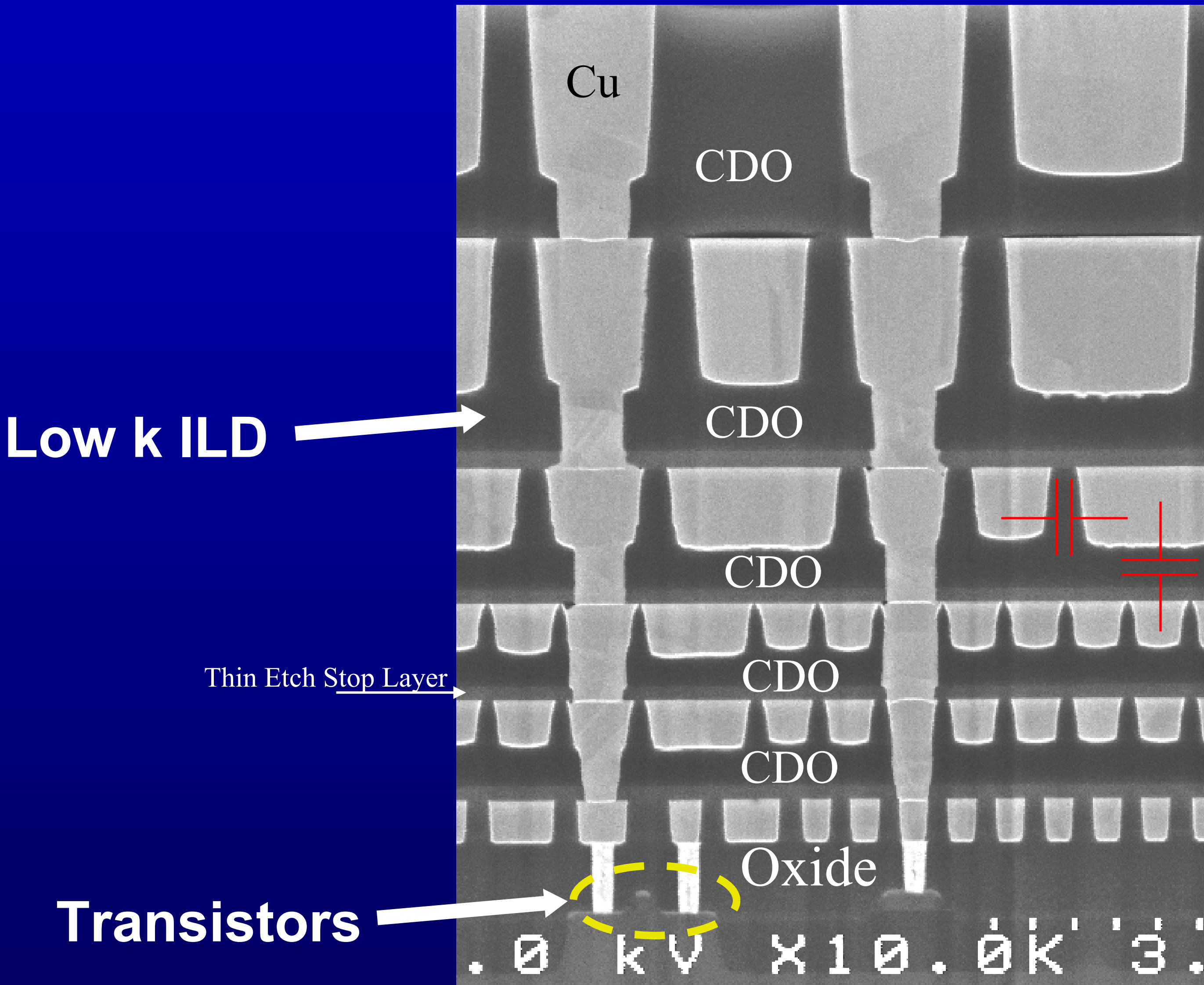
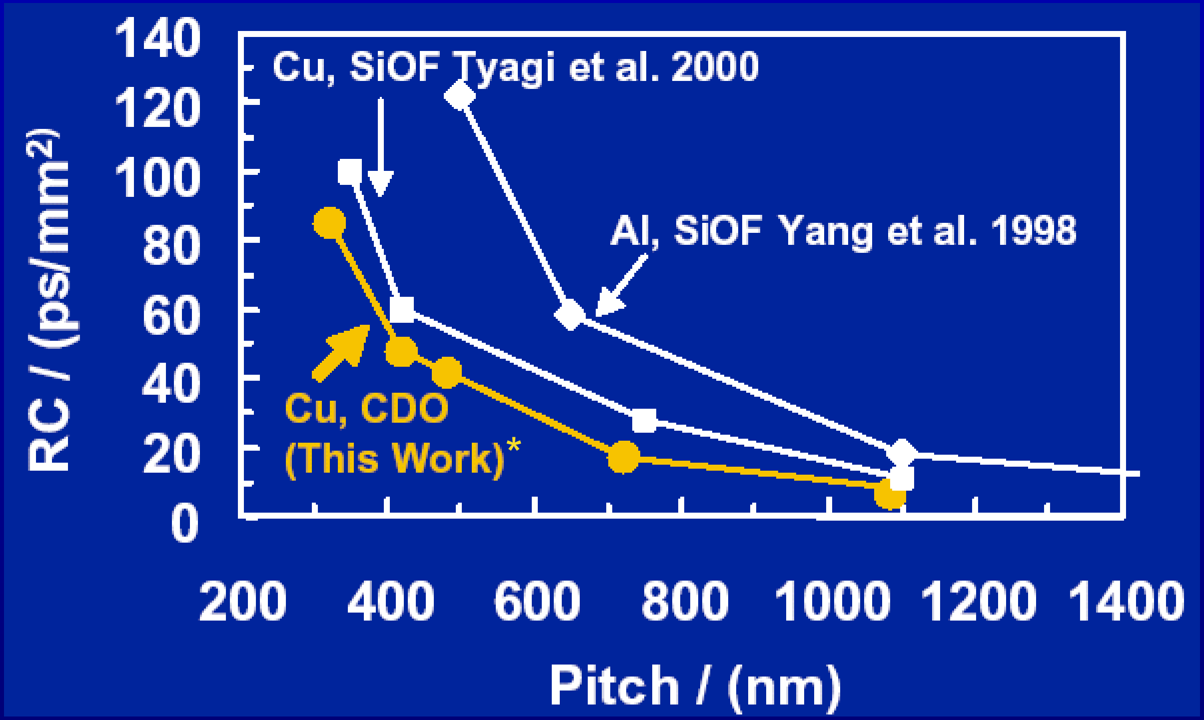
Interconnects



Backend RC Delay



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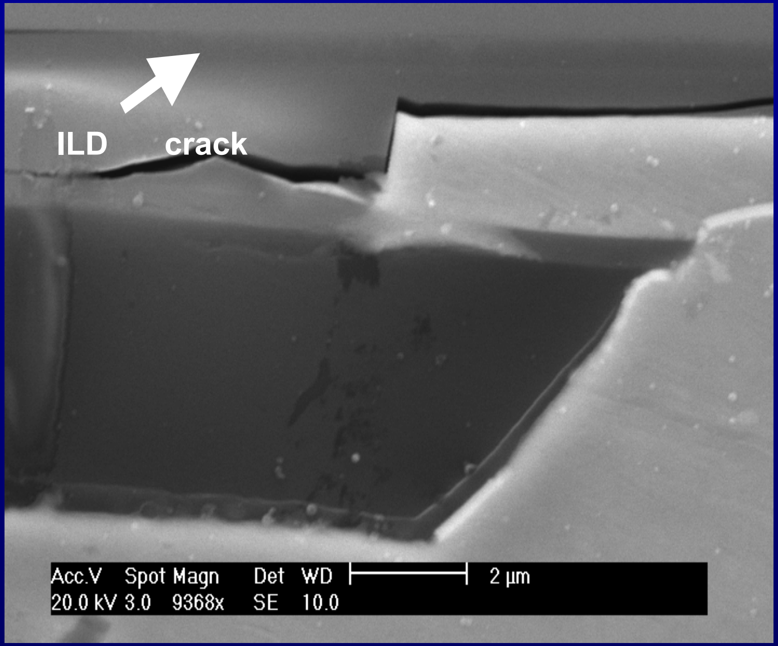
Reliability

- Low k materials are soft and/or brittle.
- Assembly processes must be developed to address the poor material properties.
- They are susceptible to delamination and cracking during reliability test cycles.



Conclusions

- Interconnect engineers face many challenges in evaluating and integrating new materials.
- It is important to screen out new materials and focus resources on minimum number of potential candidates.
- A methodology has been outlined to evaluate the new material efficiently and effectively.
- We have successfully integrated CVD CDO low κ ILD film in 90 nm technology.
- Use of CVD CDO low k ILD can reduce LtL capacitance >20% compared to SiOF.

Acknowledgements

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Biography for Eb Andideh

Eb Andideh received his PhD in Electrical and Computer engineering from University of Illinois at Urbana in 1990. He joined Intel Corporation Portland Technology Development as a Thin Films process development engineer in March of 1990. He has worked on numerous process development projects including ILD gap fill, CMP, selective Si/SiGe epitaxy, and low k ILD material development and integration. He is Currently director of Polymer Memory Technology Development.